: IP Catalog

SIPAC

2005년 8월부터 10월 초까지 22개의 IP가 SIPAC에 새로 등록되었습니다. SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total: 1809 개)

No.	IP Name (Type/Format)	Seller	Category	Description
1	CAN(Controller Area Network) Controller(Software IP / Verilog)	Chonbuk National University (www.chonbuk.ac.kr)	Processor & Micro-controller 〉 Network Processor	통신 속도는 실시간 제어가 가능한 1Mbps(ISO 11898 규격)의 고속 통신을 제공하며 더불어 자동차 환경과 같은 심각한 노이즈 환경에 적합하도록 에러 검출 및 에러 보정의 기능이 있다.
2	SIMD Saturation and average adder (Soft IP / Verilog)	Korea University (www.korea.ac.kr)	Arithmetic & Logic Function	SIMD 구조의 Saturation adder는 다양한 데이터 구조의 영상처리를 위한 연산에 적합한 구조를 지니고 있다. 4개의 8bit 덧셈 및 2개의 16bit 덧셈 그리고 한 개의 32bit 덧셈을 수행 할 수 있을 뿐만 아니라 Saturation 덧셈을 수행 함으로써 기존의 Wraparound 방식에 의한 데이터의 손실을 없앨 수 있다.
3	IEEE 802.16 TC(Transmission Convergence) Sublayer(Firm IP / EDIF)	Wonkwang University (www.wonkwang.ac.kr)	Data Transmission 〉 Format Conversion	An firm IP on a transmission convergence(TC) sublayer for broadband wireless access(BWA) system based on IEEE 802.16 is described, which performs formatting TC PDUs to MAC PDUs, RS encoding/decoding and providing various control signals for a PHY modem.
4	EDCA Coordination(Soft IP / VHDL)	Chonbuk National University (www.chonbuk.ac.kr)	Networking	This IP is coordination sub-block in IEEE 802.11e EDCA protocol It supports EDCA MAC functions as like AC and AIFS.
5	A VLSI Architecture for New Motion Estimation Based on Bit-Plane Matching(Hard IP / GDS II)	Korea University (www.korea.ac.kr)	Digital Signal Processing 〉 Others	Architecture performs binary motion estimation using 1-bit plane image of the video sequence. Motion estimator can be implemented using simple Boolean function only, which can greatly reduce the hardware cost and the time overhead.
6	X-ray Image Sensor (Hard IP / GDS II)	Changwon National University (www.changwon.ac.kr)	Analog & Mixed Signal	-Pixel Array =128 X 128 / Pixel Size = 50 X 50 (um)^2 -Clock Frequency =5MHz / Supply Voltage =5V -Chip Size = 8.1 X 8 (mm)^2
7	RFID Tag Chip 용 EEPROM (Hard IP / GDS II)	Changwon National University (www.changwon.ac.kr)	Memory Element 〉 Flash Memory	Hynix 0.25um공정을 이용하여 RFID Tag chip에 사용되는 syncronous EEPROM 1Kbit IP를 설계하였고, 외부의 주파수를 이용하여 자체적으로 Program과 Erase, Read를 할 수 있다.
8	Voltage-Down Converter using Hynix 0.25um CMOS Process (Hard IP / GDS II)	Changwon National University (www.changwon.ac.kr)	Memory Element	Voltage-Down Converter used as internal current driving and stable voltage level at Process, Supply Voltage and Temperature
9	Photon Counting용 PREAMP (Hard IP / GDS II)	Changwon National University (www.changwon.ac.kr)	Analog & Mixed Signal 〉 Operational Amplifier	A Premamp for Photon Counting is circuit that amplifies small charge pulse signal and devides charge. Amplification is decided by total loadcap.
10	PAD ISS(Software IP / python)	Pusan National University (www.pusan.ac.kr)	Software	PNU Audion Digital Signal Processor Instruction Set Simulator
11	bit-serial 1D DWT filter (Soft IP / Verilog)	Catholic University (www.cuk.ac.kr)	Digital Signal Processing 〉 Transform 〉 Others	Discrete wavelet transform (DWT) is the oncoming generation of compression technique that has been selected for MPEG4 and JEPG2000, because it has no blocking effects and efficiently determines frequency property of temporary time.

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12	Wrappers for Multiple-Clock Operations(Soft IP / VHDL)	EDA Lab., Chungnam National University(eda.cnu.ac.kr)	Bus Interface 〉On Chip/System Bus Interface 〉Others	Wrappers for Multiple-Clock Operations – 온 칩 버스와 다양한 IP (Intellectual Property)들을 이용하는 시스템 온 칩 설계에서 발생되는 Multiple-Clock Operation을 지원하는 Wrapper – Clock Speed 차가 정수 배인 경우만 사용 가능
13	2D DWT for JPEG2000 (Soft IP / Verilog)	Chungnam National University (www.chungnam.ac.kr)	Digital Signal Processing 〉Filter	In this IP, We implementated Lifted architecture for integer(5,3) DWT(Discrete Wavelet Transform). This architecture is suitable for both decomposition and reconstruction of signal, and high frequency operation.
14	MAC evaluation IP for ADSRC (Soft IP / C/C++)	Chonbuk National University (www.chonbuk.ac.kr)	Wireless Communications	This IP is for MAC process and available for ADSRC. The IP includes DCF, Management and WEP function.
15	Control Software for 1.9MHz GPS Radio Buoy(Software IP / Assembly)	Anyang University (www.anyang.ac.kr/)	Software 〉Application	– System and protocol control software for 1.9MHz Radio buoy – Used for deep sea fishery applications – Automatic position finding by GPS technology
16	Control S/W for 27MHz GPS Radio Buoy(Software IP / Assembly)	Anyang University (www.anyang.ac.kr/)	Software 〉Application	– Control S/W for 27MHz Radio Buoy for inshore and deep sea fishery – Automatic Position finding using GPS Technique
17	IEEE 802.11 MAC with PCI interface(Soft IP / VHDL)	Chonbuk National University (www.chonbuk.ac.kr)	Networking	This IP is that IEEE 802.11 MAC added PCI interface.
18	PTPCIExpress(Soft IP / Verilog)	Perftrends Technologies Inc(www.perftrends.com)	Bus Interface	Perftrends PCI-Express IP Core is compliant with PCI Express Base specification 1.0a, including the Data link, Transaction and Physical layers. This core's architecture is highly modularized and has a synchronous design.
19	PTDDR2(Soft IP / Verilog, EDIF)	Perftrends Technologies Inc(www.perftrends.com)	Memory Element	Perftrends DDR2SDRAM Controller IP Core is designed for use in ASICs requiring high memory throughput, high clock rates and full programmability. The DDR2SDRAM controller performs all initialization and refresh functions.
20	Charge Pump(Hard IP / GDS II)	Changwon National University (www.changwon.ac.kr)	Analog & Mixed Signal 〉Regulator	VRD(VPP) Generator의 Block Diagram은 Reference Voltage Generator, Voltage-Down Converter, VPP Level Detector, Ring Oscillator, VRD Control Logic 과 Charge Pump로 구성되어 있다.
21	Speech Interface(Soft IP, Software IP / Assembly, C/C++)	Chonbuk National University (www.chonbuk.ac.kr)	Speech Interface	Interface Implementation between Facility Equipment and Driver using Speech Recognition and Synthesis in Intellectual Vehicle. Robust noise reduction algorithm in car environment. Improvement speech detection. Speech feature vector extraction regard to the auditory characteristic
22	UWB Impulse Generator (Soft IP, Hard IP / GDS II, ADS)	Jeonju University (www.jj.ac.kr)	Wireless Communication	–1ns Gaussian Impulse Generation –1ns Monocycle Impulse Generation