: IP Catalog

SIPAC

2005년 6월부터 7월 말까지 180개의 IP가 SIPAC에 새로 등록되었습니다. 지면관계상 37개의 IP의 정보를 제공해 드리며, SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total: 1787 개)

No.	IP Name (Type/Format)	Seller	Category	Description
1	Shading correction system for camera applications(Soft IP / Verilog)	Dong-a University (www.donga.ac.kr)	Digital Signal Processing	1. Programmable maximum compensation value (9 types) 2. Programmable correction-weight line curvature (5 types) 3. Maximum Single 50 MHz Clock available 4. Available for Various Image Resolution (39 types)
2	CI3122ja - 16-Bit, Stereo ADC(Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal > Converter > ADC	16 bit A/D conversion / 93 dB Dynamic Range / Single-ended inputs / Complete stereo ADC system / Analog Filter with S-E to Diff conversion / Delta-Sigma Multibit modulator / 64X Decimation Filter
3	Multichannel Fraction Resampler(Firm IP / EDIF)	Chipidea Microelectronica SA (www.chipidea.com)	Digital Signal Processing > Building Block	The resampling rates can be selected with high precision, and allow selection of output sample rates with a resolution less than one Hertz. When operating on multiple input channels, the architectures treat each channel independently, allowing different input/output sampling rates, and rate changes for each channel.
4	CI8332ee - Stereo Audio DAC with Mixing Line Input(Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal > Converter > DAC	20-bit 93dB Dynamic Range 48kHz Sampling Frequency Stereo Audio DAC with Mixing Line Input10kOhm line loads and 74dB Dynamic Range, -65dB THD 32Ohm loads at 20mW output power
5	MXL450 : VESA MDDI Transceiver(Hard IP / GDS II)	Mixel, Inc.(www.mixl.com)	Bus Interface > LVDS	This is an LVDS transceiver compliant with the VESA Mobile Display Interface Client specifications. Wide common mode voltage receivers are used to meet the input common mode voltage required by the VESA MDDI standard.
6	MXL4254A : 4.25 Gbps Transceiver + SERDES + CDR(Hard IP / GDS II)	Mixel, Inc.(www.mixl.com)	Peripheral Core > Receiver / Transmitter	The MXL4254A is a Quad Gigabit transceiver implemented in digital CMOS technology. Each of the four channels supports data rate from 1 to 4.25 Gbps. It is compatible with router-backplane links, PCI Express, RapidIO,
7	MXLSYN : Frequency Synthesizer PLL (Hard IP / GDS II)	Mixel, Inc.(www.mixl.com)	Analog & Mixed Signal > PLL/DLL	The MXLSYN is a high performance PLL based frequency synthesizer implemented using a digital CMOS technology. It is highly integrated and requires no external components.
8	MXLBGRLV : Low Voltage BandGap Reference(Hard IP / GDS II)	Mixel, Inc.(www.mixl.com)	Analog & Mixed Signal > Voltage Reference	The MXLBGRLV is a CMOS Bandgap reference that can operate from a power supply as low as 1V. It is implemented in digital CMOS technology and generates a reference voltage that is temperature, process, and power supply independent as well as reference currents.
9	Symbol Detector for SDM-OFDM(Soft IP/ Verilog)	Yonsei University (www.yonsei.ac.kr)	Wireless Communications	Symbol Detector for SDM-OFDM system - Using SQRD(sorted QR decomposition) algorithm. - Consider 2 transmit/receive antennas
10	Symbol Detector for SFBC-OFDM with Interference Cancellation(Soft IP / Verilog)	Yonsei University (www.yonsei.ac.kr)	Wireless Communications	- Symbol Detector for SF(Space-Frequency) OFDM system with the interference cancellation - Consider 2 transmit/receive antennas
11	Phase tracking module for 2x2 MIMO OFDM system(Soft IP / Verilog)	Yonsei University (www.yonsei.ac.kr)	Wireless Communications > 802.11	-Phase error calculator and compensator for 2x2 MIMO OFDM system -Use pilot pattern in 802.11n system -Consider 2 transmit/receive antennas
12	Local Adaptive Contrast Enhancement (Soft IP / Verilog)	Yonsei University (www.yonsei.ac.kr)	Digital Signal Processing	- Enhance the contrast adaptively - Real time adaptive contrast enhancement
13	Advanced Color Interpolation(Soft IP / Verilog)	Yonsei University (www.yonsei.ac.kr)	Digital Signal Processing > Others	Interpolating missing two channels of CFA image from the neighboring pixels / Considering cross-channel correlation while demosaicking each channel / High quality and low complexity
14	(De)punctured (de)interleaver for IEEE 802.11a WLAN system(Soft IP / Verilog)	Yonsei University (www.yonsei.ac.kr)	Wireless Communications > 802.11	Block interleaving scheme / Support IEEE 802.11a system / The (de)puncturer is combined in the (de)interleaver : The input data are stored in memory by patterns and (de)interleaving permutation simultaneously
15	CI8204va - 10-Bit, 44MHz, IQ-DAC (Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal > Converter > DAC	10-bit, 44 MHz, 3.3 V Current-steering IQDAC with Differential Voltage Buffer / 10-bit Resolution / Above 44 MS/s Sampling Rate / 2Vpp Voltage Output / 3.3+/-10% Analog Power Supply
16	CI5021ia - Third-Order Active-RC Filter (Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal > Analog Filter	Programmable 200 kHz/500 kHz/3MHz Third-Order Active-RC Filter with Auto-Calibrated Offset / Low current consumption 2.3 mA / Supply voltage 2.7 to 3.6 V / Programmable cut-off frequency 200 kHz, 500 kHz, 3000 kHz
17	CI1411tl - 1.056GHz programmable clock-multiplying PLL(Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal > PLL/DLL	0.13 um Generic CMOS technology / Fully integrated, compact design / 1.2 V single supply operation / 6mA typical current consumption / Minimum comparison frequency 19MHz / Output frequency from 660MHz to 1.056GHz

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18	Multi-Layer AHB BusMatrix(Soft IP / VHDL)	Chungnam National University (www.chungnam.ac.kr)	Bus Interface > On Chip/System Bus Interface > AMBA	Multi-Layer AHB BusMatrix which provides variable arbitration method1. Fixed Priority based Arbitration method2. Arrival Sequence based Arbitration method3. Round Robin based Arbitration method
19	The Verification Environments for Multi-Layer AHB BusMatrix(Soft IP / VHDL, C/C++)	Chungnam National University (www.chungnam.ac.kr)	Bus Interface > On Chip/System Bus Interface > AMBA	Verification environment about simulation for Multi-Layer AHB BusMatrix- AHB-Lite Master BFM / AHB-Lite Slave BFM - AHB-Lite Master Protocol Checker / AHB-Lite Slave Protocol Checker
20	JPEG Decoder(Soft IP / VHDL)	Handong Global University (www.han.ac.kr)	Digital Signal Processing	This JPEG decoder converts the JPEG stream into RGB video signal. This JPEG decoder is designed for sequential DCT-based decoder. It supports only 4:2:0 mode(Y:Cb:Cr = 4:1:1). Our Implementation targeting Xlinx Sprtan2 FPGA shows 4000 blocks/sec processing performance with 25 MHz clock.
21	CLAP Logic Analyzer(Soft IP / Vhdl, C/C++)	Chungnam National University (www.chungnam.ac.kr)	Verification Component	Logic Analyzer Software & Hardware for Design Verification of Digital Circuits on FPGA board- Data Width: 8, 16, 32, 64, 128, 256 bit - OSC Frequency: 5, 10, 20, 25, 40, 50 MHz
22	Simple Multi-Layer AHB BusMatrix (Soft IP / VHDL)	Chungnam National University (www.chungnam.ac.kr)	Bus Interface > On Chip/ System Bus Interface > AMBA	Simple Multi-Layer AHB BusMatrix- Decreasing of Latency Time, Power Consumption and Hardware Overhead
23	Xilinx FFT Library(Firm IP / EDIF)	RF Engines Ltd.(www.rfel.com)	Digital Signal Processing > Transform > FFT(Fast Fourier Transform)	RF Engines? FFT Library provides developers with a range of high performance Fast Fourier Transform (FFT) cores for Xilinx FPGA. The cores are designed to be highly silicon efficient and support complex sample rates up to 500 MHz.
24	12bit, 80MS/s Nyquist-Rate Dual ADC (Hard IP / GDS II)	AnaFocus(www.anafocus.com)	Analog & Mixed Signal > Converter > ADC	The cell is a dual high-performance fully differential, low-power 12-bit 80MS/s pipelined ADC core designed for 0.13um CMOS 1P6M (1.2V/3.3V) CMOS technology.
25	12bit, 80MS/s Nyquist-Rate DAC (Hard IP/GDS II)	AnaFocus(www.anafocus.com)	Analog & Mixed Signal > Converter > DAC	The cell is a complete high-performance fully differential high speed current-steering DAC core designed for consumer electronics and communication applications.
26	12bit, 224kS/s 4-input ADC (Hard IP / GDS II)	AnaFocus(www.anafocus.com)	Analog & Mixed Signal > Converter > ADC	The cell is a complete 12bit 224kS/s low-power ADC core designed as part of an sensor front-end for the automotive industry.
27	14bit, 4.4MS/s Sigma-Delta ADC (Hard IP/GDS II)	AnaFocus(www.anafocus.com)	Analog & Mixed Signal > Converter > ADC	The cell is a complete low-power 14bit 4.4MS/s sigma-delta ADC core designed for xDSL MODEM front-end. It achieves 86dB dynamic range (14bit effective resolution) with optimized power consumption.
28	17bit, 9.6kS/s Sigma-Delta Audio ADC (Hard IP / GDS II)	AnaFocus(www.anafocus.com)	Analog & Mixed Signal > Converter > ADC	The cell is a complete 16.4bit 9.6kS/s sigma-delta very low-power ADC core designed for high-quality audio applications in 0.7um (5V) CMOS technology.
29	24bit, 50kSample/s Stereo Audio DAC (Hard IP / GDS II)	AnaFocus(www.anafocus.com)	Analog & Mixed Signal > Converter > DAC	The cell is a complete, high-performance, single-chip, stereo audio digital-to-analog converter delivering 95dB dynamic range. Input format is 3 wire serial, Inter-IC Sound (I2S) format, standard in audio applications.
30	DMA delay time optimized PCI 64bit/66MHz bus interface logic(Soft IP, Firm IP / VHDL)	Pusan National University (www.pusan.ac.kr)	Bus Interface > Peripheral Bus Interface > PCI (Peripheral Controller Interface)	PCI V2.2 compatible / PCI 64bit/66MHz / PCI master/target / Minimize latency time for DMA / Support 2 interrupts
31	SIMD MAC (Multiply and Accumulate) Unit (Soft IP / Verilog)	Korea University(www.korea.ac.kr)	Arithmetic & Logic Function	This is a SIMD Multiply-Accumulate (MAC) unit for embedded systems. Its design of the tree that sums up the partial products generated according to the selected precision, “a single 32bit x 32bit , dual 16bit x 16bit and quad 8bit x 8bit operation”, is applied by using “shared segmentation” scheme, which is allegedly the best scheme.
32	A 10bit, 50MHz Pipeline architecture, ADC (Hard IP / GDS II)	Keimyung University (www.keimyung.ac.kr)	Analog & Mixed Signal > Converter > ADC	A 10-bit, 50MHz Pipeline architecture, analog to digital converter The converter was implemented with a 9 stage pipeline architecture, with 1.5 bits per stage.
33	Low power Oscillator(Hard IP / GDS II)	Keimyung University (www.keimyung.ac.kr)	Analog & Mixed Signal > PLL/DLL	Low power Oscillator for Embbeded System.
34	RAMP-C2(Software IP / Verilog)	KAIST(www.kaist.ac.kr)	Digital Signal Processing	A 3D rendering accelerator for handheld devices. It supprots gouraud shading, pixel alpha blending, texture mapping and texture blending. It can draw a 3D graphics image with the speed of 20Mpixels/sec.
35	ADSL Front-end Programmable gain controlled Amplifier(PGA)(Hard IP / Spice)	Chonbuk National University (www.chonbuk.ac.kr)	Analog & Mixed Signal	Two low voltage 3V CMOS programmable gain-controlled amplifier(PGA)s for using in the transmitter and receiver of ADSL analog front-end are designed. The designed receiver PGA is connected with 1.1MHz continuous-time lowpass filter and controls the gain from 0dB to 30dB.
36	Low-error fixed-width squarer(Soft IP / VHDL)	Chonbuk National University (www.chonbuk.ac.kr)	Arithmetic & Logic Function	This IP is designed for the fixed-width squarer at FEQ block in IEEE.802.11a. This IP uses a design method for fixed-width squarer that receives a 10-bit input and produces a 10-bit squared product.
37	Power control algorithm by using adaptive Carrier wave in OFDM System(Soft IP / Matlab)	Chonbuk National University (www.chonbuk.ac.kr)	Data Transmission	To settle some question such as ISI (inter symbol interference) and mitigating the effects of multipath delay spread of the wireless radio channel effectively, OFDM (orthogonal frequency division multiplexing) seems the best promising answers for this recent uprising demand.