SIPAC

2005년 4월부터 6월 초까지 215개의 IP가 SIPAC에 새로 등록되었습니다. 지면관계상 40개의 IP의 정보를 제공해 드리며, SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total: 1607 개)

No.	IP Name (Type/Format)	Seller	Category	Description
1	AMBA AHB Bus Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Bus Interface 〉On Chip/System Bus Interface 〉AMBA	The AU-B0000 AMBA AHB Bus provides the muxes that implement the AMBA AHB Bus as described in the "AMBA Specification 2.0". The read and write data widths are user configurable to either 32 bits or 64 bits.
2	Ethernet 10/100 MAC Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Networking 〉Protocol Layer 〉Ethernet	The SSN8006 is an Ethernet 10/100mb/s Media Access Controller. It performs the IEEE 802.3 recommended service specification for Media Access Control.
3	Flash Controller Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Peripheral Core 〉Controller 〉Memory Controller	The AU-M3000 Flash Controller Core is a versatile NAND/NOR flash controller that supports various types of NAND and NOR flash chips from several manufacturers.
4	64 Bit PCI Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Bus Interface 〉Peripheral Bus Interface 〉PCI (Peripheral Controller Interface)	The SSP8064 PCI Core provides 64 bit PCI master and slave functionality. It is a 33/66MHz PCI core in ASIC technologies. It contains the standard PCI configuration registers including three base address registers.
5	32 Bit, Tiny Low Power Processor Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Processor & Micro-controller 〉Microprocessor 〉RISC 32-Bit	The AU-C01XX 32 Bit Tiny, Low Power Processor Cores are a family of small, low power 32 bit processor cores targeted at embedded controller, wireless, and other portable applications.
6	Processor Memory and Bus Interface Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Bus Interface	The AU-S1000 Processor Memory and Bus Interface Core provides system interfaces for Aurora VLSI processors including the AU-C01XX Processor Core family, AU-J1XXX Java Core family, and AU-J2XXX Java Core family.
7	SDRAM Controller Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Peripheral Core 〉Controller 〉Memory Controller	The AU-M2000 SDRAM Controller Core is a pipelined, high performance SDRAM controller. The SDRAM data bus width is user configurable to 32 or 64 bits. The SDRAM Controller supports SDRAM memory systems from 4 Mbytes to 4 Gbytes.
8	USB 2.0 Device Core(Soft IP / Verilog)	Aurora VLSI, Inc.(www.auroravlsi.com)	Bus Interface 〉Serial Bus Interface 〉USB (Universal Serial Bus)	The SSU7320 USB 2.0 Device Core provides USB 2.0 Device functionality. It includes the required endpoints plus eight bulk/iso transfer endpoints.
9	UART(Soft IP / Verilog)	KAIST(www.kaist.ac.kr)	Peripheral Core	Simple UART (Universal asynchronous receiver transmitter) core
10	LCD controller(Soft IP / Verilog)	KAIST(www.kaist.ac.kr)	Processor & Micro-controller	LCD controller for SAMSUNG LTS350Q1-PE2 LCD module
11	SafeXcel IP - Packet Engine(Soft IP / Verilog)	SafeNet, Inc.(www.safenet-inc.com)	Networking	High-performance, highly integrated Packet Engine, supporting cryptographic algorithms and protocol related operations.
12	DLL(Hard IP / GDS II)	MOSAID Technologies Incorporated(www.mosaid.com)	Analog & Mixed Signal 〉PLL/DLL	MOSAID Delay Locked Loops (DLLs) provide the ideal solution for high-speed interface timing, multi-phase clocking strategies, and clock signal restoration. MOSAID DLLs can be combined with MOSAID I/O libraries for a complete I/O solution.
13	Special Purpose HSTL Library(Hard IP / GDS II)	MOSAID Technologies Incorporated(www.mosaid.com)	Physical Library 〉I/O 〉Connectivity I/O	MOSAID offers complete I/O libraries for HSTL (Class I and II) for interfacing to QDR SRAMs. Libraries include all required buffer, spacer/corner, power and ground cells.
14	QDR/QDR2 SRAM Memory Controller(Soft IP, Hard IP / Verilog, GDS II)	MOSAID Technologies Incorporated(www.mosaid.com)	Peripheral Core 〉Controller 〉Memory Controller	The MOSAID QDR/QDR2 SRAM controller is offered for ASICs, ASSPs and SOC applications requiring controller logic to access industry standard QDR and QDR2 SRAMs.
15	CI7600#g - Wireless LAN 0.18um Platform(Hard IP / GDS II)	Chipidea Microelectronica SA(www.chipidea.com)	Platform IP 〉Networking & Communication	- Dual Voltage 3.3V±10% and 1.8V±10% supply operation - 10-bit 80MS/s IQADC (scalable to 40 MS/s) - Internal Bias and Reference / Analog loop-back modes
16	CI7129ca - 3-Channel Analog Video Processor(Hard IP / GDS II)	Chipidea Microelectronica SA(www.chipidea.com)	Analog & Mixed Signal 〉Coder/Decoder(CODEC)	- Analog Front-End with 3-channel for CVBS, S-Video (Y/C) and component video (YPbPr) - 27 MHz Conversion Rate - Single-ended input with fully differential processing
17	CI7613tg - WLAN baseband AFE (802.11abg) with PLL and voltage regulator(Hard IP / GDS II)	Chipidea Microelectronica SA(www.chipidea.com)	Wireless Communications 〉802.11	TSMC 0.18 um CMOS generic process. / Dual Voltage 3.3V±10% and 1.8V±10% supply operation. / 10-bit 40MHz IQADC, with two selectable inputs
18	CI7713kg - 2 Channel Video Analog Front End(Hard IP / GDS II)	Chipidea Microelectronica SA(www.chipidea.com)	Analog & Mixed Signal	2-Channel Video AFE, 3.3V, w/ DAC Clamp, 2-bit PGA and 10-bit 27 MHz ADC / 0.18um CMOS technology - 1P5M / Programmable Gain Amplifier (0.5, 1, 2 and 4) / 10-bit 27 MHz ADC / Single-ended input with fully differential processing
19	CI4018ea - 12.5 kHz, I/Q Tx Interface for PMR(Hard IP / GDSII)	Chipidea Microelectronica SA(www.chipidea.com)	Wireless Communications 〉Others	2.7 V to 3.6 V single supply operation / 12.5 kHz signal bandwidth / 10-bit resolution / Input sampling of 144 kHz / Out of band noise energy: -90 dBc/25 kHz / Linear phase response in a 12.5 kHz bandwidth
20	CI12295ug - USB2.0 OTG LS-FS-HS 3.3/1.8 UTMI+(Hard IP / GDSII)	Chipidea Microelectronica SA(www.chipidea.com)	Bus Interface 〉Serial Bus Interface 〉USB (Universal Serial Bus)	Complete PHY for USB2.0 On-The-Go / UTMI+ specification compliant / Supports 480Mbps "High Speed"(HS), 12Mbps "Full Speed"(FS) and 1.5Mbps "Low Speed"(LS) serial data transmission / USB2.0 Integration in HOST, DEVICE and Dual Role Device applications
21	PS/2 Keyboard interface(Soft IP / VHDL)	Handong Global University(www.han.ac.kr)	Peripheral Core	This core provide the PS/2 Keyboard interface logic. It converts the PS2 data stream from keyboard into corresponding character code (ASCII). It can handle the shift key. But, it cannot handle control key and ALT key properly.

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22	H.264 Decoder (Soft IP / Verilog, C/C++)	PixSil Technology (www.pixsiltech.com)	Digital Signal Processing 〉 Video Encoder/Decoder	PixSil Technology's PXL-ID264B video decoder is a highly integrated application specific core for up to 4 Mbps video decode. It is ideal for wireless applications that require real-time video decode in a power and area efficient solution.
23	H.264 Variable Length Coding (Soft IP / Verilog, C/C++)	PixSil Technology (www.pixsiltech.com)	Digital Signal Processing 〉 Video Encoder/Decoder	One of the key IP blocks in PixSil Technology's H.264 solution is VLC(Variable Length Coding). It is a reversible procedure for entropy coding that assigns shorter bit strings to symbols expected to be more frequent and longer bit strings to symbols, expected to be less frequent.
24	Variable-clock NTSC/PAL Video Encoder for camera applications(Soft IP / Verilog)	Dong-a University(www.donga.ac.kr)	Digital Signal Processing	* Convert Component video signals to Composite Video signal. * Clock Required among 19.06993 or 18.7375 or 28.63636 or 28.375MHz * Support output mode in NTSC-M/J/4.43, PAL-B/D/G/H/I/M/N/ combination N
25	NTSC/PAL/SECAM Video Encoder with power management(Soft IP / Verilog)	Dong-a University(www.donga.ac.kr)	Digital Signal Processing	* Convert Component video signals to Composite Video signal. * Support output signal in NTSC-M/J/4.43, PAL-B/D/G/H/I/M/N/combination N, SECAM-B/D/G/K/K1/L * Support input signal in ITU-R BT.601 4:2:2 or ITU-R BT.656
26	UART - Universal Asynchronous Receiver/Transmitter Core(Soft IP / Verilog)	Silicon Interfaces (www.siliconinterfaces.com)	Peripheral Core 〉 Receiver / Transmitter 〉 Asynchronous Communication	The SI40U550 IP core is a Universal Asynchronous Receiver Transmitter fully compatible with the de-facto standard 16550 UART. The SI40U550 core performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the host .
27	8051 - Microcontroller(Soft IP / Verilog)	Silicon Interfaces (www.siliconinterfaces.com)	Processor & Micro-controller 〉 Microcontroller	The SI80MC51 is an Intel microcontroller compatible, which is a true computer on chip. The product incorporates all of the features found in a microprocessor CPU: ALU, Program Counter, Stack Pointer and Registers.
28	8530 - Serial Communication Controller (Soft IP / VHDL)	Silicon Interfaces (www.siliconinterfaces.com)	Data Transmission	The SI85SCC30 SCC is a dual channel, multiprotocol data communications peripheral. It supports virtually any serial data transfer application with important functions like baud rate generator, digital phase locked loop on the cell, it makes a self contained controller.
29	Bluetooth - BaseBand Controller (Soft IP / Verilog)	Silicon Interfaces (www.siliconinterfaces.com)	Wireless Communications 〉 Bluetooth	The SI23BTB11 Bluetooth Baseband Controller implements the baseband and host controller interface (HCI) of the Bluetooth protocol and is specifically designed to meet the immediate market needs for low-power Bluetooth applications.
30	USB2.0 - Function Controller (Hard IP / Verilog)	Silicon Interfaces (www.siliconinterfaces.com)	Bus Interface 〉 Serial Bus Interface 〉 USB (Universal Serial Bus)	The SI16USB20 is a USB Function controller core designed as per USB2.0 revision of USB standards. This core provides 480Mb/s high speed USB interface. It autonomously handles the USB transactions and data transfers, thus bridging the USB interface to an easy read/write parallel interface.
31	Rapid IO - Physical Layer Interface Core (Soft IP / Verilog)	Silicon Interfaces (www.siliconinterfaces.com)	Bus Interface	This high performance low pin-count packet switched system level interconnect provides highly reliable error handling scheme whilst transferring packets between processing elements via the RapidIO Fabric.
32	SafeXcel IP - Public Key Accelerators (Soft IP / Verilog)	SafeNet, Inc. (www.safenet-inc.com)	Software	Designed for full scalability and an optimal performance over gate count ratio, SafeXcel IP Public Key Accelerators address the unique needs of semiconductor OEMs and provide a reliable and cost-effective IP solution that is easy to integrate into SoC designs.
33	SafeXcel IP - ARC4 Accelerators (Hard IP / Verilog)	SafeNet, Inc. (www.safenet-inc.com)	Bus Interface	Designed for fast integration, low gate count, and maximum performance, the SafeXcel IP ARC4 Accelerators address the unique needs of semiconductor OEMs, and provide a reliable and cost-effective silicon IP solution that is easy to integrate into SoC designs.
34	Current Limiter Reference with Enable (SC1320)(Hard IP / GDS II, Spice)	Simplechips Technology Inc. (www.simplechips.com)	Analog & Mixed Signal	A temperature-compensated, unipolar current limiter with metal programmable taps for current limits from 2 to 26 mA in 2 mA steps. Works from 5 V to 250 V AC/DC with 50/60 Hz rejection and bandwidth to 250 kHz. Enable pin can be used for PWM (digital input 3 - 5 V) or analog control.
35	CI2418tg - General Purpose LDO (Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal 〉 Others	0.18um CMOS, 4 Metals / Supply Voltage 3.0 V - 3.6 V / Output Voltages: 2.8 V - 3.4 V / Drop Out Voltage 200 mV / Output Regulation +/- 2.5% (excluding precision on reference voltage
36	CI2344tg - Charge Pump(Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal 〉 Regulator	2.5V Input Voltage 3.26V Output Voltage 10uA Average Output Current Charge Pump - 2.5 V supply operation (- 4% +16%) / 3.26 V output voltage (+/- 7.5%) / 10 uA output current
37	CI2189ca - Fan Driver and Control (Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal 〉 Others	- 3.3 V +/- 10% supply operation / 8 bit DAC to control reference voltage / Output charge pump with 30mA driver / 50 kHz typical charge pump switching frequency
38	SocEye - On Chip Monitoring System(Soft IP, Firm IP, Software IP / VHDL, Verilog, EDIF)	RealFast Intellectual Property (www.realfast.se)	Verification Component	The SocEye is a hardware based black box monitoring system, for System-on-Chip. It differs from traditional monitoring system since both hardware and software events could be monitored using the same device.
39	CI10072ka - 1.75 GHz, Frequency Synthesizer(Hard IP / GDS II)	Chipidea Microelectronica SA (www.chipidea.com)	Analog & Mixed Signal 〉 RF Module	VCO without External Components / Programmable Divider / RF Output Frequency: 1.75 GHz / Low Phase Noise: -116 dBc/Hz @ 1.152 MHz / 132 dBc/Hz @ 2.88 MHz
40	CI10069ka - 1.9 GHz, LNA with Internal Matching(Hard IP / GDS II)	Chipidea Microelectronica SA(www.chipidea.com)	Analog & Mixed Signal 〉 RF Module	RF Operation Frequency: 1.9 GHz / Low System Noise Figure: below 2dB / High Gain: 18 dB / High Linearity: 4.5 dBm IIP3 / Power Dissipation: 36 mW @ 3.3 V / Voltage Supply: 2.7 V - 3.3 V