SIPAC

No.	IP Name (Type/Format)	Seller	Category	Description
1	Tiny AES Core (Firm IP/Verilog, VHDL)	Elliptic Semiconductor Inc. (www.ellipticsemi.com)	Data Transmission	· Throughput up to 40 Mbps, 32 bit data and control bus interface · Area: 8,000 ASIC gates for encrypt/decrypt, key expansion and interface logic · Core verified through NIST FIPS vectors ensure complete standards compliance
2	Design of Quadrature CMOS VCO using Source Degenration Resistor (Hard IP/GDSII)	University of Seoul (www.uos.ac.kr)	Analog & Mixed Signal 〉 Oscillator	A new schematic of quadrature voltage controlled oscillator is designed and fabricated in standard CMOS technology. This design has ehanced linearity at the cost of the gain and phase noise by the using source degeneration resistor.
3	Low-power 64-point FFT/IFFT processor core (FFT64p) (Soft IP/Verilog)	Kumoh National Institute of Technology (www.kumoh.ac.kr)	Wireless Communications 〉 802.11	The FFT64p core is a low-power 64-point FFT/IFFT processor, which is an essential block in OFDM-based wireless LAN modems. The radix-2/4/8 DIF (Decimation-In-Frequency) FFT algorithm is implemented using R2SDF (Radix-2 Single-path Delay Feedback) structure.
4	Half-VDD Generator (Hard IP/GDSII)	Changwon National University (www.changwon.ac.kr)	Memory Element 〉 Asynchronous DRAM	Gate voltage of pull-up and pull-down transistor is swung with CMOS Level in novel proposed circuit. It is proposed the pull-up current is proportioned (VDD-|VTP|)2 using PMOS pull-up transistor and the pull-down current is proportioned (VDD-VTN)2 using NMOS pull-down transistor.
5	Voltage-Down Converter (Hard IP/GDSII)	Changwon National University (www.changwon.ac.kr)	Memory Element 〉 Asynchronous DRAM	It shows the block diagram of voltage-down converter which perform a conversion of VDD into VINT to maintain the reliability of memory device and reduce power consumption. The voltage-down converter is composed of Reference Voltage Generator (Vref), Voltage-Up Converter (VL) and VINT Driver.
6	Back-Bias Voltage Generator (Hard IP/GDSII)	Changwon National University (www.changwon.ac.kr)	Memory Element 〉 Asynchronous DRAM	Negative-voltage word-line driving method is proposed to improve the refresh time problem caused by storage charge decreased under 1.5v. VBB generator is composed of VBB Level Detector, Ring Oscillator and Charge Pump.
7	VPP Generator for DRAMs (Hard IP/GDSII)	Changwon National University (www.changwon.ac.kr)	Memory Element 〉 Asynchronous DRAM	Low power DRAM is essential to maintain reliability of minimized semiconductor and reduce power consumption of mobile DRAM of large capacity and high speed. In addition to DRAM chip, VPP(boosted voltage)generator is used for removing Vtn(threshold voltage) loss of NMOS in DRAM cell and peripheral circuit.
8	VPP Generator for FLASH Memory (Hard IP/GDSII)	Changwon National University (www.changwon.ac.kr)	Memory Element 〉 Flash Memory	Block Diagram of the VPP generator for flash memory is composed of Reference Voltage Generator, Voltage-Up Converter, VPP Level Detector, Ring Oscillator, VPP Control Logic and Charge Pump.
9	ISP (Soft IP/Verilog)	LogicMeca Co., Ltd (www.logicmeca.co.kr)	Digital Signal Processing	This ISP is the image signal processor for Digital camera, mobile camera. This processes the input signalfrom CCD/CMOS Imge sensors to digital camera fuction like Interploation, Gamma Correction,AE, AWB Auto Focus.
10	JPEG CODEC (Soft IP/Verilog)	LogicMeca Co., Ltd (www.logicmeca.co.kr)	Data Transmission 〉 Compression/Decompression 〉 Video	This JPEG CODEC supports standard JPEG compression for capturing images.The JPEG algorithms uses DCT and VLC. JPEG size is not fixed for the same input image size.
11	Compact Flash Interface (Soft IP, Hard IP/Verilog)	LogicMeca Co., Ltd (www.logicmeca.co.kr)	Peripheral Core 〉 Controller 〉 Memory Controller	CFI is the camera controller for handheld information or comunication to implement camera function easily. It reads image data from sensor and ouput through standard CF(compact flash) interface.
12	Victorus DSP 8-PE core (Soft IP/Verilog)	InterQoS Systems Ltd. (www.interqos.com)	Digital Signal Processing	Low-cost high-performance DSP architecture and the assocaited optimization software-Issue up to 8 instruections per cycle, 4 instructure on average
13	ADC8b220M : 8b 220MS/s 230mW 0.25um CMOS ADC (Hard IP/Verilog, GDS II, Spice)	Sogang University (www.sogang.ac.kr)	Analog & Mixed Signal 〉 Converter 〉 ADC	This work proposes an 8b 220 MS/s 230 mW 3-stage 0.25um CMOS ADC with on-chip filters for temperature- and supply-insensitive voltage references. The proposed RC low-pass filters reduce reference settling time at heavy R&C loads and improve switching noise performance without conventional off-chip bypass capacitors.
14	ADC8b240M : 8b 240MS/s 104mW 0.18um CMOS ADC (Hard IP/Verilog, GDS II, Spice)	Sogang University (www.sogang.ac.kr)	Analog & Mixed Signal 〉 Converter 〉 ADC	This work describes a two-step pipelined 8b 240 MS/s 0.18 um CMOS ADC as one of embedded cells for high-performance displays requiring low-noise on-chip references and dual-mode inputs with the specifications of limited pins, low power, and small size at high speed.
15	IEEE802.11a BaseBand Codec (Soft IP /VHDL)	Chungbuk National University (www.chungbuk.ac.kr)	Wireless Communications	This IP is designed for a codec which is suited to the standard of IEEE802.11a wireless LAN. The IP contains plcp, scrambler, convolution encoder, interleaver and symmetric blocks of theirs.

2005년 2월부터 4월 초까지 33개의 IP가 SIPAC에 새로 등록되었습니다. (Total : 1392개, 2005년 4월 6일 기준)
SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다.

No.	IP Name (Type/Format)	Seller	Category	Description
16	IEEE802.11a Baseband Modem (Soft IP/VHDL)	Chungbuk National University (www.chungbuk.ac.kr)	Wireless Communications 〉 802.11	This IP is designed for a OFDM modem which is suited to the standard of IEEE802.11a wireless LAN. The IP contains mapper, FFT, IFFT, symbol wave shaping filter, clock recovery and equalizer.
17	IEEE802.11a BaseBand Processor (Soft IP/VHDL)	Chungbuk National University (www.chungbuk.ac.kr)	Wireless Communications 〉 802.11	Code rate : R=1/2(2/3, 3/4 using Puncturing method)/Constraint Length K=7/Generation Polynomial : (G0=133,G1=177)_8/Data input : 4-bit soft-input/Trace-back length : 64 symbols(Used RAM)/Maximum data transmit rate : 54Mbps(Follow the IEEE 802.11a)
18	UART-LIN (Soft IP/Verilog)	Aurelia Microelettronica (www.aurelia-micro.it)	Bus Interface	Programmable device able to transmit and receive using UART (Universal Asynchronous Receiver Transmitter) protocol or LIN (Local Interconnect Network) protocol and with 8051 CISC processor interface
19	5GHz RF RX front-end module (Hard IP/GDS II)	Information and Communications University (http://www.icu.ac.kr)	Analog & Mixed Signal	RF RX front-end module including low noise amplifier and down frequency converter for 5GHz WLAN
20	5GHz WLAN RF TX front-end module (Hard IP/GDS II)	Information and Communications University (http://www.icu.ac.kr)	Analog & Mixed Signal	Driving amplifier and up converter for 5GHz WLAN
21	Variabe Gain Amplifier (Hard IP/GDS II)	Information and Communications University (http://www.icu.ac.kr)	Analog & Mixed Signal	Variable gain amplifier in Receiver for 5GHz WLAN
22	A Current reused differential VCO (Hard IP/GDS II)	Information and Communications University (http://www.icu.ac.kr)	Analog & Mixed Signal	Differential VCO to reduce current consumption.
23	A current reused quadrature VCO (Hard IP/GDS II)	Information and Communications University (http://www.icu.ac.kr)	Analog & Mixed Signal	Quadrature VCO to reduce current consumption
24	TL6108FS-1.2GHz/250MHz Dual Frequency Synthesizer (Hard IP/GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 Clock Synthesizer	The TL6108FS of full CMOS monolithic, dual frequency synthesizer is to be used as a local oscillator for RF and IF of a dual conversion transceiver. It is fabricated using 0.25mm standard CMOS process.
25	TL6118FS-1.8GHz/500MHz Dual Frequency Synthesizer (Hard IP/GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 Clock Synthesizer	TL6118FS contains dual modulus prescalers. A 64/65 or a 128/129 prescaler can be selected for RF synthesizer and a 8/9 or 16/17 prescaler can be selected for IF synthesizer.
26	TL6301PL-25~230MHz PLL (Hard IP/GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 PLL/DLL	TL6301PL is capable of generating any frequency from 25MHz to 230MHz by writing the appropriate values to the PLL Dividers. This IP can use the external loop filter to obtain better performance and wider operating range of reference clock and output clock frequency.
27	TL6302PL-25~210MHz PLL (Hard IP/GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 PLL/DLL	TL6302PL is capable of generating any frequency from 25MHz to 210MHz by writing the appropriate values to the PLL Dividers. this IP can use the external loop filter to obtain better performance and wider operating range of reference clock and output clock frequency.
28	TL6303PL_A-6~150MHz PLL (Hard IP/GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 PLL/DLL	TL6303PL-A is capable of generating any frequency from 6MHz to 150MHz by writing the appropriate values to the PLL Dividers. Although an on-chip loop filter is included, this IP can use the external loop filter to obtain better performance and wider operating range of reference clock and output clock frequency
29	TL6303PL_B-6~150MHz PLL (Hard IP/GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 PLL/DLL	TL6303PL-B has a duty correcting by-3-divider, so duty corrected 1/3 frequency output is provided. TL6303PL-B is silicon proven and test sample and board is ready.
30	Cardbus Interface Controller (Soft IP/VHDL)	Konkuk University (http://www.konkuk.ac.kr)	Bus Interface	PCMCIA type-II cardbus interface controller
31	SafeXcel IP-MD5/SHA-1/SHA-256 Accelerators (Soft IP/Verilog)	SafeNet, Inc (http://www.safenet-inc.com)	Networking	Silicon-proven IP for acceleration of MD5, SHA-1, and SHA-256 hash operation. Multiple configurations are available, where any combination of these hash algorithms can be selected. Layered design, with a wide bus core and a 32-bit register interface.
32	iinChip W3100A (Hardwired TCP/IP) (Soft IP, Firm IP/VHDL, EDIF)	WIZnet (http://www.wiznet.co.kr)	Networking 〉 Protocol Layer 〉 Ethernet	iinChip W3100A Core is a unique silicon-proven hardwired TCP/IP protocol stack requiring minimal host interaction by processor TCP Offload technology.
33	DR8051-High Performance 8-bit Micro-controller (Soft IP, Firm IP/VHDL, Verilog, EDIF)	Digital Core Design (http://www.dcd.com.pl)	Processor & Micro-controller 〉 Microcontroller 〉 RISC 8-Bit	DR8051 is a high performance, area optimized soft core of a single-chip 8-bit embedded controller dedicated for operation with fast (typically on-chip) and slow (off-chip) memories.