An InGaP/GaAs HBT Monolithic VCDRO with Wide Tuning Range and Low Phase Noise

Jae-Young Lee · Bhanu Shrestha · Jeiyoung Lee · Gary P. Kennedy · Nam-Young Kim

Abstract

The InGaP/GaAs hetero-junction bipolar transistor(HBT) monolithic voltage-controlled dielectric resonator oscillator(VCDRO) is first demonstrated for a Ku-band low noise block down-converter(LNB) system. The on-chip voltage control oscillator core employing base-collector(B-C) junction diodes is proposed for simpler frequency tuning and easy fabrication instead of the general off-chip varactor diodes. The fabricated VCDRO achieves a high output power of 6.45 to 5.31 dBm and a wide frequency tuning range of 165 MHz(1.53 %) with a low phase noise of below −95 dBc/Hz at 100 kHz offset and −115 dBc/Hz at 1 MHz offset. Also, the InGaP/GaAs HBT monolithic DRO with the same topology as the proposed VCDRO is fabricated to verify that the intrinsic low $1/f$ noise of the HBT and the high Q of the DR contribute to the low phase noise performance. The fabricated DRO exhibits an output power of 1.33 dBm, and an extremely low phase noise of −109 dBc/Hz at 100 kHz and −131 dBc/Hz at 1 MHz offset from the 10.75 GHz oscillation frequency.

Key words : Hetero-Junction Bipolar Transistor(HBT), InGaP/GaAs, Voltage-Controlled Dielectric Resonator Oscillator(VCDRO), Low Noise Block Down-Converter(LNB), Phase Noise.

Ⅰ. Introduction

With the rapid growth in X- to Ku-band satellite communication technologies, there is a great demand for improved VCO performance in terms of phase noise, cost, size, bandwidth, tuning linearity, and efficiency. Because it affects the dynamic range, selectivity, and sensitivity of a receiver, the phase noise is a critical analysis parameter[1]. Due to the intrinsic low 1/f noise performance, HBT technology is more suitable for low phase noise performance than high efficiency applications. As HBTs have a higher output power density compared to GaAs FETs as power amplifiers[2], they can also generate a high oscillation output power[3].

Also, DROs are attractive and stable microwave sources because of their high quality factor(Q), low phase noise, good output power and high stability versus temperature[4]. DROs exhibit excellent frequency stability with temperature, but their applications in the wide range of microwave systems have been limited by the lack of sufficient electrical tuning capability for phase locking. Therefore, the possibility of electrically tuning the center frequency, i.e., frequency modulation(FM), is very important.

This problem has been solved in a few different ways: by tuning the voltage of varactor diodes or PIN diodes, whose electrical networks influence the DR. An alternative solution utilizes a light source[5]. N. Popovic summarized the above methods in the circuit design and construction of various types of varactor tuned DROs[6]. However, most VCDROs are very complex and difficult to fabricate.

In this paper, a simpler frequency tuning method is proposed by implementing on-chip base-collector(B-C) junction diodes instead of using the general off-chip varactor diodes used in most VCDROs. Although the B-C junction diodes are connected in parallel, between the off- chip DR and on-chip active device, the fabricated VCDRO achieves a wide frequency tuning range with low phase noise by utilizing both the intrinsic low $1/f$ noise characteristics of the HBT and high Q of the DR. In order to verify the low phase noise performance, a DRO with the same configuration as the proposed VCDRO is fabricated, and it exhibits extremely low phase noise characteristics by excluding the B-C junction diodes.

Ⅱ. Ku-Band LNB System

The LNB is located in front of the dish and at the focal point of an antenna, and acts as a LNA. It converts the received electromagnetic signal fed from an antenna into an electrical signal, and amplifies the signal during the conversion process.

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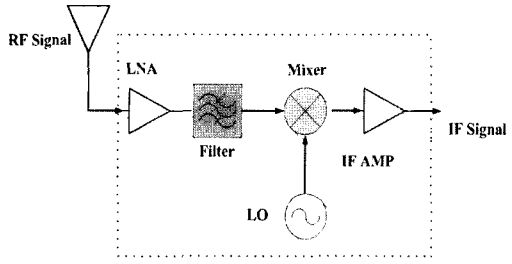


Fig. 1. Block diagram of the Ku-band LNB.

The Ku-band LNB converts the radio frequency(RF) signal of 11.7 to 12.75 GHz to a lower intermediate frequency(IF) of 950 to 2,000 MHz using the 10.75 GHz reference frequency of the X-band local oscillator. The block diagram of the Ku-band LNB is shown in Fig. 1. The typical required phase noise specification of the DRO for the Ku-band LNB system is −95 dBc/Hz at 100 kHz offset and −115 dBc/Hz at 1 MHz offset from the 10.75 GHz oscillation frequency[7].

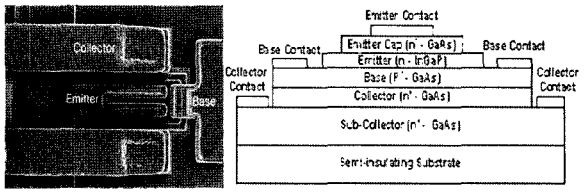
Ⅲ. Low 1/f Noise in InGaP/GaAs HBT

The monolithic VCDRO is designed using high linearity InGaP/GaAs HBT technology from Know-ledge*on Inc. in Korea. Although the GaAs HBT has higher white noise than III-V FETs, its advantages include greater speeds with relaxed lithographic dimensions, higher current per effective chip, better device matching, higher transconductance, low output conductance, and reduced trapping effects accompanied by low $1/f$ and phase noise.

Because the thermal conductivity of GaAs is lower than Silicon, the vertical bipolar inter-company(VBIC) model is used to consider the self-heating effect. The VBIC model extracts accurate large signal characteristics and improves Early effect and temperature modeling of the HBT by comparison with the existing Gummel-Poon(GP) model.

The transistors used for the on-chip oscillator core of the monolithic DRO consist of 2 emitter fingers, 2 μm emitter width, and 20 μm emitter length(HL_F2×2×20). These transistors have a β of 115, f_T of 50 GHz, and f_{max} of 80 GHz at V_{ce} of 1.5 V and an I_c of 20 mA. The microphotograph and cross section of the InGaP/GaAs HBT are illustrated in Fig. 2.

The extended InGaP ledge around the emitter periphery shown in Fig. 3 allows a well-passivated extrinsic base region and easy fabrication process. Thus, the extended InGaP passivation ledge prevents surface recombination currents and performs a significant role in reducing $1/f$ noise mainly originating from the exposed P^+-GaAs doped base region[8]. Therefore, the InGaP



(a) (b)

Fig. 2. (a) Microphotograph of InGaP/GaAs HBT with 2 emitter finger, and (b) Cross section of the HBT.

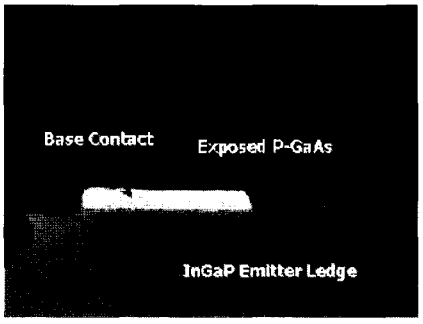


Fig. 3. Microphotograph of the extended InGaP emitter ledge.

ledge makes InGaP/GaAs HBT technology suitable for designing a low phase noise oscillator.

Ⅳ. VCDRO Design

The VCDRO as depicted in Fig. 4 is composed of an on-chip common-base(CB) negative resistance InGaP/GaAs HBT voltage-controlled oscillator core with a series inductive feedback configuration and an off-chip reflection type DR located beside a microstrip line. A series inductance($L2$) in the base of $Q1$ provides the necessary negative output resistance, and the inductor $L3$

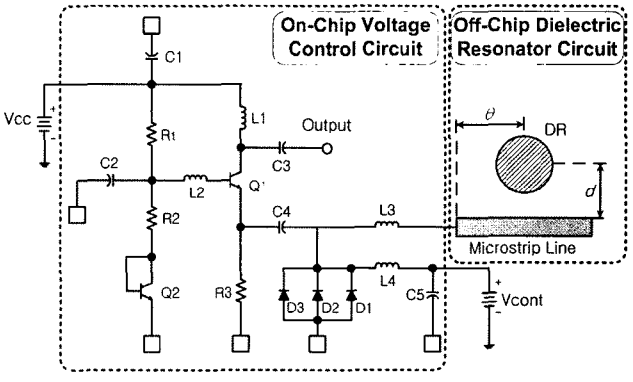


Fig. 4. Schematic of the VCDRO composed of on-chip voltage-controlled oscillator core employing B-C junction diodes and off-chip DR located beside the microstrip line.

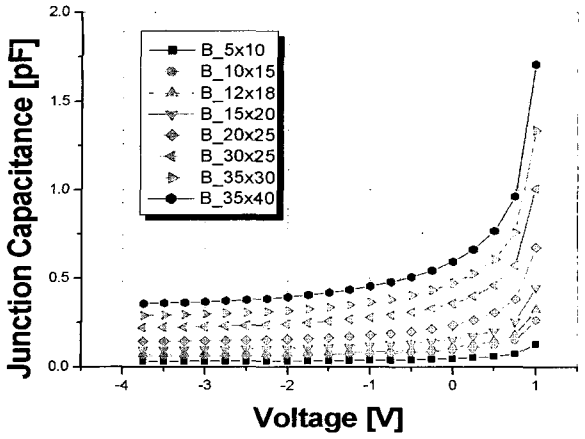


Fig. 5. Junction capacitance variation of the B-C junction diodes as a function of control voltage.

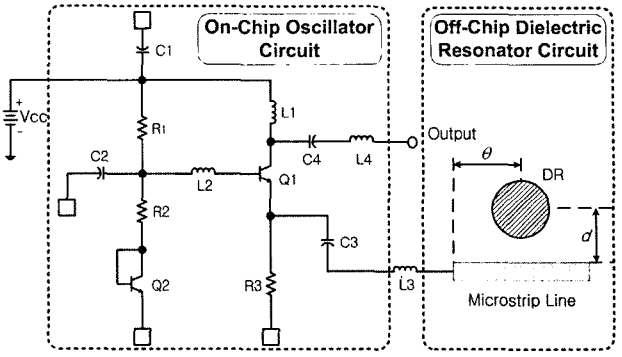


Fig. 6. Schematic of the DRO composed of on-chip oscillator core and off-chip DR circuit. The B-C junction diodes of VCDRO in Fig. 1 are excluded, and the output matching components $L4$ is added.

represents a bonding wire. Only matching components $L1$ and $C3$ are used in the collector port to avoid power losses instead of a resistive load. The base-collector connected transistor $Q2$, which is an identical device to $Q1$, maintains a fixed bias condition for the transistor $Q1$ by tracking the base-emitter voltage variation of $Q1$ with temperature.

The diodes $D1$, $D2$ and $D3$ are all the identical B-C junction diodes that consist of 12 μm base width and 18 μ m base length($B\_12\times18$), which have a junction capacitance of 0.111 pF at 0 V. They are used to tune the impedance of the input port of the series feedback CB oscillator. The junction capacitance characteristics of several B-C junction diodes as a function of the control voltage variation are shown in Fig. 5.

The phase noise of the VCDRO mainly depends on the quality of the DR and coupling structures such as varactor diodes, microstrip line and substrate. Furthermore, the use of a metal cavity to shield the DR is considered as critical for phase noise since the Q of the DR is drastically affected by the proximity of metal walls[9]. Moreover, the position of the DR relative to the microstrip line determines the stability, output power and phase noise of the oscillator. Adjusting d in Fig. 4 increases or decreases the amount of coupling between the microstrip line and the DR. Stronger coupling results in better frequency tuning. On the other hand, the Q factor as well as stability of the DR decreases and the frequency modulation(FM) noise increases[6]. The electrical length θ in Fig. 4 determines how fast and stable the build-up will occur, driving both the output power and phase noise performance[4]. In this configuration, d and θ are optimized to obtain a sufficient oscillation condition, output power and phase noise with regard to the DC blocking capacitor $C4$, bonding wire $L3$, and B-C junction diodes $D1$, $D2$ and $D3$.

Because DROs are generators of stable frequency, the center frequency is tunable within narrow limits(up to 1 percent of f_c)[6]. Therefore the structures and configurations for tuning the oscillation frequency so far were very complex and difficult to fabricate. However, in this work, employing on-chip B-C junction diodes using InGaP/GaAs HBT technology the oscillation frequency can be tuned using lumped varactor diodes. The greater the number of B-C junction diodes used, the greater the frequency tuning range obtained, but the number of the B-C junction diodes must be limited to preserve a high Q value for the off-chip DR. The optimum number of diodes satisfying the phase noise requirement of -95 dBc/Hz at 100 kHz offset and -115 dBc/Hz at 1 MHz offset is investigated by a CAD simulation using Agilent's ADS. Thus, three B-C junction diodes are used in the VCDRO presented here.

Also, the DRO based on the same configuration with the VCDRO as shown in Fig. 6 is fabricated to verify the low phase noise performance. The voltage control diodes are excluded, and the matching component $L4$ is added to the output port. The values of all components of the DRO in Fig. 6 are adjusted for the oscillation build-up because removing the control diodes changes the oscillation condition, but the off-chip DR circuit remains the same as the proposed VCDRO. The phase noise performance of VCDRO is slightly degraded by the diodes compared to the DRO.

V. Experimental Results

The die sizes of the fabricated on-chip oscillator cores of the VCDRO and DRO as depicted in Fig. 7 are 838 μm$\times$670 μm and 867 μm$\times$650 μm, respectively. The dies are attached to the gold coated teflon substrate of ε_r=2.5 by using the silver epoxy. The Q value of a

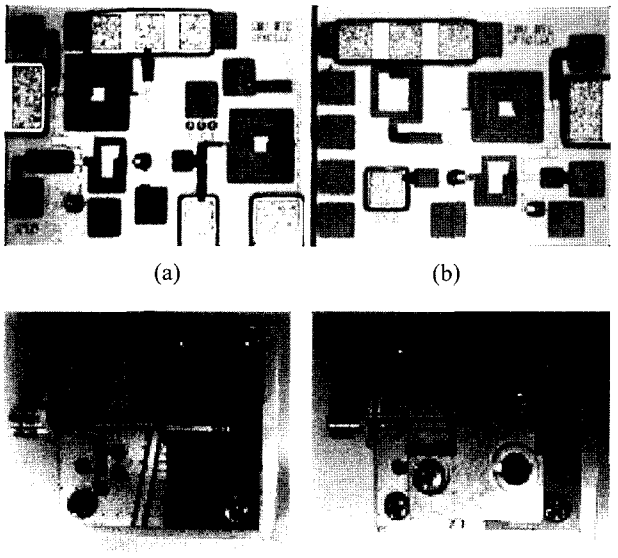


Fig. 7. Microphotographs of the fabricated dies and final VCDRO; (a) VCDRO(838 μm×670 μm), (b) DRO(867 μm×650 μm), (c)VCDRO with off-chip DR mounted on the aluminium jig, and (d) with shielding metal cavity.

DR from I-TEK Co. in Korea is 3256 at 10.75 GHz. The final VCDRO and DRO consist of an on-chip oscillator core and an off-chip DR with a shielding metal cavity, and those are mounted on the aluminum jig.

The VCDRO achieves a high output power of 6.45 to 5.31 dBm and wide frequency tuning range of 165 MHz (10.6901 to 10.8551 GHz) when the control voltage is varied from 0 to 6 V as shown in Fig. 8. Table 1 confirms that the frequency tuning range of the proposed VCDRO is the widest reported so far.

The best phase noise performance at the 10.75 GHz oscillation frequency is shown in Fig. 9. The VCDRO exhibits a low phase noise of −100.8 dBc/Hz at 100

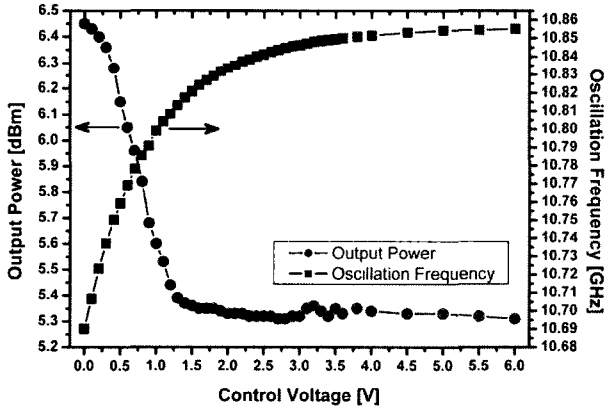


Fig. 8. Frequency tuning and output power variation of VCDRO as a function of the control voltage.

Table 1. Comparison of frequency tuning range.

No.	Device	Type	Oscillation Freq. [GHz]	Tuning Freq. [MHz]	Ref.
1	FET	Hybrid	11	11(0.1 %)	6
2	FET	Hybrid	10.5	11.2(0.11 %)	
3	FET	Hybrid	29	45(0.16 %)	
4	HJFET	MMIC	60	34(0.06 %)	
5	FET	Hybrid	10.5	28(0.27 %)	
6	FET	Hybrid	12.66	30(0.24 %)	
7	FET	Hybrid	10.5	7(0.07 %)	
8	FET	Hybrid	7.4	60(0.81 %)	
9	FET	Hybrid	16	40(0.25 %)	
10	FET	Hybrid	8	30(0.38 %)	
11	FET	Hybrid	10.4	91(0.88 %)	
12	**HBT**	**MMIC**	**10.75**	**165(1.53 %)**	**This Work**

kHz offset and −119.4 dBc/Hz at 1 MHz offset. In the case of the DRO, the extremely low phase noise of −109 dBc/Hz at 100 kHz offset and −131 dBc/Hz at 1 MHz offset is obtained. Due to the B-C junction diodes, the phase noise of VCDRO is 8.1 dB at 100 kHz offset and 11.6 dB at 1 MHz offset higher than that of the DRO. Nevertheless, the phase noise variation of VCDRO as a function of the frequency tuning is maintained below the typical required specification of −95 dBc/Hz at 100 kHz offset and −115 dBc/Hz at 1 MHz offset as shown in Fig. 10. It is clear that the intrinsic low $1/f$ noise of the InGaP/GaAs HBT and the high Q of the DR contribute to achieve the low phase noise performance. The other parameters of both DROs are summarized and compared in Table 2.

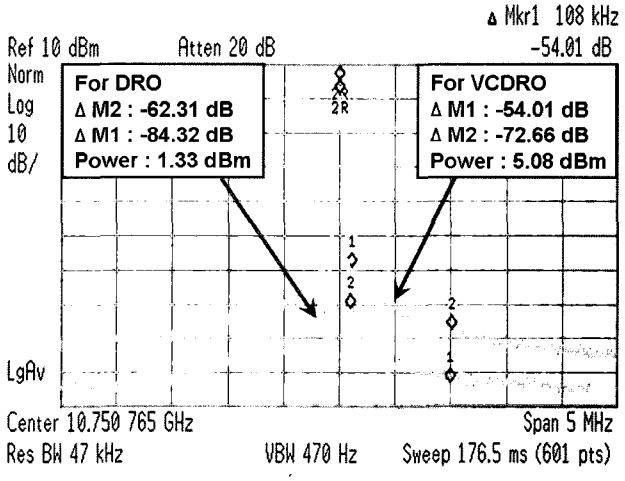


Fig. 9. Phase noise performance of both VCDRO and DRO.

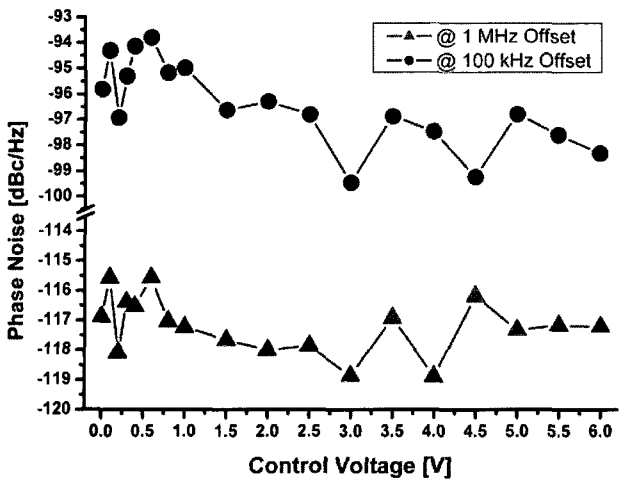


Fig. 10. Phase noise variation of VCDRO as a function of the frequency tuning.

Table 2. Summary of the measurement results.

Parameters		Units	VCDRO	DRO
Supply Voltage(Vcc)		V	3.5	3.3
Current Consumption		mA	12.8	10.9
Tuning Voltage		V	0~6	-
Oscillation Frequency		GHz	10.6901~10.8551	10.75
Frequency Tuning Range		MHz	165	-
Output Power		dBm	6.45~5.31	1.33
2nd Harmonic Suppression		dB	23.1	32
Pushing Figure($V_{cc}\pm0.5$ V)		MHz	35.7	7.17
Phase Noise	at 100 kHz offset	dBc/Hz	-100.8	-109
	at 1 MHz offset	dBc/Hz	-119.4	-131

Ⅵ. Conclusion

The InGaP/GaAs HBT monolithic VCDRO is first demonstrated here with the provision of simpler frequency tuning and easy realization method by implementing on-chip B-C junction diodes instead of general off-chip varactor diodes. The proposed VCDRO exhibits the widest electrical frequency tuning range with a sufficient low phase noise performance among the VCDROs reported. The electronic tuning capability of proposed VCDRO can be used to compensate for the frequency drift of the oscillator with temperature by programming the tuning voltage of B-C junction diodes to achieve better frequency stability and phase locking. Also, the InGaP/GaAs HBT DRO based on the same configuration with the proposed VCDRO is fabricated to verify and compare the phase noise performance. The fabricated DRO achieves an extremely low phase noise as expected.

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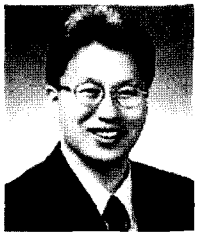

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