Printed Polymer and a-Si TFT Backplanes for Flexible Displays

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Abstract

The need for low cost, flexible, thin film transistor (TFT) display backplanes has focused attention on new processing techniques and materials. We report the development of TFT backplane technology based entirely on jet-printing, using a combination of additive and subtractive processing, to print active materials or etch masks. The technique eliminates the use of photolithography and has the potential to reduce the array manufacturing cost. The printing technique is demonstrated with both amorphous silicon and polymer semiconductor TFT arrays, and we show results of small prototype displays.

Keywords : jet-printing, TFTs, polymer semiconductor

1. Introduction

Jet-printing is an interesting patterning technique for electronic devices because it requires no physical mask, has digital control of ejection to provide drop-on-demand printing, and is also a non-contact process. The combination of additive and subtractive jet-printing, as well as excellent layer-to-layer registration, provides flexibility in the choice of materials and structures. Jet-printing has the potential to reduce display manufacturing cost and enable roll-to-roll processing. However, particularly for additive printing, new materials and processes must be developed, which need to be validated on prototype arrays. Towards this end, we describe the fabrication and characterization of printed TFT arrays on glass and flexible plastic substrates, and the performance of small jet-printed reflective displays. Other groups have reported jet-printing to deposit polymeric semiconductors for polymer light emitting diodes [1], and to print metal nanoparticles [2]. Our work on printed TFT arrays has been reported in several previous publications [3-6]. There are also several alternative printing techniques that have been applied to fabricate electronic devices, including micro-contact printing, thermal transfer, and micro-fluidics [7-9].

2. Jet-printed TFT Devices and Arrays

2.1 Printing methods

The jet printing systems developed at PARC use piezo-jet print-heads with 500-1000 independently addressable ejectors based on commercial Xerox technology, as
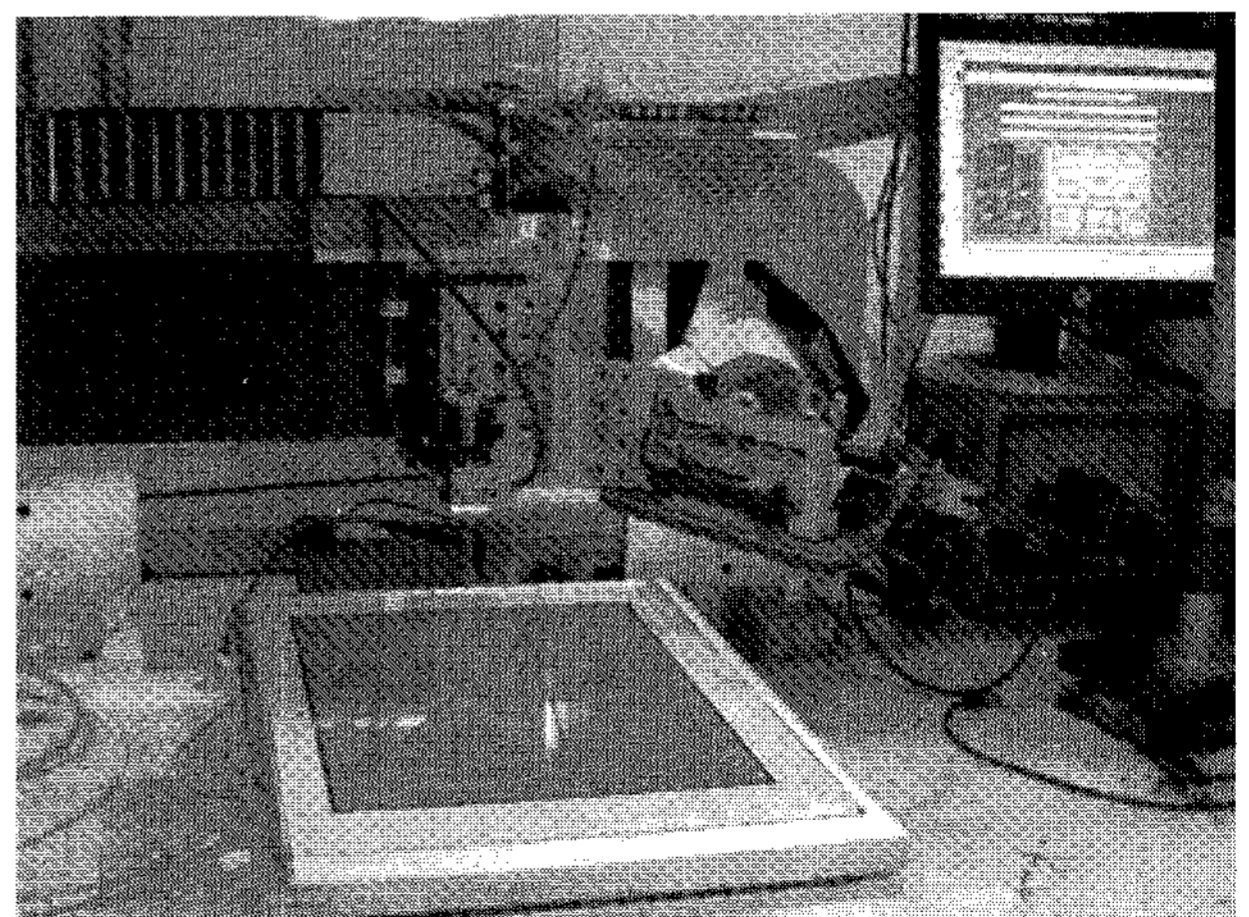
Fig. 1. Photograph of the jet-printing system, showing the print-head, the alignment camera, the 15″ substrate holder and substrate mechanical translation stage.

well as other commercial print-heads. Fig. 1 shows a photograph of one of the printing systems. The substrate is mounted on a heated stage on an x-y translation system accurate to about 1 μm. The printing system has an electronic image-capture system comprising a video camera mounted on the stage, to locate alignment marks and has software to adjust the drop ejection to provide better than 5 μm alignment from one printed layer to the next. The printing system in Fig. 1 can print an area of about 15″x15″, and the printer could be scaled to a much larger area while maintaining the same precision. A single multi-ejector print head provides printing speeds of order 100m^2/hour, depending on the complexity and coverage of the printed surface, and a system with multiple print heads could have a much larger print speed.

The main considerations for jet-printed electronic devices are the ejected drop size, which controls the minimum feature size, and the precision with which drops are placed on the surface, which controls the layer-to-layer registration and the alignment of features within a layer. At present, neither the jet-printed feature size nor the registration accuracy matches the performance of large area photolithography. However, these are not fundamental limitations and there are many opportunities to develop and improve the technology.

The print-head is typically positioned 0.5 – 1 mm above the substrate. Precise printing requires that the drops ejected from the head have accurate directionality, and the movement of the print-head or substrate along with a variation in the drop velocity also give errors in the drop position. The error, δx, in the drop position as a result of uncertainty in the drop velocity, v, the head-to-substrate spacing, s, the ejection time, t, and the jetting direction, θ, is given by,

$$\delta x = \frac{u.s}{v}\left[\frac{\delta v}{v} + \frac{\delta s}{s} + \frac{\delta t}{t}\right] + s\delta\theta \qquad (1)$$

where u is the head velocity. The terms within the brackets in eq. 1 only apply to the print direction, while the directionality deviations apply in all directions. Hence the printing precision is directional and this fact should be considered in developing the printing process and designing device structures.

A position error of 5 μm corresponds to a jetting direction error of ~0.25 degree, and the same error results

from a few percent differences in drop velocity. Commercial high performance piezo-electric print-heads can be normalized to give very uniform drop velocity by modifying the printing waveform. In addition, we can calibrate for the ejection directionality by printing a set of marks and using the computer vision system to locate the printed spot accurately.

Two methods are used to fabricate devices by jet-printing and these are illustrated in Fig. 2. With Digital Lithography, an etch mask is jet-printed and used to pattering conventionally deposited thin films (metals, dielectrics and semiconductors) [1,2]. Our technique achieves reproducible features by printing a molten wax which freezes on contact with the substrate. The advantage of printing wax is that the printed feature is controlled by the freezing of the wax on the substrate and is relatively insensitive to the surface energy of different surfaces. Hence, the wax mask technique allows patterning of arbitrary films on various substrates.
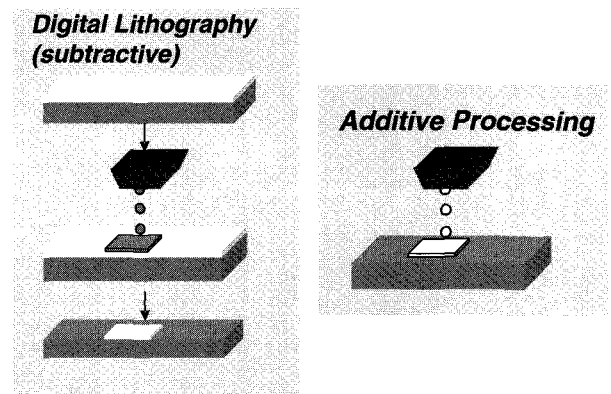

Fig. 2. Schematic illustration of the printing processes described in the paper. (Left) Digital lithography; (right) Additive printing process.
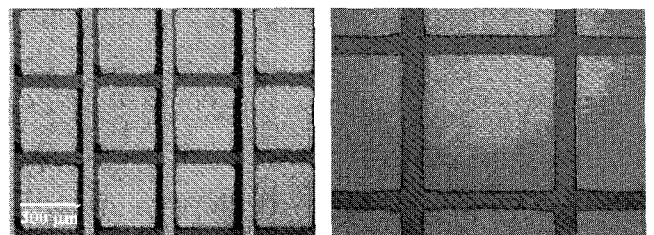

Fig. 3. (Left) Photograph of a metal film that is patterned using the printed wax mask process. (Right) Close-up of etched metal lines showing the straight edges and square intersections that can be achieved with careful digital lithography processing.

Additive printing is the direct deposition and patterning of an active material. This technique has been used by several groups for printed OLEDs, color filter, metals and polymer semiconductors [1]. Our research has focused on the printing of polymer semiconductors, as described further below [3-6].

2.2 Digital lithography of amorphous silicon on glass and flexible substrates

Fig. 3 shows an example of an etched pattern on a deposited metal thin film using a printed wax mask. The print process direction is vertical in the Fig. and it can be seen that more precise lines are printed in the process direction than perpendicular, so discussed above. The printed drops overlap partially and surface tension tends to give straight edges in the print direction. One of the design considerations in fabricating arrays is to choose the optimal print direction. Careful control of the processing conditions, including surface preparation, print speed, drop overlap, etc, allows etched metal lines that have straight edges and square intersections, as shown in Fig. 3 (right).

Using the digital lithography process, we have fabricated amorphous silicon (a-Si) TFT arrays having both the island etch and back-channel etch designs. The backchannel etch design is more suitable to digital lithography because the channel length is defined by the gap between two printed features and this can be made smaller than the printed drop size. Hence, although the printed feature size is 40 μm, we are able to make TFTs with channel lengths down to 20 μm. The minimum channel length is limited by the edge definition of the printed lines and the directional accuracy of printing, rather than by the printed feature size. Fig. 4 shows part of an a-Si TFT array fabricated using digital lithography in a 5 mask process (gate metal, source-drain metal, island, via, top
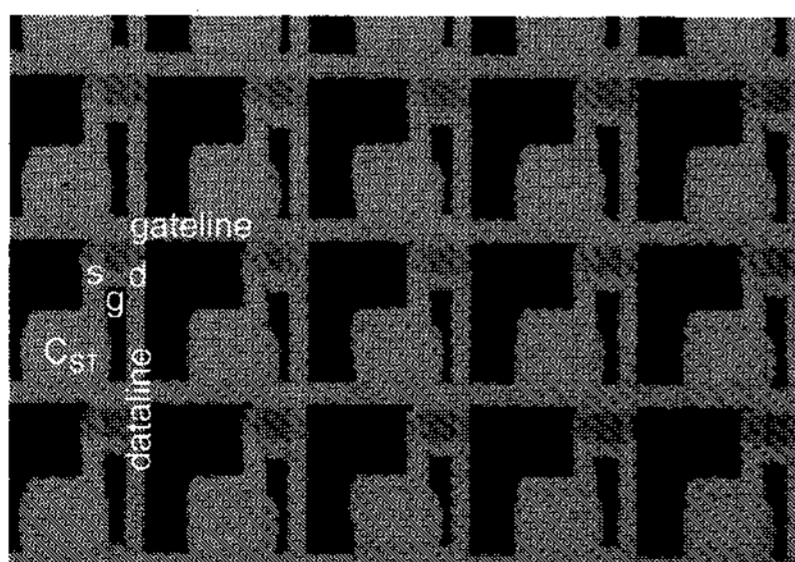
metal). The 180x180 pixel array has 75 dpi resolution. Since conventional materials are used, the TFT characteristics are essentially identical as for conventional processing.

The same digital lithography process was used to fabricate a-Si TFTs on flexible plastic substrates. We chose polyethylene naphthalene (PEN) for its good surface finish, moderately high process temperature and reasonable dimensional stability. It was first necessary to develop a low temperature process for a-Si and the gate dielectric. Devices deposited at 150C achieved a performance equivalent to the high temperature material, and we have demonstrated TFTs at 120C with only slightly degraded characteristics. A TFT array on a PEN substrate is shown in Fig. 5(a) and the TFT transfer characteristics are given in Fig. 5(b), showing that the digital lithography process is successful for TFTs on plastic substrates.

2.3 Additive printed polymer TFTs

It is desirable to reduce display manufacturing costs
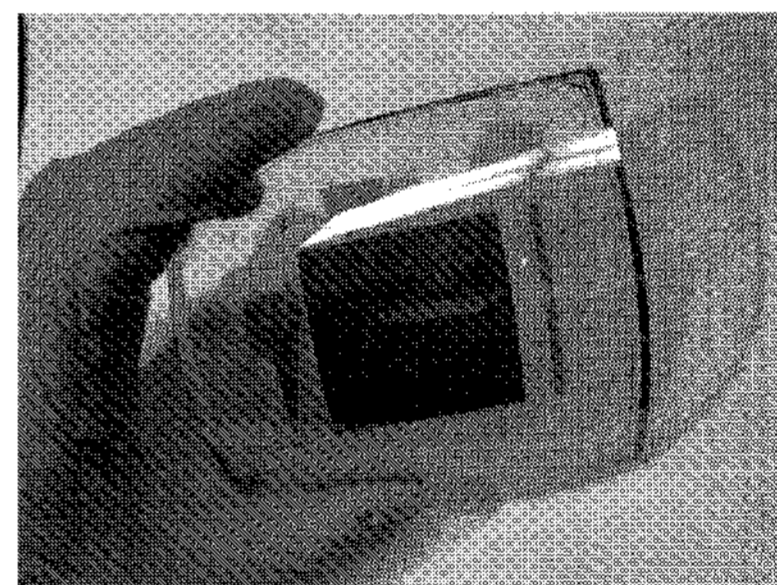
(a)
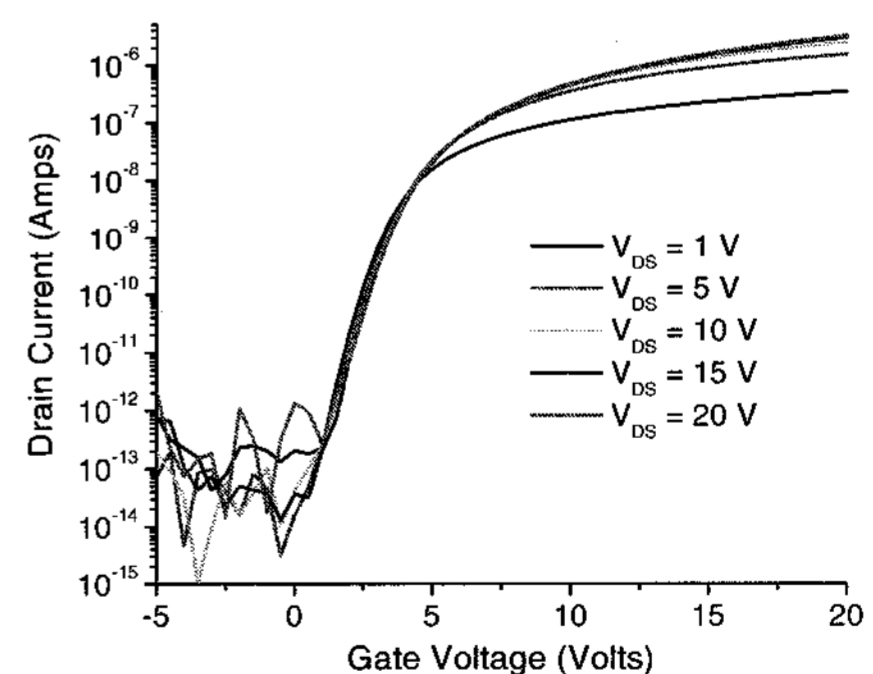
(b)

Fig. 5. (a) Photograph of a flexible printed amorphous silicon TFT array using a low temperature deposition process. (b) TFT characteristics for a-Si deposited onto flexible substrate at a process temperature of 170C.

Fig. 4. Part of an amorphous silicon TFT backplane array fabricated using digital lithography.

by minimizing the number of process steps and material usage. In an ideal additive printing process, deposition and patterning are done in a single step, and there is zero material waste. However, additive jet-printin g requires solution-based materials. Although suitable semiconductor, metal, and dielectric materials are available, they have not yet been shown to give TFT performance that meets the requirements of displays. Our research has focused on additive jet-printing of the polymer semiconductors. Specifically, we use a polythiophene polymer (PQT-12) which results in TFTs with mobility of about 0.1 cm^2/Vs [8].

The polymer structure is illustrated in Fig. 6(a). It has a polythiophene backbone with alkyl side groups to give solubility. The monomer comprises four thiophene rings and is designed to give a regioregular polymer structure, which is known to be important for achieving high mobility [10]. The polymer film is polycrystalline with a highly oriented lamella structure, as determined by x-ray diffraction and AFM imaging. Polymer TFTs are fabricated
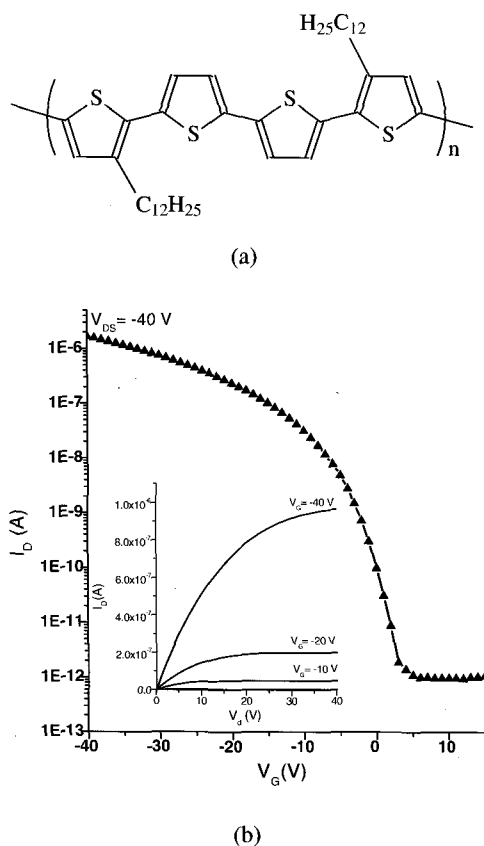
with a PECVD dielectric and a self-assembled monolayer at the surface which is belived to promote structural ordering. Devices are annealed at about 130C. Typical TFT characteristics are shown in Fig. 6(b) for polymer deposited on glass. The p-type devices turn on near zero gate voltage, and have moderate threshold voltage and high on/off ratio ($>10^6$), giving characteristics that are suitable for display applications. Jet-printed polymer devices have essentially the same performance as spin-coated films, showing that the let-printing process does not introduce any significant degradation of device performance. The TFT characteristics for devices made on flexible plastic substrates have slightly reduced mobility and a higher threshold voltage, showing that further optimization of the dielectric is required.

The printing process fabricates bottom gate TFTs with coplanar source and drain contacts. This structure is similar to conventional a-Si TFTs. It is also convenient because the metal and dielectric layers are completed before the semiconducting polymer is deposited, thus minimizing the possible degradation of the polymer from subsequent processing. Our process uses subtractive printing to pattern the metal and dielectric layers, and Fig. 7 shows part of a polymer TFT array made by this process. Additive printing of the remaining materials can be expected in the future. Alternatively the metals and dielectric layers could be patterned by conventional photolithography and only the polymer jet-printed.

There is considerable uncertainty about the environmental and bias-stress lifetime of polymer TFTs. For devices made from PQT, we observe good stability of un-

(a)

(b)

Fig. 6. (a) The monomer chemical structure for the PQT-12 semiconducting polymer. (b) Example of the transistor transfer characteristics for a bottom gate PQT-12 TFT on glass.
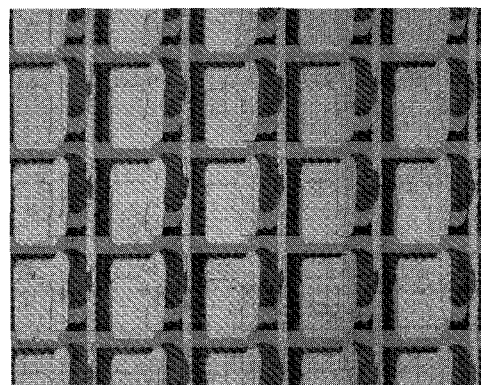

Fig. 7. Photograph of part of a 128x128 pixel TFT array on a flexible substrate with a jet-printed polymer semiconductor.
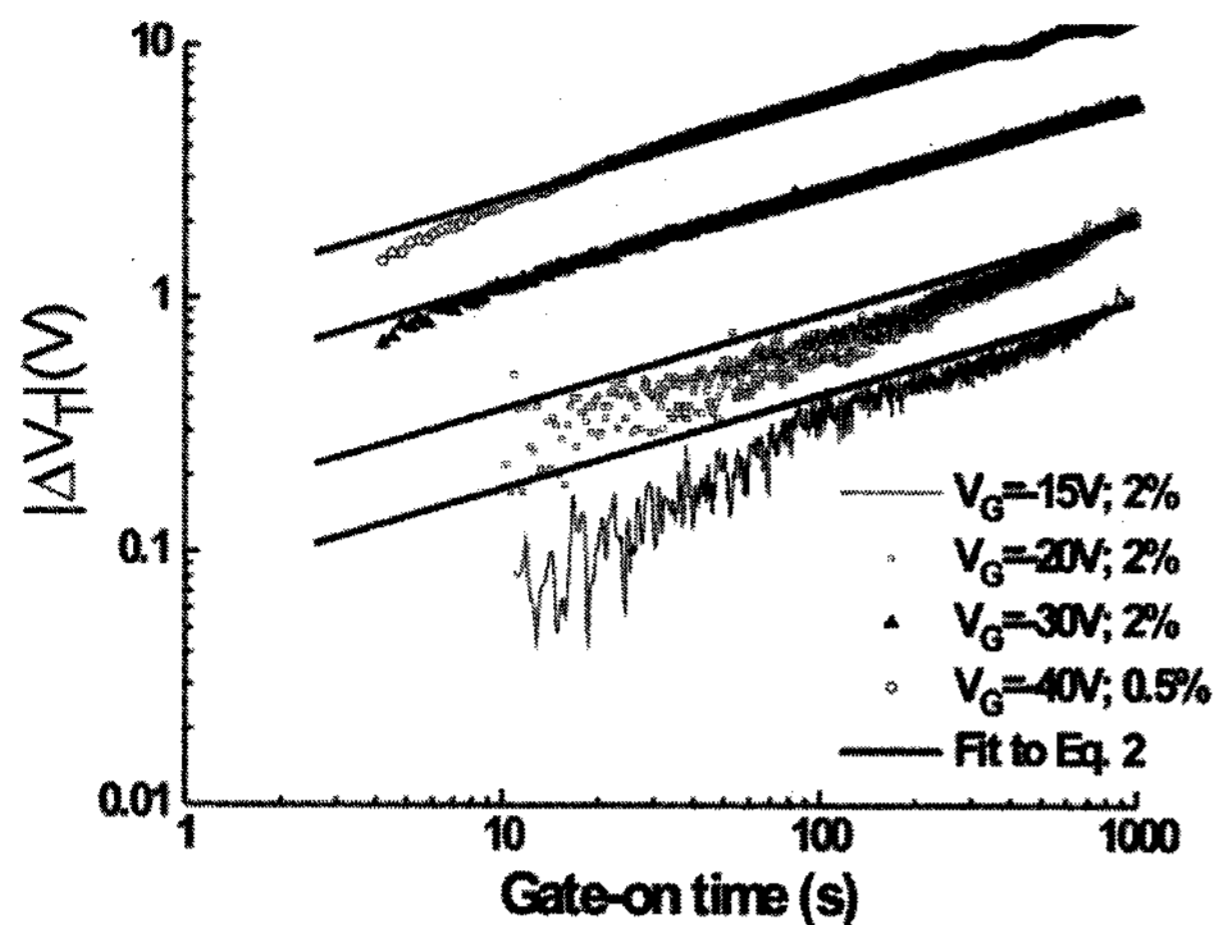
Fig. 8. Plot of the time dependence of the threshold voltage shift, as a result of bias stress of a PQT-12 TFT at different gate voltages.
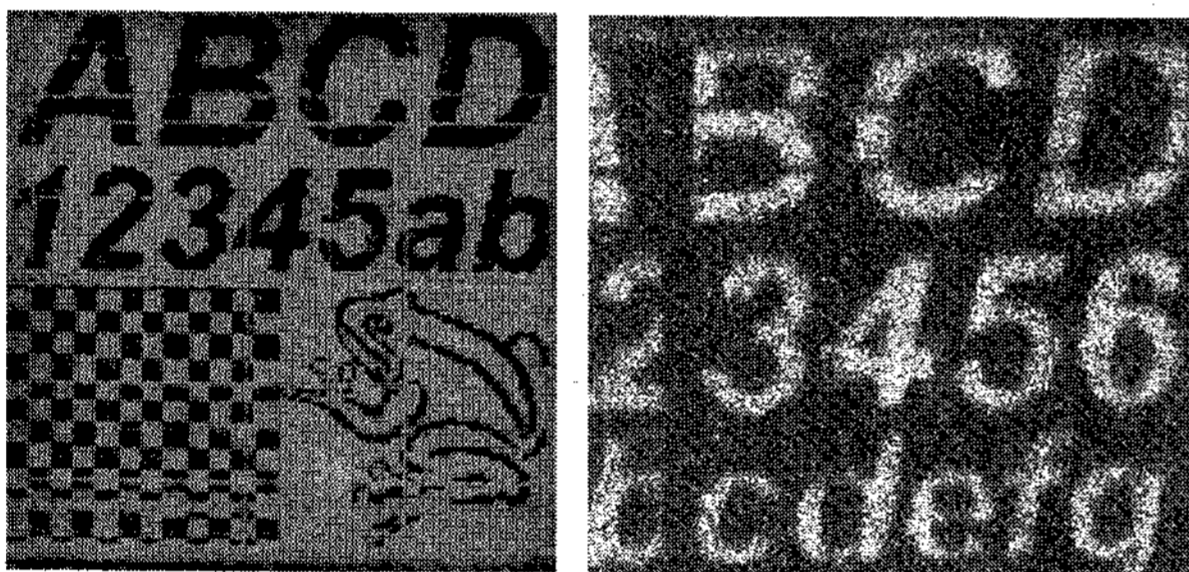

Fig. 9. (Left) Reflective electrophoretic display made using the printed TFT backplane. (Right) Reflective display fabricated from a 128x128 printed polymer TFT array with gyricon media.

encapsulated films in dry air [11]. The devices are affected by humidity, although the effects are reversible, and by airborne impurities. We find that simple encapsulation Provides good protection, and that the further encapsulation provided by a display can yield long term stability.

The bias stress effects in polymers are significant and fairly complicated [12]. Our studies of PQT show that there are both fast and slow components of the bias stress, which give a threshold voltage shift under prolonged application of a negative gate bias. The fast component reverses rapidly, and so does not have a significant long term effect. The slow component gives a threshold voltage shift that increases as a power law in time, as indicated in Fig. 8, and similar to the behavior of amorphous silicon. The rate of threshold voltage shift increases rapidly with gate voltage as shown in Fig. 8. The low duty cycle of an active matrix display minimizes the bias stress effect. Our studies

indicate that threshold voltage shifts can be kept below about 3 V for typical display operating conditions. However, further long term studies are needed.

3. Prototype Displays

These printed TFT backplanes have been integrated with reflective display media to make small prototype displays on both glass and flexible substrates [13]. The intention is to demonstrate that digital lithography and additive printing are a practical means to fabricate both a-Si and polymer active matrix arrays, and that polymer semiconductors can operate displays. Our research has focused on reflective displays but the backplanes could similarly be applied to liquid crystal displays. Indeed the lower operating gate voltage of the LCD would help to reduce the bias stress effect and extend the lifetime.

We have tested both gyricon and electrophoretic display media with a-Si and polymer TFTs. The electrophoretic media were encapsulated in an SU8 cell structure and laminated onto the backplane. An example of a display with a print-patterned a-Si TFT backplane is shown in Fig. 7, and operates at a gate voltage of 15-40 V.

The gyricon media comprises rotating bichromal spheres, and has the characteristics of excellent bistability, with a high operating voltage of 60-100V. Operation of this display with printed polymer TFTs was successfully demonstrated, with brightness and contrast that are consistent with the known properties of the media, and an image is shown in Fig. 7. One of the printed polymer TFT gyricon displays has been tested intermittently for about a year with no obvious degradation, despite being stored in room light ambient. This shows that the media provides sufficient protection so that transistors degradation is not a significant problem.

4. Discussion

The large feature size associated with present jet-printing technology affects the capability of the technique by limiting the pixel size. We currently fabricate arrays with pixel size of 340 microns and this is about as small as can be made with our present printing equipment and with a reasonably high aperture ratio. The jet-printing techniques

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may therefore initially be most useful for larger format displays. A smaller ejected drop size would give a corresponding reduction in the minimum pixel size. The present 40 micron feature size is not limited by the printing technology but by the present needs of document printing. A reduction by a factor 2 should need minimal new technology and only a redesign of the print-head.

The capacitance of overlapping metal layers is one of the concerns of jet-printed arrays. Gate to pixel capacitance gives a feed-though charge which affects the pixel voltage. The effect can be corrected for in the addressing of the pixel, but needs to be minimized. The good spot placement precision of jet-printing allows the metal overlap to be smaller than the feature size, and further improvement in printing precision is desirable. The lower mobility of the polymer TFTs compared to a-Si requires a larger W/L TFT to give the same performance and so causes a corresponding increase in the overlap capacitance. It is therefore highly desirable to improve the mobility of the polymer TFTs and many groups are working on new polymer formulations to achieve this goal.

One strategy to improve the performance of printed TFT backplanes is to use a 3-dimensional design. In a planar format the pixel elements compete for space, and many design compromises must be made. In a 3-dimensional structure, the TFTs are in one layer, each interconnect line could have its own metal layer, and the contact pad can take up most of the top surface. This approach does not necessarily work for an LCD display which must be transparent, but can be applied to reflective displays.

5. Summary

Our research has shown that jet-printing is a versatile

method of patterning electronic devices and particularly flat panel displays. The combination of printed etch masks and additive printed active materials allows almost any combination of materials to be patterned. Although the printed feature sizes are still large, due to the existing print-heads, significant reduction in size can be expected as the printing technology develops. The increased availability of nano-particle metal solutions and polymer dielectrics should allow the development of a fully additive printing process in the future.

References

[1] T. R. Hebner, C. C. Wu, D. Marcy, M. H. Lu, and J. C. Sturm, *Appl. Phys. Lett.*, **72**, 519 (1998).

[2] C. M. Hong and S. Wagner, *IEEE Electron Device Letters* **21**, 384 (2000).

[3] W.S. Wong, S. Ready, R. Matusiak, S.D. White, J.-P. Lu, J. Ho, and R.A. Street, *Appl. Phys. Lett*, **80**, 610 (2002).

[4] W.S. Wong, S.E. Ready, J.P. Lu, and R. A. Street, *Electron Dev. Lett.* **24**, 577 (2003).

[5] K.E. Paul, W.S. Wong, S.E. Ready, and R.A. Street, *Appl. Phys. Lett.*, **83**, 2070 (2003).

[6] A. C. Arias, S. E. Ready, R. Lujan, W. S. Wong, K. E. Paul, A. Salleo, M. L. Chabinyc, R. B. Apte, Y. Wu, P. Liu, B. S. Ong, and R. A. Street, *Appl. Phys. Lett.* **85**, 3304 (2004).

[7] J. A. Rogers, Z. Bao, and K. Baldwin et al., *Proc. Nat. Acad. Sci.* **98**, 4835 (2001).

[8] G. B. Blanchet, Y-L. Loo, J. A. Rogers, F. Gao, and C. R. Fincher., *Appl. Phys. Lett.* **82**, 463 (2003).

[9] M.L. Chabinyc, W. S. Wong, K. E. Paul, and R. A. Street., *Advanced Materials*, **15**, 1903 (2003).

[10] B. S. Ong, Y. Wu, P. Liu, and S. Gardner, *J. Am. Chem. Soc*, **126**, 3378 (2004).

[11] M. Chabinyc, to be published.

[12] A. Salleo, F. Endicott, and R. A. Street, *Appl. Phys. Lett.*, **83**, 263505 (2005).

[13] J. H. Daniel, A. C. Arias, W. S. Wong, R. Lujan, B. S. Krusor, R. B. Apte, R. A. Street, N. Chopra, and P. M. Kazmaier, *SID '05 Digest* (2005), p. 1630.