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Development of an RSFQ 4-bit ALU

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RSFQ 4-bit ALU개발

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Abstract

We have developed and tested an RSFQ 4-bit Arithmetic Logic Unit (ALU) based on half adder cells and dc switches. ALU is a core element of a computer processor that performs arithmetic and logic operations on the operands in computer instruction words. The designed ALU had limited operation functions of OR, AND, XOR, and ADD. It had a pipeline structure. We have simulated the circuit by using Josèphson circuit simulation tools in order to reduce the timing problem, and confirmed the correct operation of the designed ALU. We used simulation tools of XIC™, WRspice™, and Julia. The fabricated 4-bit ALU circuit had a size of 3000 μm × 1500 μm, and the chip size was 5 mm × 5 mm. The test speeds were 100 kHz and 5 GHz. For high-speed test, we used an eye-diagram technique. Our 4-bit ALU operated correctly up to 5 GHz clock frequency. The chip was tested at the liquid-helium temperature.

Keywords : flux, quantum, arithmetic, logic, superconductivity, digital

I. Introduction

Arithmetic Logic Unit (ALU) is an essential component to build a computer processor. Recently, telecommunication industry has requested high data transfer capability and fast process unit. The Rapid Single Flux Quantum (RSFQ) integrated circuit systems have a potentially high performance over semiconductor integrated circuit systems, in terms of their high frequency operation and extremely low power consumption. It can be a suitable solution [1].

The purpose of this paper is to develop an RSFQ 4-bit ALU by using non-standard cells. By using non-standard cells, we could construct more compact circuits and simplify the designs. Our target frequency was 5 GHz. The designed 4-bit ALU had about 1,000 Josephson junctions, and occupied the layout area of 3000 μm × 1500 μm. We tested the 4-bit ALU at various speeds [2,3,5].

II. Circuit Designs

We have designed, fabricated, and tested the RSFQ 4-bit ALU. The designed ALU had limited operation

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functions of OR, AND, XOR, and ADD. It had a pipeline structure. The ALU circuits consisted of half adder cells and dc switches. The 1-bit ALU block had a half adder cell and three dc switches, but the 4-bit ALU had 10 half adder cells and 12 dc switches. The block diagram of the simple 1-bit ALU is shown in Fig. 1 [4]. We can select proper outputs of the half adder cell with three switches to choose the logical functions. Table.1 shows the logical table for the instruction decoder. If both switches "a" and "b" are "ON," the ALU operates as an OR. If only switch "b" is "ON," the ALU operates as an AND. If both switches "a" and "c" are "ON," the ALU operates as an adder. If only switch "a" is "ON," the ALU operates as an XOR.

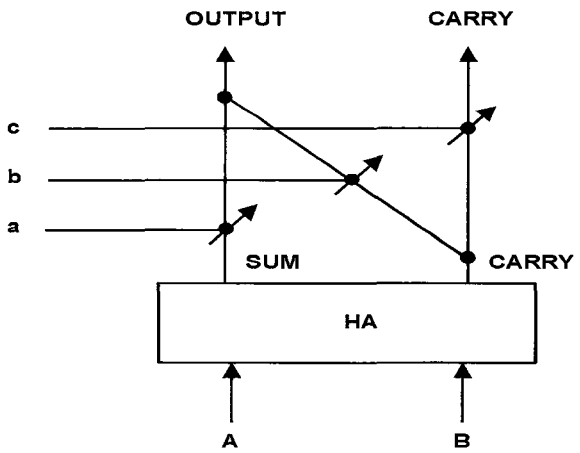

Fig. 1. Schematic block diagram of the 1-bit ALU that uses only one half adder. Four logic operations of OR, AND, ADD, and XOR can be performed by controlling the three dc switches a, b, and c.

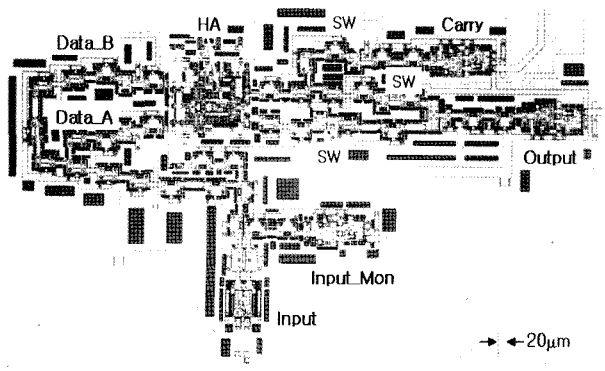

Fig. 2. Photo image of a 1-bit ALU for high-speed test.

Table 1. Switch selections for each logic function in the superconductive ALU.

	OR	AND	ADD	XOR
a	1	0	1	1
b	1	1	0	0
c	0	0	1	0

Fig. 2. shows the photo image of a 1-bit ALU block constructed for high-speed tests. The input port of the ALU is connected to a DC/SFQ circuit. This DC/SFQ circuit converts the signal from an Arbitrary Waveform Generator (AWG) to an SFQ pulse train. These SFQ pulses entered through some JTLs to a pulse splitter. SFQ pulse splitter produced two SFQ pulses (one on each output) for each incoming pulse. We used these SFQ pulses as two input data of the 1-bit ALU block.

Our 4-bit ALU extended the existent of our 1-bit ALU block. Diagram of the designed 4-bit ALU is shown in Fig. 3. It had 8 input data channels. The most important point in the 4-bit ALU design was in the timing of the clock pulses distributed throughout the 4-bit ALU circuit. To operate at high clock frequency, we used the forward clocking scheme and could optimize the operation speed of the circuit. We have simulated the circuit by using Josephson circuit simulation tools in order to reduce the timing problem and confirmed the correct operation of the designed ALU. We used simulation tools of XIC™, WRspice™, and Julia.

Figure 4 shows the completed 4-bit ALU core circuit layout. The designed ALU occupies the layout area of 3000 μm × 1500 μm.

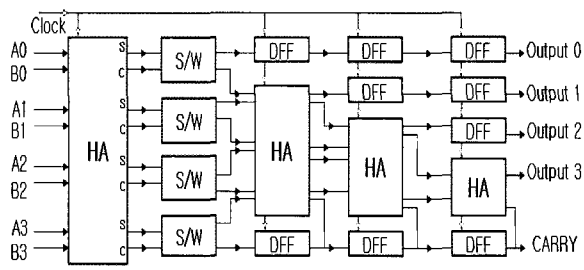

Fig. 3. Block diagram of the 4-bit ALU. Our 4-bit ALU had 5 output channels, which are noted as ouput 0 to 3 and CARRY. We used the forward clocking scheme.

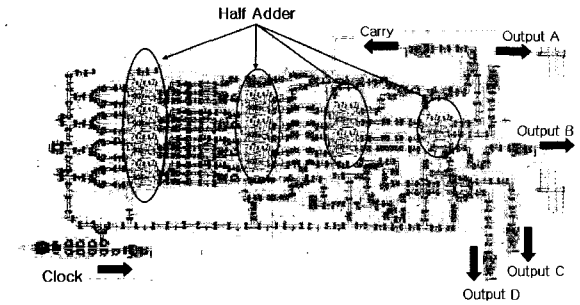

Fig. 4. Mask layout of the 4-bit ALU. The ALU core circuit size was 3000 μm × 1500 μm.

III. Circuit Test

The circuits were fabricated by Korea Photonics Technology Institute (KOPTI) with its standard ten-level Nb process (Josephson critical current density of 1 kA/cm^2) [6,7].

We used a computerized test setup to test the RSFQ digital circuits more effectively. Finding optimum dc bias current was very important in operating the RSFQ circuit. We constructed an automatic test setup with PXI (PCI eXtensions for Instrumentation) measurement system. Our PXI system generated an AWG signal and detected the output signal of 0.1mV range through SFQ/DC circuit. To test the circuit at cryogenic environment, we used a high-speed cryo-probe. This probe has 40 parallel contact pads, 26.7 GHz bandwidth, and auto alignment of 5 mm × 5 mm chip.

The data inputs were gated at 100 kHz. By using the switches as an instruction decoder, we were selecting the ALU operation of ADD, OR, AND, and XOR.

At the high-speed test, we observed so-called "eye-diagram" on the oscilloscope. If there is no output signal, the output monitor was in a random voltage state giving us a double line ("0"/"1") on the oscilloscope. Test results in figure 6 showed a correct operation at 5 GHz of the designed 1-bit ALU. Our high-speed measurements also showed that the 1-bit ALU operated correctly at 20 GHz.

Fig. 7. shows high-speed eye diagram test results of the 4-bit ALU at 5 GHz. These results were ADD test. As shown in figure 7, designed 4-bit ALU worked correctly at high frequency clock.

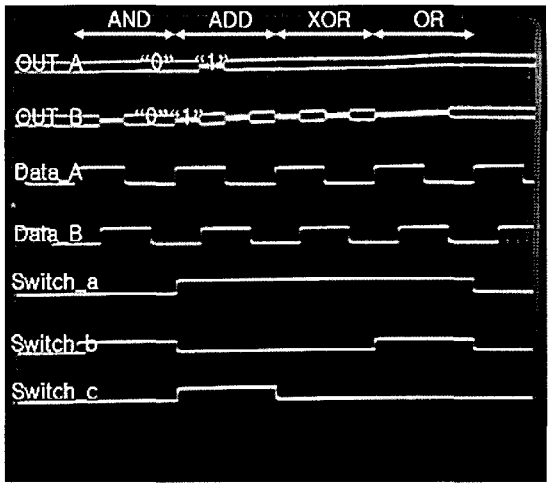

Fig. 6. 5-GHz test results of the 1-bit ALU block. The above graph shows OR, AND, XOR and ADD of the 1-bit ALU block.

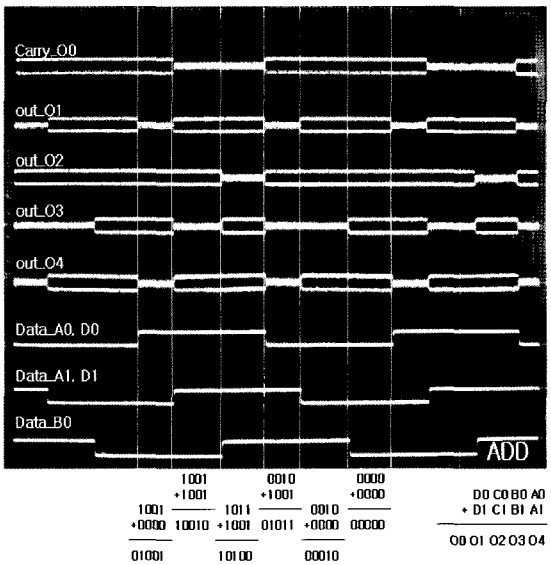

Fig. 7. 5-GHz test results of the 4-bit ALU. Correct operation of the circuit is shown. The six case of ADD are shown in the above picture.

Fig. 8. shows the test results of OR, XOR, and AND. The six case of OR XOR, and AND, are shown in the Fig. 8, and the bottom picture shows the input data traces. As shown in Fig. 8, the logical operation of OR, XOR, and AND, does not have carry output. In the case of logical operation, the carry output value was always "0".

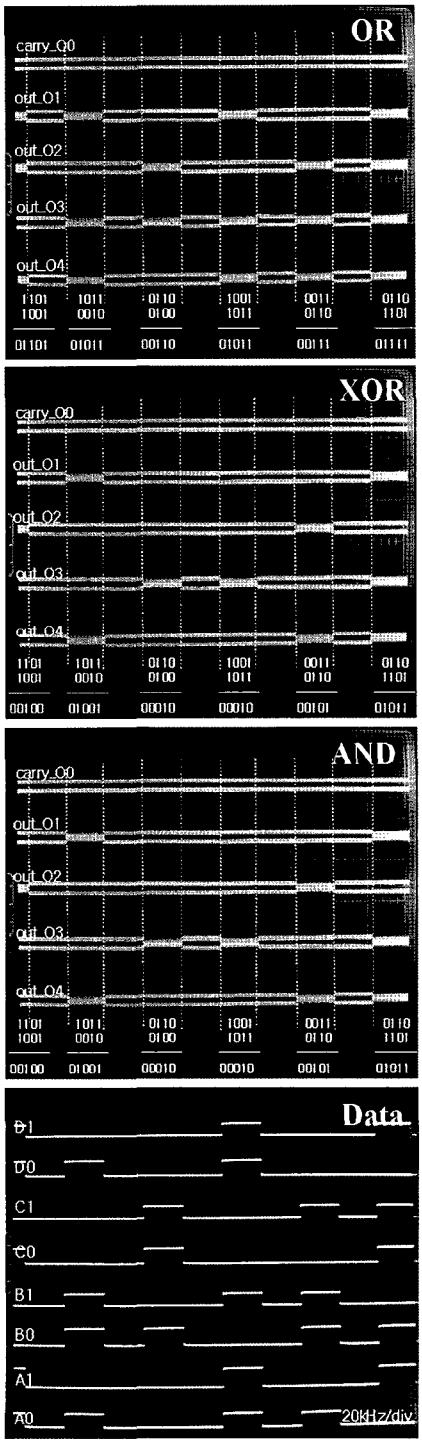

Fig. 8. The 4-bit ALU testing result. The six case of OR XOR, and AND, are shown in the above picture. The bottom picture is shown input data traces.

IV. Conclusion

We have designed, fabricated, and successfully tested the RSFQ 4-bit ALU. The designed circuit operated correctly for all four operations of ADD, OR, AND, and XOR at low speeds and high speeds. The 1-bit ALU block was tested at the high frequency up to 20 GHz and the 4-bit ALU was tested at the high frequency up to 5 GHz. Both tests showed correct operations of the circuits.

Acknowledgments

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References

[1] K. K. Likarev and V. K. Semenov, "RSFQ Logic/Memory Family: A new Josephson Junction Technology for sub-Terahertz Frequency Clock Digital Systems", IEEE Trans. Appl. Supercon.d, Vol. 1, 13-28, (1991).

[2] O. A. Mukhanov, S. V. Polonsky, V. K. Semenov, "New elements of the RSFQ Logic Family", IEEE Trans. Mag., Vol. 27, 2435-2438, (1991).

[3] N. Yosikawa, F. Matsuzaki, K. Yoda, "Design and component test of a 1-bit RSFQ microprocessor", Physica C, Vol. 378, 1454-1460, (2002).

[4] J. Y. Kim, S. H. Baek, J. H. Kang, "Construction of a Single Magnetic Flux Quantum Switch and Its Usage in an Arithmetic Logic Unit", J. Kor. Phys. Soc., Vol.43, 1129-1134, (2003).

[5] M. Dorojevets, "A 20-GHz FLUX-1 superconductor RSFQ microprocessor", J. Phys. IV France, Vol. 12, 157-160 (2002).

[6] Alex F. Kirichenko, Oleg A. Mukhanov, "Advanced On-ChipTest Technology for RSFQ Circuits", IEEE Trans. Appl. Superco.d, Vol. 7, 3438-3441, (1997).

[7] O. A. Mukhanov, S. V. Rylov, V. K. Semenov, "RSFQ Logic Arithmetic", IEEE. Trans. Mag., Vol. 25, 857-860, (1989).