The Analysis of p-MOSFET Performance Degradation due to BF_2 Dose Loss Phenomena

Jun-Ha Lee[a] and Hoong-Joo Lee
Information Display Research Center, Department of Computer System Engineering, Sangmyung University, Anseo-dong, Chonan-si, Chungnam 330-720, Korea

[a]E-mail : junha@smu.ac.kr

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Continued scaling of MOS devices requires the formation of the ultra shallow and very heavily doped junction. The simulation and experiment results show that the degradation of pMOS performance in logic and SRAM pMOS devices due to the excessive diffusion of the tail and a large amount of dose loss in the extension region. This problem comes from the high-temperature long-time deposition process for forming the spacer and the presence of fluorine which diffuses quickly to the Si/SiO_2 interface with boron pairing. We have studied the method to improve the pMOS performance that includes the low-energy boron implantation, spike annealing and device structure design using TCAD simulation.

Keywords : p-MOSFET, Simulation, BF_2, Dose loss, Device performance

1. INTRODUCTION

Ideally, the driving current of MOSFET is controlled by the channel resistance, but realistically, other resistive components influence the degradation of the device performance[1]. Lots of relevant literature have shown that the formation of shallow junction and heavily doped extension can solve the problems caused by the short-channel effect and the increased resistance[2-6]. For deep submicron devices, simple scaling alone will not suffice to improve performance. Series resistance in the source/drain region is becoming a bottleneck for pMOS device performance[7]. Since, for the present, the performance ratio between nMOS and pMOS devices reaches more than 3:1, the performance improvement for the pMOS device must be a problem awaiting solution in a full chip design. This paper presents both the analysis on device performance and the methods for performance improvement for the pMOS device using the measured data and TCAD (Technology Computer Aided Design) simulation. Additionally, a dose loss mechanism has been analyzed based on the movement of fluorine on BF_2 ion-implantation and the condition for the following annealing and oxide/ntiride film deposition. And, the low-energy boron ion-implantation and rapid thermal annealing (RTA) which are applied to a mass production have been evaluated through simulation.

2. PMOS PERFORMANCE FACTORS

Figure 1 shows the simulated boron doping distribution and junction profile for the extension region and the source/drain region of the pMOS device with a gate length of 0.13 μm.

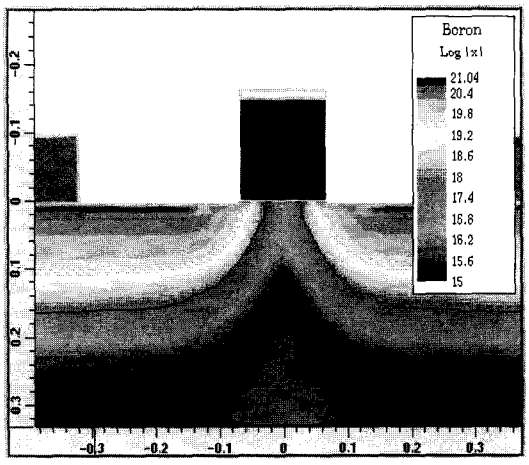

Fig. 1. Simulated boron doping distribution and junction profile of 0.13 μm -technology pMOS device.

2.1 Analysis on deep source/drain

Figure 1 does not show a, so-called, shallow extension

which should be considered on junction engineering. The reasons could be the deep source/drain overspreads the extension region due to both 1800 Å vertical junction depth of the deep source/drain region and 1100 Å lateral junction depth. The lateral junction was defined as 65 % of the vertical depth. In the case of the extension region covered up by the deep source/drain, improvement of short-channel effect using the shallow extension cannot be expected[8].

The device performance means the capability of transistor current drive. PMOS performance in term of I_{Dsat} current can be improved by the electron mobility increase, the thinner gate oxide and minimize the resistance. Moreover, since the excessive channel implant and halo implant are needed to obtain the effective threshold voltage, the device performance cannot but degrade due to the decrease of channel mobility[9]. For the case of a device with the spacer length 700 Å comprised of gate poly layer, oxide layer and nitride layer, the vertical junction depth must be around 1000 Å ~ 1300 Å for the source/drain region not to overspread the extension region. In Fig. 2, the simulated doping profiles are shown. The simulation conditions were the boron implantation with a dose of 3E15/cm^2 and energies of 1 KeV and 5 keV, respectively, and successive activation annealing temperature of 1025 ℃. A simulation result for case of 5 KeV has been compared to the SIMS(Secondary Ion Mass Spectroscopy) measurement data. The SIMS sample was prepared as follow. The boron was implanted to a Si(100) substrate which has 50 Å buffer oxide. After implantation, rapid thermal annealing was performed at the temperatures of 1025 ℃.

As shown in Fig. 2, the boron energy was reduced to 1

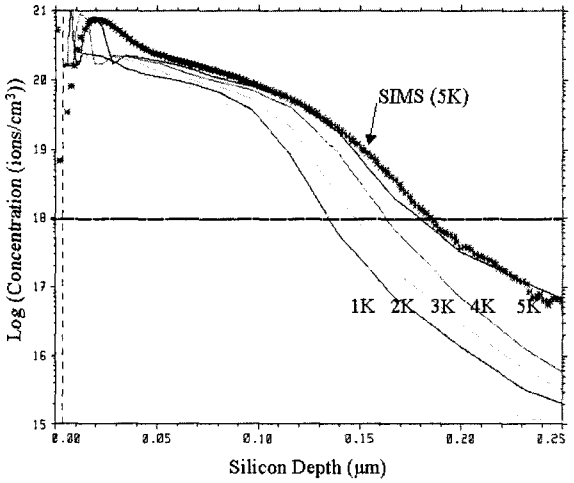

Fig. 2. Boron doping profiles of energy 1 K ~ 5 K implanted and annealed at 1025 ℃.

KeV, but a vertical junction depth less than 1300 Å making the extension was not obtained. A vertical junction depth of 1500 Å might be obtainable under a specific process condition satisfying a reduced buffer oxide thickness, a reduced annealing temperature compared with conventional temperature, and an energy of about 2 ~ 3 KeV. However, under other simulation conditions making the extension region appear, I_{Dsat} at the same I_{Doff}, unfortunately, has not been increased compared to the case of the extension overspread by source/drain. That results from the low doping concentration in the extension region even though the junction depth is shallow. I_{Dsat} and I_{Doff} are the output parameters of device characteristics. The I_{Dsat} is the saturated drain current for $V_g = V_d = 3.3$ V and I_{Doff} is the leakage current for $V_g = 0$ V and $V_d = 3.3$ V.

2.2 Analysis on extension region

SIMS profiles at each step of spacer formation, activation, and oxide/nitride deposition after BF_2 implantation with a dose of 4E14/cm^2 have been shown in Fig. 3. The profile in the extension region cannot be specified with junction depth, activated boron concentration and doping abruptness which means the slope of concentration. Table 1 presents a comparison between ITRS(International Technology Roadmap for Semicon-

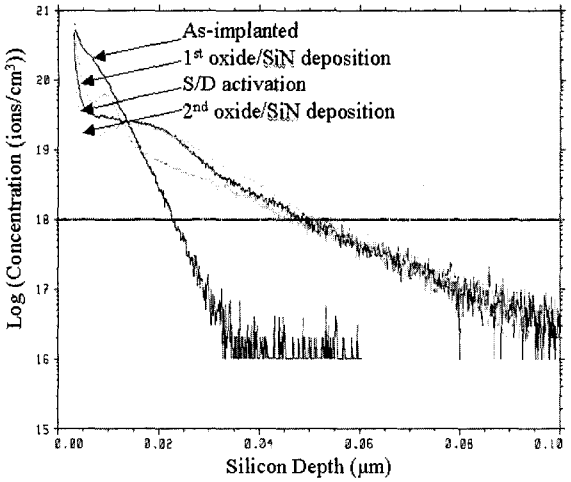

Fig. 3. SIMS profiles of extension region.

Table 1. Comparison of ITRS roadmap and extracted value from extension SIMS data.

	ITRS roadmap	SIMS Data
Xj (Å)	500	600
Rs (Ω/□)	700	5000
Abruptness (nm/decade)	10	20

ductors) estimate and measured SIMS data after the final annealing in the extension region.

There has been a dose loss as well as severe diffusion in as-implanted boron profile after MTO as depicted in Fig. 3, which means that fluorine ions have boron ions trapped at the SiO_2/Si interface and in the oxide bulk[10]. The trapped boron ions have been thought to be deactivated, and removed during etching prior to SIMS measurement. The amount of dose loss at the final profile is about 60 %, and the sheet resistance is about 5 KΩ. Table 2 presents a dose loss percentage of each process condition. Namely, the junction depth becomes shallow in the case of the extension not overspread by source/drain, but the low doping level brings about the steep increase of sheet resistance which results in the degradation of the device performance which means the capability of transistor current drive.

Table 2. Dose loss percentage of each process condition.

	MTO	BF_2	Boron
RTA	Hot-Temp.	60%	35%
	Low-Temp.	20-30%	10-15%
Spike	Hot-Temp	30-60%	35%
	Low-Temp	20-30%	5-15%

2.3 Analysis on junction depth and activation level

We analyzed the performance variation due to the peak concentration and junction depth in the extension region. Each contour line means the equal device performance. It has been analyzed that the device with a junction depth of 450 Å and a peak concentration of 3E19/cm^2 in the dose-lost extension region has the same performance as the case of the overspread extension with a junction depth 800 Å and a peak concentration of 1E20/cm^2. Every 1 % improvement of the device performance can be expected by every 1E19/cm^2 increase of the peak concentration, and every 2.5 % performance improvement can be also expected by every 100 Å decrease of the junction depth. Consequently, 10 ~ 15 % performance improvement can be possible, when the extension is made with a junction depth of 400 Å and a peak concentration of 1E20/cm^2 which is the ITRS estimate. 10 ~ 15 % performance improvement can be also considered by the resistance decrease of 170 ~ 250 Ω, since based on device simulation, 500 Ω resistance decrease can be converted into 30 % current increase. Resistance in the surface accumulation region, Racc (Accumulation Resistance), is controlled by the extension tail region below the gate. The abrupt extension profile should be, thus, formed to reduce Racc.

2.4 Dose loss mechanism

In case of BF_2, a large amount of dose loss, i.e., 40 ~ 60 %, happens after oxide removal due to the boron pile-up at Si/SiO_2 interface. BF_2 is distinguished from boron based on the following facts. BF_2 makes a shallow junction, considerable amount of dose loss, and relatively high activation level. On the other hand, boron allows deep junction, no dose loss, and strong de-activation[11,12]. Not the damage from the implantation but the existence of fluorine makes the property difference between BF_2 and boron[13,14].

3. ANALYSIS ON DEVICE PERFORMANCE

3.1 Deep source/drain

Source/drain profile must be deep enough to prevent the increase of resistance during the silicide contact fabrication. But, in case of the deep source/drain, the extension should not be laterally overspread. Therefore, a low-energy boron implantation is needed to form a proper extension region, and then the following spike annealing is indispensible. Figure 4 shows junction depths depending on both the deep source/drain implantation energy and the annealing condition. In this work, it has been found that a junction depth of 1000 ~ 1300 Å with the boron energy of 3 ~ 5 KeV might makes the best device performance.

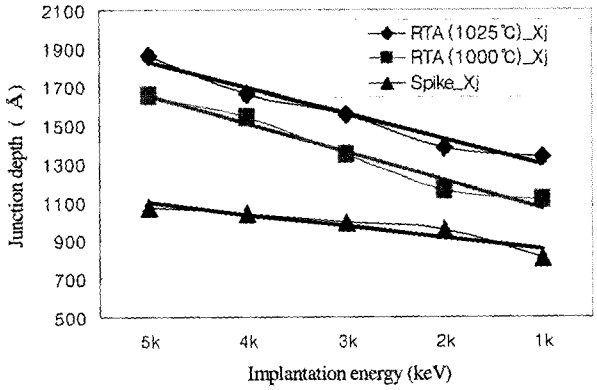

Fig. 4. Dependence of junction depth on boron energy and annealing condition.

3.2 Extension region

Simulation has been done to extract an optimal process condition for the extension region. The simulation parameters for ion implantation have been split into dose of 4E14/cm^2 and energies of 2 ~ 5 KeV with BF_2, dose of 1E15/cm^2 and energies of 2 ~ 200 eV with boron, and dose of 1E15/cm^2 and energies of 2 ~ 200 eV with boron after pre-amorphization. And the simulation parameters for successive annealing have

been split into high temperature deposition-RTA(Rapid Thermal Annealing) (1025 ℃/10 sec), low temperature deposition-RTA, and spike annealing(1050 ℃, ramping rate of 150 ℃/sec). The results show a peak concentration and a junction depth extracted under each simulation condition. Fluorine in BF_2 has a natural property suppressing TED(Transient Enhanced Diffusion), but boron shows more diffusion due to BIC (Boron-interstitial Cluster) formation than fluorine. Since the relatively high dose of boron implantation is used, in case of the low energy boron, especially, spike annealing must be necessary to avoid the deep junction [15]. And it has been found that the pre-amorphization prior to implantation does not have an effect on the junction depth after diffusion.

3.3 Device characteristic

Under the above conditions, I_{Doff} / I_{Dsat} simulation has been performed for the 0.13 μm pMOS technology. Figure 5 shows the simulation results. At the point of I_{Doff} of 1 nA and Vd of 1.2 V, I_{Dsat} can be improved from 0 to 27 % depending on impurities and annealing condition as shown in Table 3.

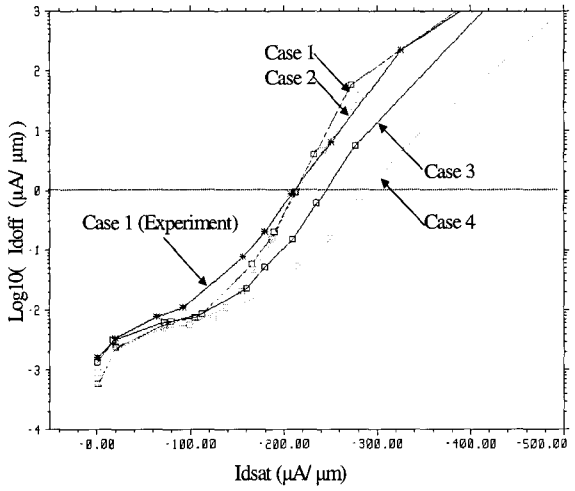

Fig. 5. Dependence of I_{Doff} - I_{Dsat} relations on extension structure.

Table 3. Simulated device performance.

	S/D	Extension	Anneal	Idsat (Vd=1.2)	Ref.
Case1	B 5K	BF_2	HT-RTA	200 uA/μm	Ref.
Case2	B 2K	BF_2	HT-RTA	200 uA/μm	0%
Case3	B 2K	BF_2	LT-RTA	230 uA/μm	15%
Case4	B 5K	Boron	LT-Spike	255 uA/μm	27%

4. CONCLUSIONS

In this paper, for 0.13 μm pMOS technology, analysis on the cause of device performance degradation and its solution have been presented through the calibrated TCAD simulation. It has been analyzed that up to 60 % dose loss during the extension formation comes from the quick diffusion of fluorine as well as the high temperature deposition. The simulation results have shown that 15 % I_{Dsat} improvement can be made if the factors causing the dose loss are eliminated. Also, the high dose of boron implantation with an energy of 200 eV must be essential to increase the peak concentration in the extension region. Together with a spike anneal to suppress the boron diffusion, I_{Dsat} could be increased by 25 %. Henceforth, the study on source/drain structure minimizing the contact resistance and channel/halo structure maximizing the channel mobility should be needed to obtain to the better pMOS device performance.

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