A Study on the Optimized Copper Electrochemical Plating in Dual Damascene Process

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In this work, we studied the optimized copper thickness in Cu ECP (Electrochemical Plating). In order to select an optimized Cu ECP thickness, we examined Cu ECP bulge (bump, hump or over-plating amount), Cu CMP dishing and electrical properties of via hole and line trench over dual damascene patterned wafers split into different ECP Cu thickness. In the aspect of bump and dishing, the bulge increased according as target plating thickness decreased. Dishing of edge was larger than center of wafer. Also in case of electrical property, metal line resistance distribution became broad gradually according as Cu ECP thickness decreased. In conclusion, at least 20 % reduced Cu ECP thickness from current baseline; 0.8 μm and 1.0 μm are suitable to be adopted as newly optimized Cu ECP thickness for local and intermediate layer.

Keywords : Electrochemical plating (ECP), Chemical mechanical polishing (CMP), Step height, Array height, Dishing

1. INTRODUCTION

Since damascene technology announced, copper (Cu) metallization using electrochemical plating (ECP) has played an important role in back end of line interconnect formation[1-3]. The recent BEOL interconnect technology deposits barrier metal and seed Cu layer to via hole or trench pattern in dual damascene process. It forms Cu interconnect using bottom-up gap-fill that there is no seam or void[4,5]. And layer is planarized in Cu chemical mechanical polishing (CMP) process[6-8]. Therefore, Cu interconnect of multi-layer is formed by repeat of these process sequence. In damascene process, the problems related with process integration as well as with each unit process are becoming critical issues. Especially, step height (SH) and array height (AH) after Cu plating was closely related with pattern dependencies in Cu ECP and influenced in Cu CMP process. So, Cu plating target thickness in Cu ECP process was required to be optimized. After ECP process, to minimize integration issue by SH and AH uses leveler as admixture that promotes planarization of plated Cu film surface or increases plating target thickness of Cu ECP process. In case of the former, it has a limit to remove bulge perfectly. In case of the latter, it is not desirable in cost and TAT. Because Cu wastes, heavy metal, are happened much quantity in Cu CMP process, it can not become solution. Hence, we have to minimize Cu plating target thickness of Cu ECP process in allowed extent of whole process integration, and optimize process. We must find out process condition that can minimize dishing, erosion and oxide loss in Cu CMP process. We knew that the profile after Cu ECP influences in Cu CMP process. And we have to consider dishing, erosion and oxide phenomenon after Cu CMP process to associate with Cu ECP. In this work, we performed the tests of optimized Cu ECP thickness selection in dual damascene process considering pattern dependencies of Cu ECP and Cu CMP.

2. EXPERIMENTAL DETAILS

In this experiment, barrier metal was TaN/Ta bi-layer structure. We did sputtering etch step after TaN 10 nm/Ta 15 nm deposition, and removed TaN/Ta layer of

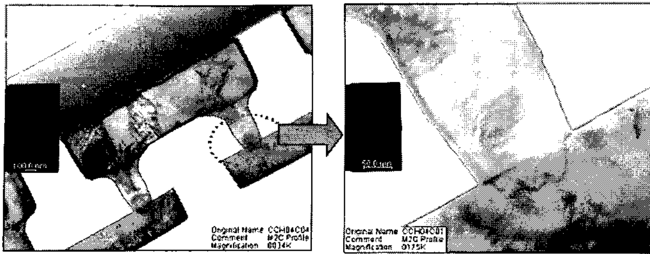


Fig. 1. Post Cu ECP TEM image: right enlarged picture shows DCV structure.

via hole bottom electively. In sputtering etch step, we deposited Ta layer 10 nm again adding flash step to via hole and neck of trench. Also, we confirmed gap-fill of dual Damascene structure using transmission electron microscope (TEM) after Cu ECP process. Figure 1 shows Post Cu ECP TEM image. We adjusted Cu plating condition changing bulk plating step time. And we confirmed AH using SEM after Cu ECP process. Finally, we measured dishing after Cu CMP process and Metal line resistance of layer.

3. RESULTS AND DISCUSSION

Figure 2 shows the profile after Cu ECP and Cu CMP process that depend on each pattern. The profile influences to the successful CMP process. And SH of Cu ECP process should be considered with AH according to pattern group form in isolated single pattern. Hence, we have to consider dishing, erosion and oxide phenomenon after Cu CMP process to associate with Cu ECP process.

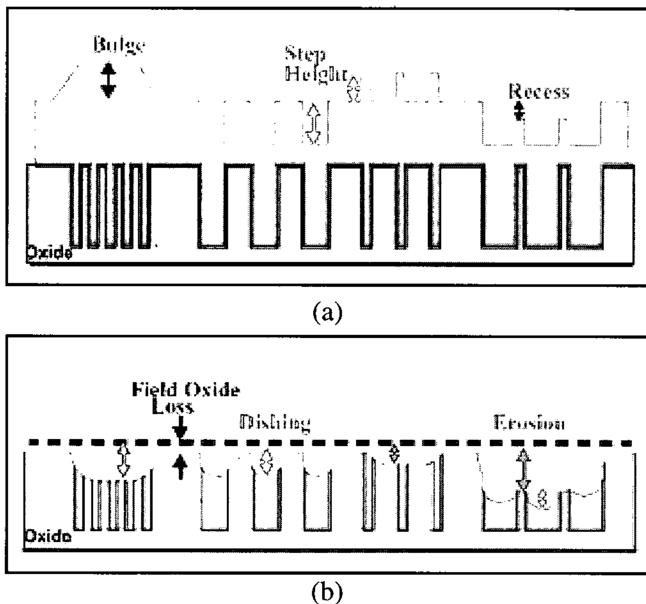
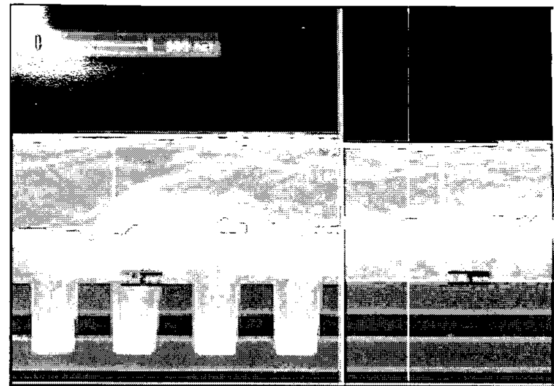
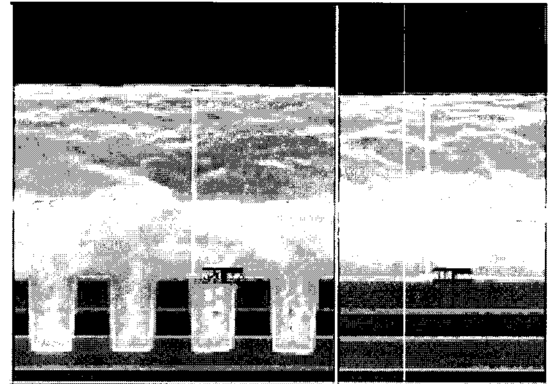


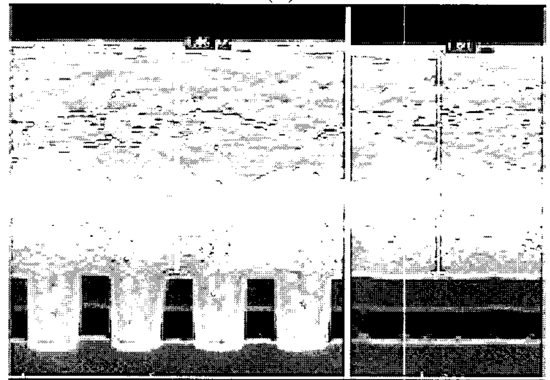
Fig. 2. (a) Post Cu ECP profile and (b) Post CMP profile.



(a)



(b)



(c)

Fig. 3. Post Cu ECP AH behavior per different plating target thickness; (a) bulge at 0.6 μm plating: 46 nm, (b) bulge at 0.8 μm plating: 43 nm, and (c) bulge at 1.0 μm plating: 20 nm.

Figure 3 shows AH after Cu ECP process using pattern wafer of different target plating thickness. We confirmed that bulge increased according as target plating thickness decreased. SH after Cu ECP process was experimented using step profiler of AFM (Atomic Force Microscope). Figure 4 shows step profiler data of FTA site scanning. In this experiment, we obtained the similar result to trench etch target depth. So, Cu ECP is conformal plating method like CVD in large pattern.

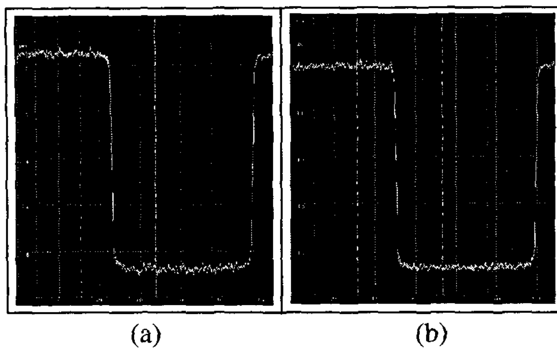


Fig. 4. Step profiler data of FTA site scanning; (a) post Cu ECP profile at center, and (b) post Cu ECP profile at edge.

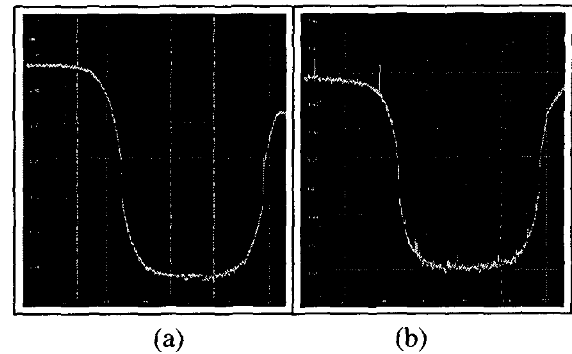


Fig. 6. Step profiler data of FTA site scanning (a) post Cu CMP at center, and (b) post DCVD at center.

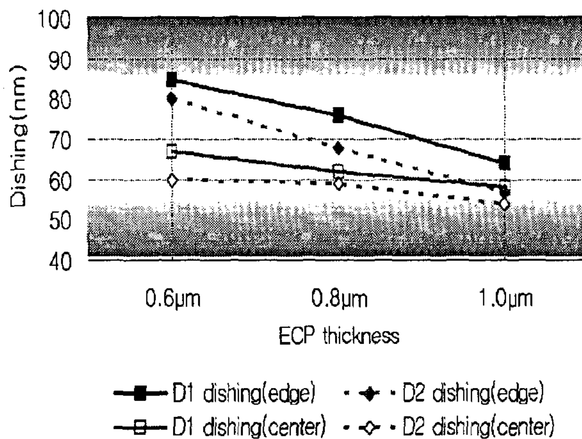


Fig. 5. Post Cu CMP dishing result per different plating target thickness at wafer center and edge.

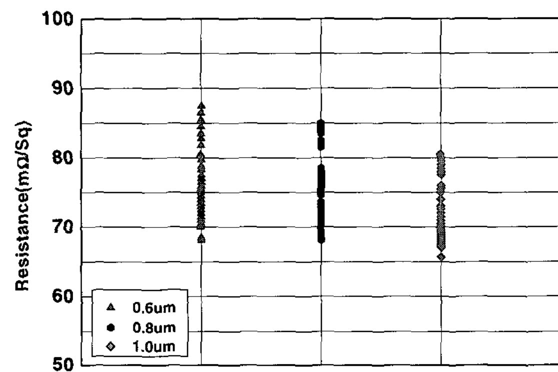


Fig. 7. Sheet Resistance per different target plating thickness.

Figure 5 shows post Cu CMP dishing result per different plating target thickness at wafer center and edge. We confirmed that dishing increased according as Cu ECP thickness decreased. Dishing of edge was bigger than center of wafer, and dishing of D1 layer was bigger about 5 nm more than dishing of D2 layer. And dishing after Cu CMP influenced to film profile of the successful DCVD process. Figure 6 shows Step profiler data of FTA site scanning after Cu CMP and DCVD process. We knew that dishing after Cu CMP should be considered like post Cu ECP SH and AH in BEOL integration. We performed an electrical test to find out the effect that different Cu ECP thickness condition affected in electrical property of metal wiring. Figure 7 shows sheet resistance per different target plating thickness in layer. Metal line Resistance of 0.6 μm target plating showed most broad distribution. Also, we confirmed that resistance distribution became broad gradually according as Cu ECP thickness decreased in layer. This result was similarly with aspect of dishing data after Cu CMP.

4. CONCLUSION

In this work, we performed the tests of optimized Cu ECP thickness selection in dual damascene process considering pattern dependencies of Cu ECP and Cu CMP. We confirmed that 0.8 μm and 1.0 μm Cu plating conditions in 0.13 μm technology node were not enough of difference in integration aspect and electrical properties with Cu CMP. 0.6 μm plating condition that baseline size reduced 40 % showed bad property in broad resistance distribution of metal line and dishing after Cu CMP process. In conclusion, at least 20 % reduced Cu ECP thickness from current baseline; 0.8 μm and 1.0 μm are suitable to be adopted as newly optimized Cu ECP thickness for local and intermediate layer.

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