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Preparation of Field Effect Transistor with $(Bi,La)Ti_3O_{12}$ Gate Film on Y_2O_3/Si Substrate

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Abstract: The field effect transistors (FETs) were fabricated on Y_2O_3/P-Si(100) substrates by the conventional memory processes and sol-gel process using $(Bi,La)Ti_3O_{12}$(BLT) ferroelectric gate materials. The remnant polarization ($2Pr = Pr^+ - Pr^-$) for Pt/BLT/Pt/Si capacitors increased from 22 $\mu C/cm^2$ to 30 $\mu C/cm^2$ at 5V as the annealing temperature increased from 700°C to 750°C. There was no drastic degradation in the polarization values after applying the retention read pulse for $10^{5.5}$ seconds. The capacitance-voltage data of Pt/BLT/Y_2O_3/Si capacitors at 5V input voltage showed that the memory window voltage decreased from 1.4V to 0.6V as the annealing temperature increased from 700°C to 750°C. The leakage current of the Pt/BLT/Y_2O_3/Si capacitors annealed at 750°C was about $5 10^{-8}$ A/cm^2 at 5V. From the drain currents versus gate voltages (V_G) for Pt/BLT/Y_2O_3/Si(100) FET devices, the memory window voltages increased from 0.3V to 0.8V with increasing the V_G from 3V to 5V.

Keywords: (Bi, La)Ti_3O_{12} (BLT), field effect transistor, capacitor, Y_2O_3 buffer layer, ferroelectric gate film

1. Introduction

As modern electronic devices such as personal digital assistants, mobile phones and notebook computers have became popular, considerable attention is focused on the nonvolatile ferroelectric memory devices which are capable of energy retention in the devices. The flash memory may be replaced with the advanced nonvolatile memories such as the ferroelectric random access memories (FRAM), phase change RAM (PRAM), magnetic RAM (MRAM) and spintronic devices. The nonvolatile memories are not necessary to refresh a memorized data. In particular, the FRAM devices show good features such as high speed operation, low power consumption, and large scale integration.[1,2] There are two kinds of ferroelectric nonvolatile memory devices. One is a memory device with a transistor and ferroelectric storage capacitor and another is the metal-ferroelectric-insulator-semiconductor field effect transistor (MFIS-FET). MFIS-FET devices have advantage over the ferroelectric storage capacitor types because of non-destructive read-out capability and high memory density.[3]

Until recently, some fabrication methods for the ferroelectric thin films such as sol-gel method, metal-organic decomposition, RF magnetron sputtering, and pulsed laser deposition have been prepared and demonstrated.[4,5] Bismuth-layer-structured ferroelectric (Bi, La)Ti_3O_{12} (BLT) material is known as one of the promising materials[6] for the non-volatile FRAM application due to their good fatigue proper-

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ties, low leakage current and high remnant polarization.[7-9] The technologies should be also developed to prevent the FRAM devices from inter-diffusion through the interface between ferroelectric film layer and Si substrate by means of a low temperature process and an optimization of the buffer layer materials.

In this research, Pt/BLT/Y_2O_3/Si FET devices were fabricated by the conventional memory processes. For this, BLT ferroelectric thin films were prepared on Y_2O_3/Si(100) substrate by using the sol-gel method. The dependences of electrical properties on the annealing temperatures were investigated for the prepared capacitors with structures of Pt/BLT/Pt/Si(100) and Pt/BLT/Y_2O_3/Si(100), respectively. In addition, we investigated the sectional morphology and the electrical properties for Pt/BLT/Y_2O_3/Si(100) FET devices.

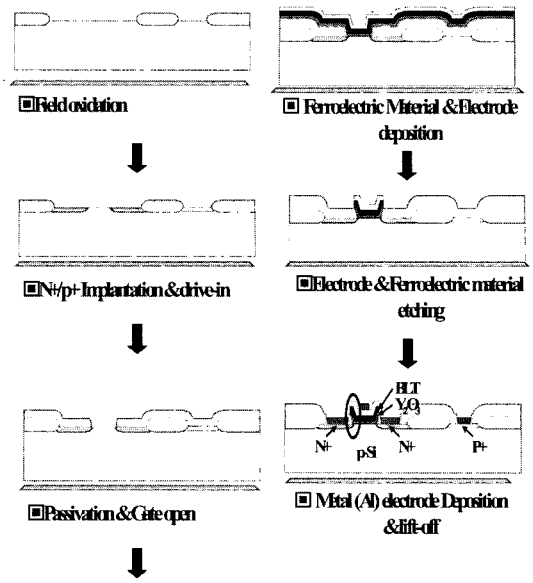

Fig. 1. Fabrication procedure of Pt/BLT/Y_2O_3/Si(100) field effect transistor.

2. EXPERIMENTAL PROCEDURE

First of all, the capacitors with the structure of Pt/BLT/Pt/Si(100) and Pt/BLT/Y_2O_3/Si(100) substrates were prepared for the characterization of ferroelectric and fatigue properties of the BLT thin films. The Pt film with 1500 Å thickness as lower electrode was deposited on Si(100) substrate by RF magnetron sputtering. For the application of FRAM devices, the MFIS-FET devices using BLT ferroelectric gate thin film on Y_2O_3 buffer layer/p-Si(100) substrates were fabricated by the conventional memory processes. The field oxidation layer with about 8000Å thickness was formed on P-Si(100) wafer (ρ:~10Ωcm) by the local oxidation of silicon. Arsenic (As) ion implantation (80KeV, 5 x10^{15}/cm^2) was carried out in order to fabricate N^+ well at the source and drain regions of Si(100) substrates. In addition, P^+ region was prepared at bulk contact area by Boron (B) ion implantation, and the drive-in process was done at 950°C for 30 minutes. After then, SiO_2 layer with a thickness of about 3000Å were deposited as passivation layer of the FET device. The gate area was opened by using ion milling method under the process condition of 110mA in beam current. The Y_2O_3 buffer layer with a thickness of 150 Å was deposited by RF magnetron sputtering method and annealed at 800 in the electric furnace. BLT sol-gel solution with the molar composition of ($Bi_{3.25}$, $La_{0.75}$)Ti_3O_{12} was spin-coated onto the Y_2O_3 buffer layer with a rotational speed of 3000 rpm for 30 seconds. After spin coatings, the films were baked on a hot plate at 330°C to remove the residual solvent. For the crystallization of BLT ferroelectric films, the annealing was carried out at the temperatures of 700°C and 750°C for 30 minutes under an air ambient. For the patterned device, Pt electrode and BLT film were etched by the reactive ion etching method. Finally, Al metal electrodes were deposited by DC sputtering and followed by a lift-off process to prepare the Pt/BLT/Y_2O_3/Si(100) FET devices.

Fig. 1. shows the flow chart of manufacturing process of the Pt/BLT/Y_2O_3/Si(100) FET devices.

The sectional morphology was observed by scanning electron microscope (SEM). The electrical properties, such as the polarization versus time, capacitance-voltage (C-V) and current-voltage characteristics of the devices, were measured by using

HP4180A, HP4155B, HP4192A and Precision Ferroelectric Test System.

3. RESULTS AND DISCUSSION

Fig. 2 shows the SEM micrograph of the cross-sectional view of the fabricated Pt/BLT/Y_2O_3/Si (100) FET device. It was difficult to find out a distinct inter-layers between BLT ferroelectric film and Y_2O_3 buffer layer, showing the thickness of about 4600Å for both film layers. The SiO_2 thickness was found to be about 2000Å as passivation layer. From the sectional morphology, the gate region may be the inside area of the trench device structure, and the source and drain regions are assumed at the marked dot area in the SEM photograph.

Fig. 3 shows the polarization versus voltage (P-E) hysteresis loops of Pt/BLT/Pt/Si(100) capacitors annealed at 700°C and 750°C, respectively. The P-E measurement was carried out at the input voltages of ±7V. All the film samples showed typical ferroelectric hysteresis property originating from a remnant polarization which is caused by the suppressed charge injection in the BLT films.[10] The remnant polarization depended on the annealing temperatures, and the calculated values of the remnant polarization ($2Pr = Pr^+ - Pr^-$) at 5V increased from 22 μC/cm^2 to 30 μC/cm^2 with increasing the annealing temperature from 700°C to 750°C. The coercive electric field (Ec) were found to be 81 ~83 kV/cm for both samples. To investigate the retention properties, the

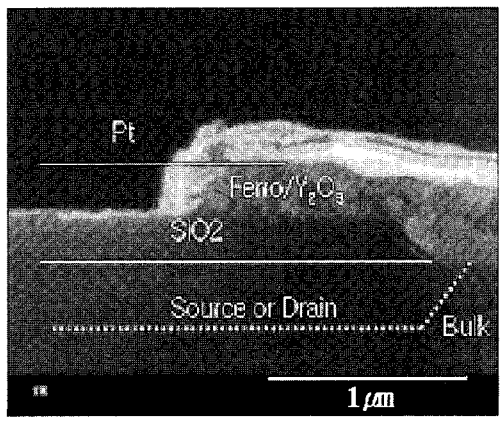

Fig. 2. SEM morphology of the cross-sectional view of Pt/BLT/Y_2O_3/Si(100) FET device.

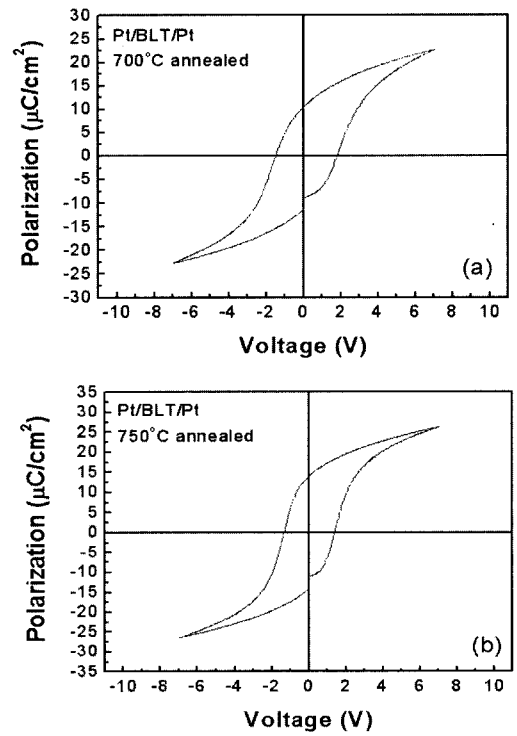

Fig. 3. Polarization versus voltages hysteresis loops of Pt/BLT/Pt/Si(100) capacitors annealed at (a) 700°C and (b) 750°C.

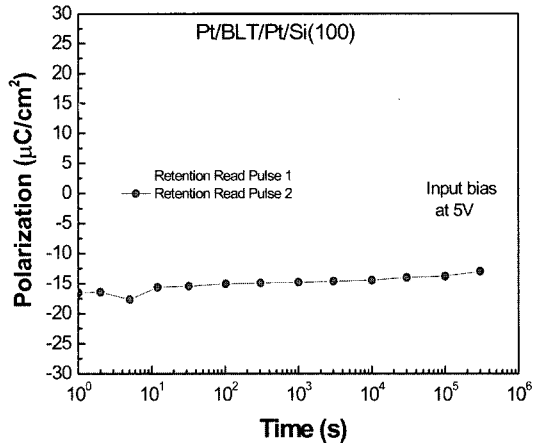

Fig. 4. The changes of polarization values of Pt/BLT/Pt/Si(100) capacitors annealed at 750°C as a function of applied retention times at 5V input voltage.

±5 V bipolar switching pulses were applied for the capacitors of Pt/BLT/Pt/Si(100) structure.

Fig. 4 shows the polarization changes as a function of the applied retention times for Pt/BLT/Pt/Si(100) capacitors annealed at 750°C. It was found that the capacitors showed no drastic change in the polarization values when the retention read pulses were applied for $10^{5.5}$ seconds at 5V, indicating a good charge retention property of the BLT films.

Fig. 5 shows the capacitance versus voltage (C-V) characteristics of Pt/BLT/Y_2O_3/Si capacitors annealed at 700°C and 750°C at 5V in bias voltage. The memory window voltages increased gradually with increasing the sweep voltage up to ±5V, and the memory window voltages were calculated from these C-V hysteresis loops. The memory window voltages decreased from 1.4V to 0.6V with increasing the annealing temperature from 700°C to 750°C. This result may be attributed to the dense microstructure and/or the suppression of inter-phases with a low dielectric constant at the lower annealing temperature of 700°C.[11] In addition, the C-V curve was shifted to the positive voltage, which may be caused by the negative charges of formed oxide layers and the volatility of Bi component during the annealing process of BLT film.

The leakage currents as a function of the applied

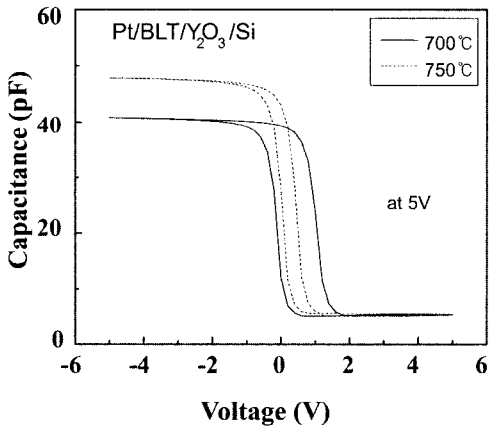

Fig. 5. Capacitance versus voltage characteristics of Pt/BLT/Y_2O_3/Si(100) capacitors annealed at 700°C and 750°C at 5V input voltage.

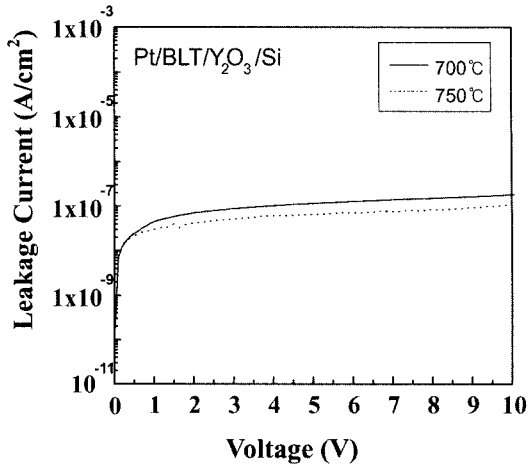

Fig. 6. Leakage current changes of Pt/BLT/Y_2O_3/Si(100) capacitors annealed at 700°C and 750°C as a function of the input voltages.

voltage for the Pt/BLT/Y_2O_3/Si(100) capacitors annealed at 700°C and 750°C are shown in fig. 6. The leakage current of the Pt/BLT/Y_2O_3/Si capacitors annealed at 700°C was about $1x10^{-7}$ A/cm^2 at input voltage of 5V and decreased slightly with the values of about $5x10^{-8}$ A/cm^2 for the sample annealed at 750°C. This decrease of leakage current at the higher temperature may be attributed to the improved crystallinity during the post-annealing process.

The Pt/BLT/Y_2O_3/Si(100) FET devices using BLT ferroelectric gate thin film on Y_2O_3 buffer layer/ p-Si(100) substrates were fabricated.

The current values between source and drain at the bulk junctions of Pt/BLT/Y_2O_3/Si(100) FET were investigated as a function of the input voltages. The drain currents (I_D) were measured as a function of the drain voltages (V_D) at the gate voltage (V_G) of 1.0V and 1.2V, respectively.

Fig. 7 shows I_D versus V_D curves of Pt/BLT/Y_2O_3/Si(100) FET devices at V_G = 1.0V and 1.2V after input (a) V_G = +3V and (b) V_G = +4V for 100 msec, respectively. We found that there was very small amounts of drain currents at V_G = 1.0 V for both samples. However, I_D was greatly increased as V_D increased gradually at V_G = 1.2V. The I_D increased

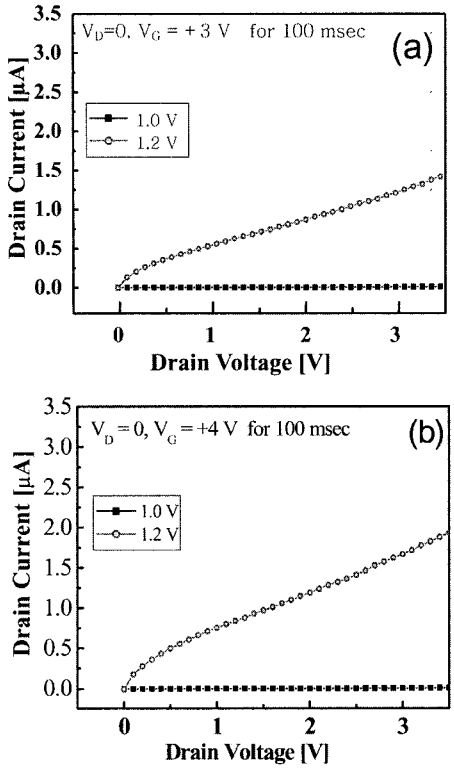

Fig. 7. Drain current versus drain voltages at gate voltage of 1.0V and 1.2V after input gate voltage (V_G) of (a) +3V and (b) +4V for 100 msec.

from 1.2 μA to 1.7 μA as the V_G increased from +3V to + 4V. It was confirmed that the current differences of $Pt/BLT/Y_2O_3/Si(100)$ FET device applied at V_G = +4V showed larger values than the one biased at V_G = +3V. This result suggests that the polarization was increased by increasing the input gate voltage, resulting in the increase of threshold voltage shift.

Fig. 8 shows the changes of drain current as a function of the gate voltages (V_G) for $Pt/BLT/Y_2O_3/Si(100)$ FET devices at the V_G of 3V, 4V and 5 V, respectively. The drain voltage was applied at 0.1V. From the I_D versus V_G data, the memory window voltages increased from 0.3V to 0.8V as V_G increased from 3V to 5V, indicating the maximum memory window voltage was about 0.8V at V_G = 5V. As a result, the memorized information between "1" or "0" writing states can be distinguished through

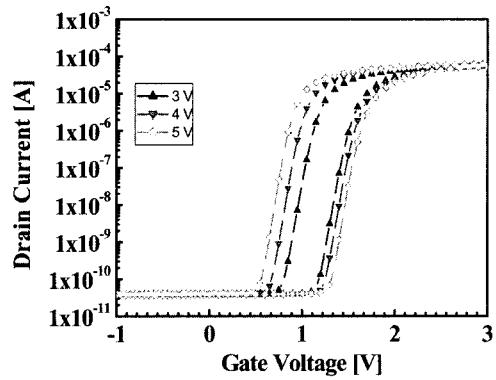

Fig. 8. Drain current versus gate voltages (I_D-V_G) of $Pt/BLT/Y_2O_3/Si(100)$ FET devices at various gate voltages (V_G) of 3V, 4V and 5V. The drain voltage (V_D) is 0.1V.

the drain current differences during the operation of memory device.

4. CONCLUSIONS

For the application of FRAM devices, the MFIS ($Pt/BLT/Y_2O_3/Si(100)$) FET devices using BLT ferroelectric gate thin film on Y_2O_3 buffer layer/p-Si(100) substrates were fabricated by the conventional memory processes and the sol-gel process. It was found that the capacitors with Pt/BLT/Pt/Si(100) structure showed no drastic degradation in polarization after the retention read pulses for $10^{5.5}$ seconds, showing a good fatigue property of the BLT films. From capacitance versus voltage characteristics at 5V, the memory window voltage of $Pt/BLT/Y_2O_3/Si$ (100) capacitors decreased from 1.4V to 0.6V with increasing the annealing temperature from 700°C to 750°C. The leakage current of the $Pt/BLT/Y_2O_3/Si$ (100) capacitors annealed at 750°C was about $5x10^{-8}$ A/cm^2 at 5V. From the drain current (I_D) as a function of gate voltages (V_G) for $Pt/BLT/Y_2O_3/Si(100)$ FET devices at V_G of 3V, 4V and 5V, the memory window voltages increased from 0.3V to 0.8V as V_G increased from 3V to 5V.

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