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1.8GHz 고주파 전단부의 결함 검사를 위한 새로운 BIST 회로

(A New Fault-Based Built-In Self-Test Scheme for 1.8GHz RF Front-End)

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요 약

본 논문에서는 1.8GHz 고주파 수신기 전단부의 결함 검사를 위한 새로운 저가의 BIST 회로(자체내부검사회로) 및 설계기술을 제안한다. 이 기술은 입력 임피던스 매칭 측정 방법을 이용한다. BIST 블록과 고주파 수신기의 전단부는 0.25m CMOS 기술을 이용하여 단일 칩 위에 설계되었다. 이 기술은 측정이 간단하고 비용이 저렴하며, BIST 회로가 차지하는 면적은 고주파 전단부가 차지하는 전체면적의 약 10%에 불과하다.

Abstract

This paper presents a new low-cost fault-based Built-In Self-Test (BIST) scheme and technique for 1.8GHz RF receiver front end. The technique utilizes input impedance matching measurement. The BIST block and RF receiver front end are designed using 0.25m CMOS technology on a single chip. The technique is simple and inexpensive. The overhead of the BIST circuit is approximately 10% of the total area of the RF front end.

Keywords : RF Front-End, BIST Scheme, input impedance matching

I. Introduction

Recently, there has been a proliferation of RF IC chips in many areas of consumer electronic products. RF circuits are widely used in data transmission, radios and mobile phone systems. The integration density and complexity of these devices increase with the increase in functionality. The test overhead is a very important component of the total cost of the system. In spite of the research underway to reduce test cost in RF ICs[1-8], the difficulties in testing still remain to be the major bottleneck of the product manufacturing. The problems come from the limited access to major components of the internal RF structures and the non-linear effects that RF faults may cause on a circuit under test[1, 5-8]. To solve these problems, the Built-In Self-Test (BIST) technique can be applied as the fundamental approach [1, 3-5, 7-10].

BIST techniques can be classified into two categories: functional and fault-based. The former apply traditional stimuli (e.g. sinusoidal or multi-tone waveforms) and measure the functional specifications of the circuit or block under test. Fault-based BIST techniques on the other hand are targeted towards detecting manufacturing faults and use

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non-conventional stimuli and signatures[8]. Several BIST schemes have been proposed, most of the BIST schemes test the analog blocks in a mixed-signal circuit via the digital-analog-digital path, unlike the analog-digital-analog path used by conventional external tests[3-5, 7]. Since the fault simulation and test for RF circuits are more complicated and time-consuming than those of analog and digital circuits, it is a crucial issue in the BIST approach[8].

Identification of catastrophic faults and parametric variations in an RF system forms an integral part of RF BIST. Analog systems have only a few inputs and outputs, and their internal states exhibit low time constants. From that follows, that a test with a high coverage is possible with small effort. A test resulting in a high coverage for catastrophic faults is possible using the standard approach based on current test stimulus and frequency domain measurements. However, according to Pleskacz et al [11], the standard approach based on current test stimulus covers only linear circuits. This approach is difficult when used to detect and diagnose spot defects that severely result in non-linear RF circuits implemented as CMOS or BiCMOS ICs[5]. The frequency domain measurement technique requires more test cost and time. To test point-to-point radios, loop back technique with BIST using spectral signature analysis is generally used with the lower effort and very small test overhead[3-5]. However, this test technique has disadvantages such as lower test coverage due to the fact that the complete transceiver is tested as a whole and the need of an additional DSP because of the higher complexity of the test signature generation[3-4]. R. Voorakaranam et al[6] showed gain, noise figure and IIP3 tests of 900MHz LNA using signature test with optimized test stimulus to test. This technique also requires additional off-chip signature response evaluator such as FASTest RF runtime system.

In this paper, a novel fault-based BIST scheme and technique for non-linear RF front end circuits using input impedance matching are presented. The RF front end and BIST circuits are integrated on a single chip using TSMC 0.25m CMOS technology. The BIST block consists of two test amplifiers and two summers. The transient voltage of the RF front end at the input is monitored to differentiate between faulty and fault-free circuits. This test technique requires only the use of digital voltmeter and RF voltage source generator. We present detailed catastrophic and parametric fault simulation results for RF front end with fault-free and faulty circuits using ADS simulation tool.

II. Fault-Based RF BIST Approach

Let us consider a small RF front end block that consists of Low Noise Amplifier (LNA) and differential mixer. Figure 1 shows proposed BIST scheme for a common RF chip. Our proposed test technique utilizes transient dc voltage and input impedance matching measurements using low-cost RF BIST block instead of conventional high-cost ATE test or membrane probe test to perform fault-based test. We designed a 1.8GHz LNA and double-balanced Gilbert-cell mixer for 1800DCS application. The BIST block consists of two inverting Test Amplifiers (TAs) and two summers. Our BIST part of the circuit had 10% additional chip area. The test set-up consists of the RF input source generator, common voltmeter and stable 50 ohm impedances for source and load matching.

The unilateral case for designed RF front-end is considered. In order to determine the error involved in

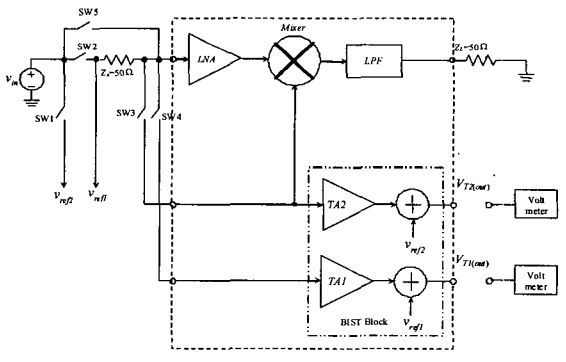

그림 1. 고주파 전단부의 검사를 위한 BIST 회로.
Fig. 1. Proposed BIST for RF front end.

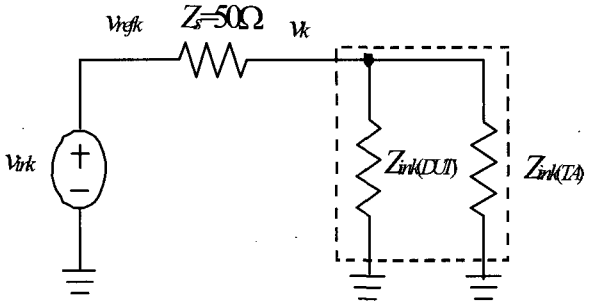

그림 2. 고주파 전단부 DUT와 검사용 증폭기의 입력 임피던스에 대한 테브난 등가회로.
Fig. 2. Thevnin equivalent circuit for the inputs of RF DUT and TA1 or TA2.

assuming $S_{12} = 0$, the magnitude ratio boundary of G_T and the unilateral power gain called G_{TU} can be introduced by open literature[12]. The value of U varies with frequency because of its dependence on the S-parameters. In designed good and faulty DUTs, the maximum error showed below 0.003dB at 1.8GHz. This error is so small enough to justify the unilateral assumption[12].

To provide the details of this technique, Figure 2 shows the Thevenin equivalent circuit for the inputs of the RF DUT and TA1 or TA2. We measure the transient dc voltage VTk(out) at the input as shown in Figure 1. The parameter k denotes LNA and mixer with 1 and 2, respectively.

The input impedances measurement for LNA and mixer is performed when the external switches S2 and S4 are in closed position to activate the LNA input, the switches S1 and S3 are in open position, and 50 ohm impedance for load matching is connected to LPF output port. Similarly, the measurement for mixer LO port is performed when the external switches S1 and S3 are in closed position to activate the mixer LO input, the switches S2 and S4 are in open position, and 50 ohm impedance for load matching is connected to LPF output port. The basic idea of the BIST scheme is to monitor the mismatch between the source impedance and input impedances of the RF chip under test and test amplifier. For example, the TA1 of Figure 1 looks for changes in input impedances of the LNA and mixer for any mismatch with the source impedance. In case of a mismatch due to a fault, the summation voltage of the amplifier and the input RF source is presented at the test output for an easy dc measurement. The TA2 performs the same function for detecting faults in the differential mixer. We neglect the influence on faults in BIST circuit

First, we consider fault-free LNA (or mixer) with good input matching condition. Considering this condition, the Equations (1) and (2) represent the theoretical values for the voltage across the input impedances of the LNA (or mixer).

$$V_{k(s)} = \frac{Z_{ink(DUT)} // Z_{ink(TA)}}{Z_s + (Z_{ink(DUT)} // Z_{ink(TA)}} V_{refk(s)} = \frac{Z_{ink(DUT)}}{2Z_{ink(DUT)} + 50\Omega} V_{refk(s)} \quad (1)$$

$$V_{Tk(out)} = V_{refk(rms)} - 3V_{k(rms)} \quad (2)$$

Inserting Equation (1) into (2), we have

$$V_{Tk(out)} = \frac{50\Omega - Z_{ink(DUT)}}{50\Omega + 2Z_{ink(DUT)}} V_{refk(rms)} \quad (3)$$

where

$$Z_{ink(DUT)} = Z_0 \left| \frac{1 + S_{11} - S_{22}\Gamma_L - S_{11}S_{22}\Gamma_L + S_{12}S_{21}\Gamma_L}{1 - S_{11} - S_{22}\Gamma_L + S_{11}S_{22}\Gamma_L - S_{12}S_{21}\Gamma_L} \right| \quad (4.1)$$

$$\Gamma_L = \frac{Z_L - Z_{0(\text{mixer})}}{Z_L + Z_{0(\text{mixer})}} = \frac{50\Omega - Z_{0(\text{mixer})}}{50\Omega + Z_{0(\text{mixer})}} \quad (4.2)$$

$Z_{ink(TA)} (= 50\Omega)$ is input impedance of TA1 or TA2, and $Z_{ink(DUT)}$ is input impedance of RF DUT or mixer at LO.

Because $\mathrm{Re}(Z_{ink(DUT)}) >> \mathrm{Im}(Z_{ink(DUT)})$ at 1.8GHz due to the good input matching condition, $|Z_{ink(DUT)}|$ and $V_{Tk(out)}$ are expressed as

$$Z_{ink(DUT)} = |Z_{ink(DUT)}| = \sqrt{[\mathrm{Re}(Z_{ink(DUT)})]^2 + [\mathrm{Im}(Z_{ink(DUT)})]^2} \approx \mathrm{Re}(Z_{ink(DUT)}) = 50\Omega \quad (5.1)$$

$$V_{Tk(out)} = 0 \quad (5.2)$$

Under faulty condition, we need to consider phase shift in input impedance of RF DUT. Thus, the voltage

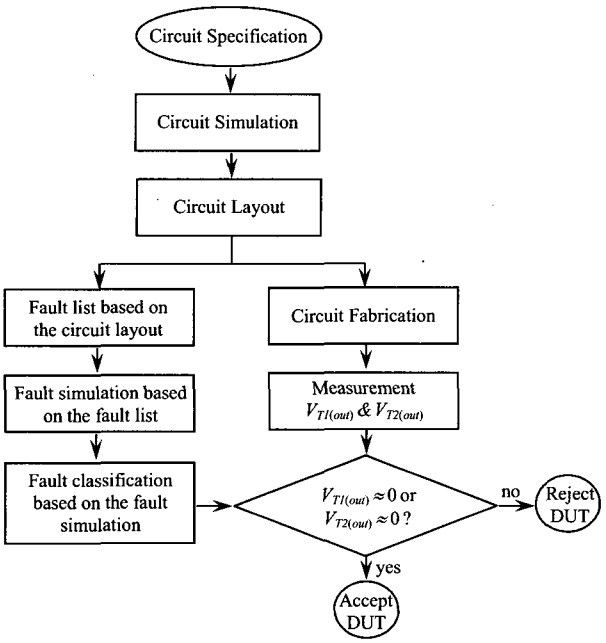

그림 3. 고주파 전단부 DUT에 대한 시험 방법 순서도.
Fig. 3. Flowchart of the procedure of test method for RF DUT.

$V_{Tk(out)}$ is in non-zero dc value because $v_{k(rms)} \neq (1/3)v_{refk}$ due to a mismatch, i.e. $Z_{ink(DUT)} \neq 50\Omega$. If $Z_{ink(DUT)} < 50\Omega$, the BIST block displays transient dc output of $V_{Tk(out)} < 0$ at a given time interval as compared to fault-free case from Equation (3). Similarly, if $Z_{ink(DUT)} > 50\Omega$, the BIST block displays $V_{Tk(out)} > 0$ at the same condition.

Since the fault simulation and test for RF circuits are more complicated and time-consuming than those of analog and digital circuits, it is a crucial issue in the BIST approach. Once chips are fabricated, simple comparison or some sophisticated techniques for fault detection can be applied to identify good chips from faulty chips. Figure 3 shows the flowchart of the procedure of test method for RF DUT.

Ⅲ. Fault Models and Fault Simulation

Both catastrophic faults and parametric faults are considered for MOSFETs and passive components as shown in Figures 4 and 5, respectively. The catastrophic fault models consist of open faults (OF) or resistive breaks, short faults (SF) or resistive bridges [5, 13] and single GOS (gate-oxide short) faults. Spot defects are typical faults of mass production in CMOS process[5], and GOS faults are the most common defects in CMOS ICs[14]. As shown in Figure 4(d), the GOS model described in [14] essentially divides the MOSFET into two devices with modified channel lengths (L1 and L2), interconnected by a diode and shunt resistor. We consider five different catastrophic faults for the MOSFET such as drain-to-source Short Fault, gate-to-drain (GD) SF, GO SF, gate-to-source (GS) SF and Open Fault (OF). Two different types of fault models of passive components are used for fault simulations. The first model of an inductor[1, 13] is shown in Figure 5. The models of resistor and capacitor follow fault models shown in Figure 5. As the second model, open fault resistor and inductor have approximately 10 times of given values, and short fault resistor and inductor have approximately 0.1 times of given values. For a capacitor, open faults have approximately 0.1 times of given value, and short faults have approximately 10 times of given value[15]. We considered 10% to 50% variation in passive components including resistors, capacitors and inductors, and 20% to 50% width variation in MOSFETs for simulation of parametric faults by unusual process variations[1,15]. A total of 192 different fault models are considered. Amongst them are fault-free model, 81 different catastrophic fault models and 110 different parametric fault models.

In addition to inserting catastrophic faults into the simulations, we also performed Monte Carlo simulations and sensitivity analysis. Monte Carlo analysis is performed to ensure that no parametric faults can mask catastrophic faults. If the range of response of a catastrophically faulty circuit is indiscernible from the fault-free case, then the parametric fault will mask the catastrophic fault. We have considered variable process parameters such as oxide thickness, surface mobility, junction depth, substrate doping, threshold voltage, transistor lengths, and transistor widths for Monte Carlo analysis. Each of the device model parameters listed above was

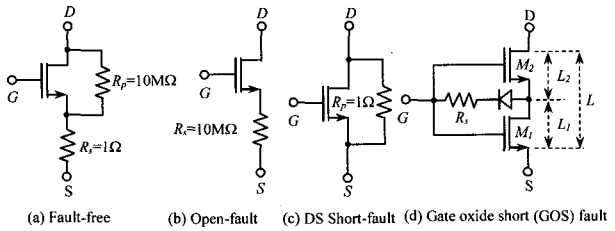

그림 4. MOSFETs의 결함모델.
Fig. 4. Fault models of MOSFETs.

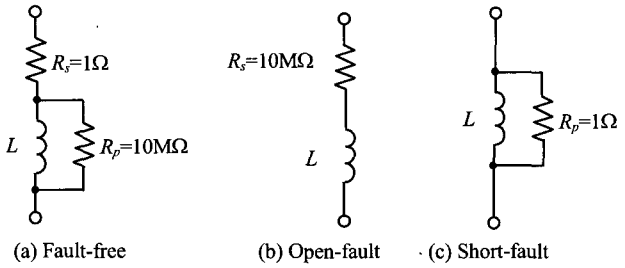

그림 5. 수동 소자의 결함 모델.
Fig. 5. Fault models of passive components.

randomly perturbed with a Gaussian distribution from one simulation to the next. The distribution of the Gaussian random variables was selected at 10% of nominal at 3σ.

Ⅳ. RF Device Under Test

The LNA and mixer used in the fault simulations are shown in Figure 6. This RF DUT is designed to verify the proposed BIST approach. They are designed for DCS1800 application operating at 1.8GHz, and have supply voltage of 2.5V. The RF front end is integrated on a single chip using TSMC 0.25m CMOS technology.

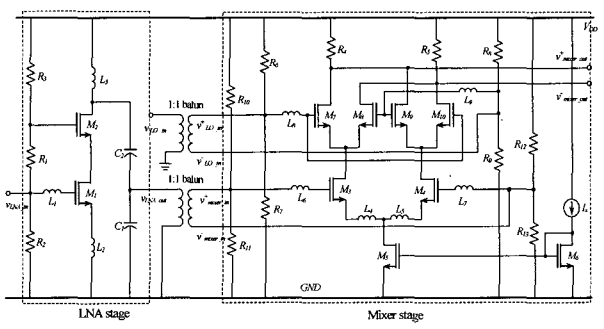

그림 6. LNA와 이중 대칭구조를 가진 Gibert-cell 믹서에 대한 회로도.
Fig. 6. Schematic diagram of LNA and double-balanced Gilbert-cell mixer.

The mixer has double-balanced Gilbert-cell topology.

Ⅴ. Test Results

In these results the impact of faults in BIST circuit itself was neglected. The input RF sinusoidal signal v_{in} with peak amplitude of 200mV and frequency of 1.8GHz was applied as an input stimulus to verify proposed BIST.

1. Faults Results at LNA Stage

Figures 7(a) and (b) show fault simulation results of the LNA stage. The $V_{T1(out)}$ response shows that the fault-free LNA response has almost all dc as compared to other faults as shown in Figure 7(a). However, faulty circuits showed amplitude variations and phase shifts between $-\pi/8$ and $+\pi/8$ because input impedance is changed due to the mismatch under faulty condition. As shown in Figure 7(a), short fault of resistor R_1 (connected to test input port directly) of

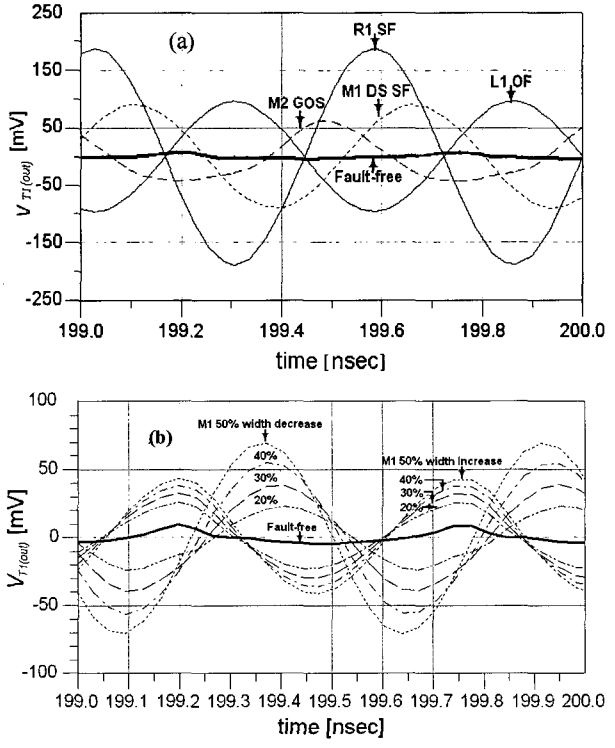

그림 7. 고주파 전단부의 LNA단에 대한 결함 검출 결과 (a) 거폭결함 (b) 미세결함.
Fig. 7. Fault simulation results for LNA stage in RF front end: (a) Catastrophic faults (b) Parametric faults.

bias circuit showed the largest amplitude variation. As we can expect, faults of components connected to input port had larger amplitude variations than those connected to output port as shown in Figure 7(a). We can therefore detect various faults by observing the different levels of amplitude variations. Using an accurate phase meter or oscilloscope, it is possible to diagnose all faults.

As an example of parametric fault, the fault for transistor M_1 is shown in Figure 7(b). The ±20% to ±50% width variation in transistor M_1 is considered. These results showed small variations when compared to catastrophic faults as shown in Figure 7(b). Increase in % width variation of transistor M_1 has the phase difference of $3\pi/4$ with decrease in % width variation of this transistor. The ±10% width variation in transistor M_1 was considered as an acceptable variation. It is shown that all of these faults have detectable amplitudes and phase shifts. These results can be calculated and verified using Equations (1) to (5), and measuring input impedances of the RF DUT.

2. Faults Results at Mixer Stage

Figures 8(a) and (b) show catastrophic fault simulation results for mixer RF stage and LO stage in RF front end. From Figures 8(a) and (b), fault-free mixer has dc response compared to other faults. However, faulty circuits showed amplitude variations and phase shifts between $-\pi/2$ and $+\pi/2$. Each fault tested had different amplitude variations and phase shifts. We can use an accurate phase meter or oscilloscope to diagnose all faults in the mixer stage. As shown in Figure 8, short fault of resistor R_{12}(connected to mixer input port directly) of bias circuit of mixer showed the largest amplitude variations. These results can also be verified and calculated using equations (1) to (5), and measuring input impedances of RF DUT.

3. Results Summary

We tested 81 different catastrophic faults in the RF front end of the receiver. Figure 9 shows percent error test results for catastrophic faults of all components in

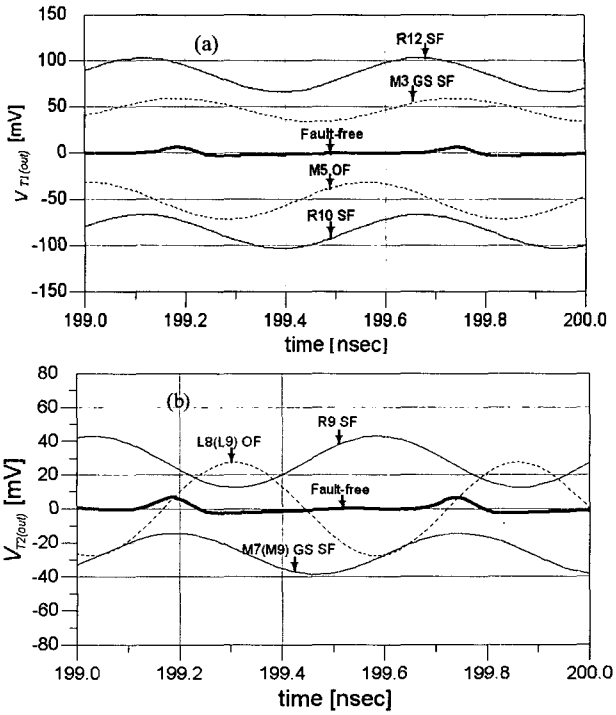

그림 8. 고주파 전단부의 믹서단에 대한 거폭 결함 검출 결과. (a) 믹서 고주파단에서의 결함 (b) 믹서 LO단에서의 결함.

Fig. 8. Catastrophic fault simulation results of mixer stage in RF front end: (a) Faults in mixer RF stage (b) Faults in mixer LO stage.

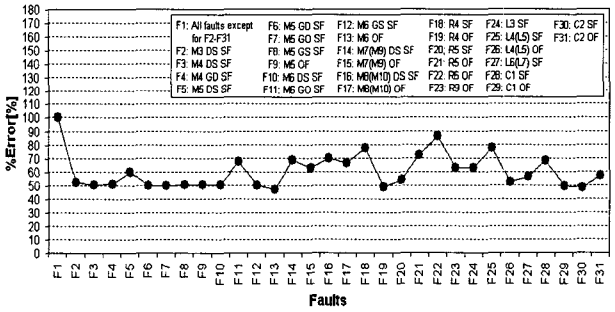

그림 9. 고주파 전단부에 사용된 모든 결함에 대한 퍼센트 오차.

Fig. 9. Faults vs. percent error of all components in RF front end.

RF front end. As shown in Figure 9, most of the faults showed percent error of more than 50%, and 51 faults had percent error of more than 100%.

Table 1 lists fault coverage for each component of RF front end. For 81 different catastrophic fault models, our proposed testing technique showed 100% fault coverage. For 110 different parametric fault models, we had fault coverage of about 90%. Table 2 shows list of partial values of input impedances of the

표 1. 고주파 DUT의 각 소자에 대한 결함 검출.
Table 1. Fault coverage for each component of RF DUT.

Faults / Components	Fault coverage [%]		
	Catastrophic Faults		Parametric Faults
	OF (# of faults)	SF (# of faults)	(# of faults)
MOSFETs	100 (8)	100 (31)	89 (20)
Resistors	100 (13)	100 (13)	100 (32)
Capacitors	100 (2)	100 (2)	100 (16)
Inductors	100 (6)	100 (6)	78 (42)
Total	100 (29)	100 (52)	89.6 (110)

표 2. 입력 임피던스에 대한 비교 결과(Ω).
Table 2. Compared results for input impedances (Ω).

Faults	External Equipment Test	Proposed On-Chip Test
Fault-free	51.69	47.62
M_1 Gate Open	4780	614.2
M_1 S-D Short	22.61	30.01
L_1 + 30%	59.54	58.54
L_1 + 40 %	64.24	63.18
L_1 + 50%	69.67	69.79

1.8GHz LNA and these values are compared with real measurement values. As can be seen from the table, input impedances measured by the On-Chip Test circuit were close to the external equipment measurements.

VI. Conclusions

This paper proposed a novel fault-based test technique for RF front end with built-in self-test hardware using input impedance matching. The RF front end and BIST block were designed using TSMC 0.25m CMOS technology. The BIST circuit consisted of two inverting amplifiers and two summers. As compared to the standard approach based on frequency domain measurement, this technique requires only use of a common RMS voltmeter and RF voltage source generator. We believe that this test technique is simple and inexpensive. Our BIST hardware had about 10% overhead.

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