

PLC 입력 인코딩 모듈 설계에 관한 연구

(Study On Design of Encoding Module for PLC input)

유정봉*

(Jeong-Bong You)

요 약

여러 제어기 중에서 PLC가 공장자동화 설계에서 가장 많이 사용되고 있으며, PLC 언어에 대한 연구도 활발히 이루어지고 있다. 본 논문에서는 PLC를 사용한 공장자동화 설계에서 입력 기기의 수가 증가되었을 때 입력을 확장하는 인코딩 모듈을 제안한다. 기본 베이스에 입력 유닛을 더 이상 장착할 수 없는 상태에서 입력 점수를 2~3점 확장하고자 한다면, 증설 베이스와 파워서플라이, 증설케이블 및 출력 유닛을 별도로 장착하여야 한다. 그러면 비용이 상당히 추가되어야 한다. 본 논문에서는 입력을 소량을 확장할 수 있는 입력 인코딩 모듈을 제안하고, 시뮬레이션을 통해 그의 타당성을 확인하였다.

Abstract

Programmable Logic Controller(PLC) is the most widely utilized among many sorts of existing controller for the design of factory automation control system, and study about a PLC language is performed actively. In this paper, we proposed the encoding module that we increase input points when increased of the input machine which is going to control it in the FA design that used PLC. Input point is going to be extended with 2-3 points in the state that cannot equip input unit in basic base any more. Then an extension base, a power supply, an extension cable and an output unit must be equipped particularly. Then a cost must be added very much. This paper proposed the encoding module which extended an input in a small quantity, and we confirmed a feasibility through a simulation.

Key Words : PLC, Ladder diagram, Encoding module, Input unit, Decoder

1. Introduction

From the PLC(Programmable Logic Controller) be developed, the PLC became indispensable equipment in the factory automation control. This can deal with an input and output of a large scale, and it can be linked by a communication network devoted to an organic connection between

* 주저자 : 공주대학교 전기전자공학부 조교수

Tel : 041-550-0169, Fax : 041-563-3689

E-mail : jbyou@kongju.ac.kr

접수일자 : 2005년 3월 30일

1차심사 : 2005년 4월 4일

2차심사 : 2005년 4월 20일

심사완료 : 2005년 4월 29일

processes[1-3].

As for the PLC, it is used a standard language offered to international standards of IEC-1131-3. A standard language of PLC is a text base of IL(Instruction List), ST(Structured Text) and a graphical base language of LD(Ladder Diagram), FBD (Function Block Diagram), SFC(Sequential Function Chart)[4].

Hardware of PLC is divided into block -type PLC and module-type PLC.

A block-type PLC is having all functions in one block all ; power unit, CPU, memory, input/output unit etc.

However, the expansibility is bad because block-type PLC must add an expansion unit to extend a function and input/output points.

A module-type PLC must adds to a module to have a lot of function toward main base as necessary and basic units are installed toward main base ; power unit, CPU unit, input/output unit etc.

Also, a module-type PLC is very used as a controller on middle scale because the extension of input and output points is convenient[5-6].

In control system with PLC, if we can add input unit to main base to extend input points because

of the spare, the extension of input points is convenient.

However, if there is not the spare that can be extended input points in input unit, an input unit must be added.

For example, an input unit must be added if 5 points of input equipment must be added when input unit covers 3 points of addition spares, and it must be done.

Because a base and a power unit must be added if some input points must be added when there is not a margin to add unit to basic base either, it is much increase a cost.

In order to overcome this advantage, this paper proposed the encoding module for PLC input and the program module that can extend input points in the input unit which can not be added input points and we confirmed his feasibility through a simulation.

2. An Encoding Module Design

2.1 Configuration of system

The system that equipped input and output unit for expansion is shown in fig.1.

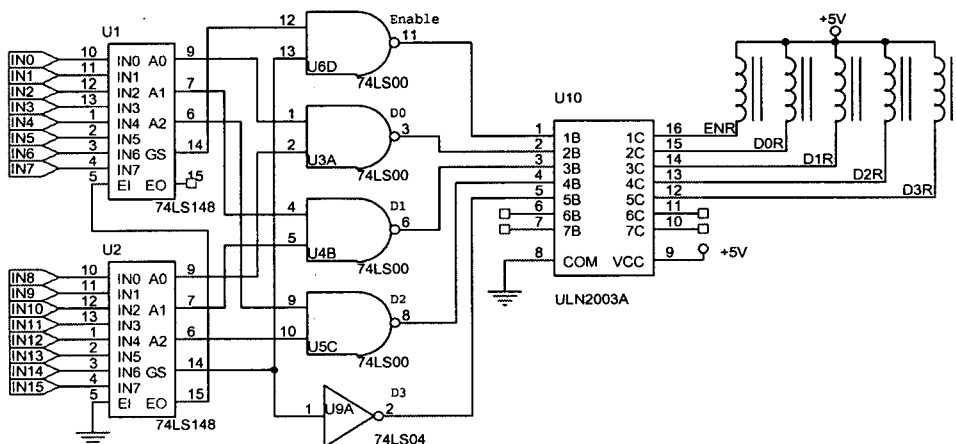


Fig. 2. Encoding Module for Input

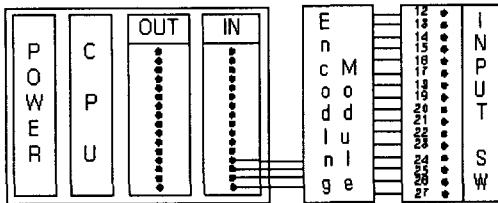


Fig. 1. Construction of System for Expansion

When 16 points of input unit was equipped in main base in fig.1, 4 bit (No.15~No.12 points) is used at a point for expansion. The No.11 point is used at an enable signal. When an input unit is not extended, input points can use a general points.

If be equipped the encoding module for expansion and extend 16 points, we propose 4 bit of an input unit(No.15~No.12 point) by an input in encoding module. Therefore, 28 input points are usable from a No. 0 point to a No. 27 point with input unit.

2.2 Encoding Module for input

We accept 16 switches by an encoding module and generate an output signal of an encoding output $D_3 \sim D_0$. A circuit of encoding module is shown in fig.2.

2.3 7-Segment Display

A 7-segment receives the four signal generated in encoding module, and displays the number of point.

The switch input of encoding module use 16 points from a No.12 to a No.27.

Therefore, it is marked that the input number of each point is displayed with 7-segment to two positions.

(1) High-rank (S2) 7-Segment

In a table 1, high rank 7-segment displays '1' when it receives from a No.12 to a No 19, and

displays '0' when it receives from a No.20 to a No.27.

In a table 1, the input of 1,2,4,8 of high rank segment decoder 74LS47 is represented by an equation (1).

$$\begin{aligned} a &= \overline{D_3}, \quad b = D_3 \\ c &= d = 0 \end{aligned} \tag{1}$$

(2) Low rank (S1) 7-Segment

In a table 1, the input of 1,2,4,8 of low rank segment decoder 74LS47 is represented by an equation (2).

Table 1. Value of Decoding

| SW No. | Decoding Signal | High rank (S2) | Low rank (S1) |
|--------|-----------------|----------------|---------------|
| | DCBA | dcb a | dcba |
| 12 | 0000 | 0001 | 0010 |
| 13 | 0001 | 0001 | 0011 |
| 14 | 0010 | 0001 | 0100 |
| 15 | 0011 | 0001 | 0101 |
| 16 | 0100 | 0001 | 0110 |
| 17 | 0101 | 0001 | 0111 |
| 18 | 0110 | 0001 | 1000 |
| 19 | 0111 | 0001 | 1001 |
| 20 | 1000 | 0010 | 0000 |
| 21 | 1001 | 0010 | 0001 |
| 22 | 1010 | 0010 | 0010 |
| 23 | 1011 | 0010 | 0011 |
| 24 | 1100 | 0010 | 0100 |
| 25 | 1101 | 0010 | 0101 |
| 26 | 1110 | 0010 | 0110 |
| 27 | 1111 | 0010 | 0111 |

$$\begin{aligned} a &= D_0, \quad b = \overline{D_3} D_1 + D_3 D_1 \\ c &= D_2 \overline{D_1} + D_3 D_2 + \overline{D_3} \overline{D_2} D_1 \\ d &= \overline{D_3} D_2 D_1 \end{aligned} \tag{2}$$

The circuit that was designed by equation (1) and equation (2) is shown in Fig.3.

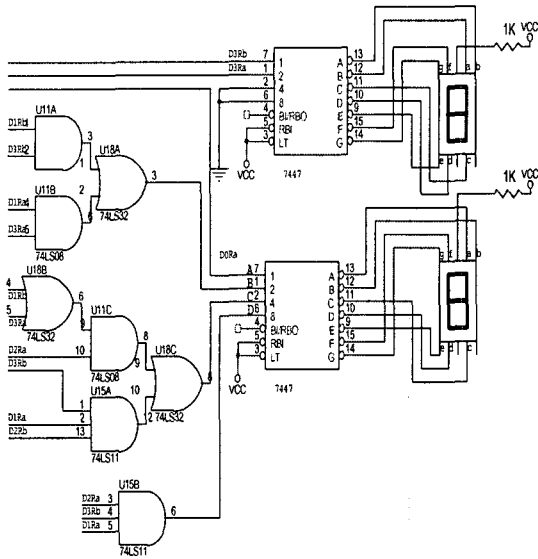


Fig. 3. Display of 7-Segment

3. A Program Module Design

An example was adopted with a system composed with one input unit providing 16 points and one output unit providing 16 points in main base, and a program module was designed.

The flow chart of program module is shown in fig.4.

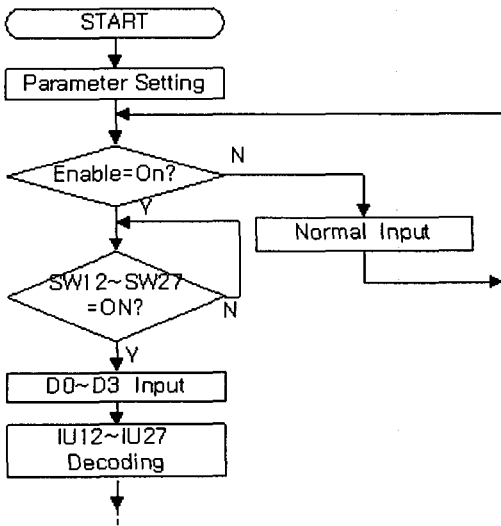


Fig 4. Flow chart of Program Module

In fig 4, if an enable signal is detected, the encoding module activates. And the input unit can be extended with from Sw12 to Sw27.

Therefore, the input unit uses 31 points. PLC is received the signal of $D_0 \sim D_3$ and decodes from IU_{12} to IU_{27} .

The value of decoding from IU_{12} to IU_{27} is same as equation (3).

$$\begin{aligned}
 IU_{12} &= \overline{D_3} \cdot \overline{D_2} \cdot \overline{D_1} \cdot \overline{D_0} \\
 IU_{13} &= \overline{D_3} \cdot \overline{D_2} \cdot \overline{D_1} \cdot D_0 \\
 IU_{14} &= \overline{D_3} \cdot \overline{D_2} \cdot D_1 \cdot \overline{D_0} \\
 IU_{15} &= \overline{D_3} \cdot \overline{D_2} \cdot D_1 \cdot D_0 \\
 IU_{16} &= \overline{D_3} \cdot D_2 \cdot \overline{D_1} \cdot \overline{D_0} \\
 IU_{17} &= \overline{D_3} \cdot D_2 \cdot \overline{D_1} \cdot D_0 \\
 IU_{18} &= \overline{D_3} \cdot D_2 \cdot D_1 \cdot \overline{D_0} \\
 IU_{19} &= \overline{D_3} \cdot D_2 \cdot D_1 \cdot D_0 \\
 IU_{20} &= D_3 \cdot \overline{D_2} \cdot \overline{D_1} \cdot \overline{D_0} \\
 IU_{21} &= D_3 \cdot \overline{D_2} \cdot \overline{D_1} \cdot D_0 \\
 IU_{22} &= D_3 \cdot \overline{D_2} \cdot D_1 \cdot \overline{D_0} \\
 IU_{23} &= D_3 \cdot \overline{D_2} \cdot D_1 \cdot D_0 \\
 IU_{24} &= D_3 \cdot D_2 \cdot \overline{D_1} \cdot \overline{D_0} \\
 IU_{25} &= D_3 \cdot D_2 \cdot \overline{D_1} \cdot D_0 \\
 IU_{26} &= D_3 \cdot D_2 \cdot D_1 \cdot \overline{D_0} \\
 IU_{27} &= D_3 \cdot D_2 \cdot D_1 \cdot D_0
 \end{aligned}
 \tag{3}$$

4. Experimental Results

For experiment, we used PLC which was a GLOFA GM4 model of LG industry and we confirmed his feasibility through experiment. [6-7]

An PLC set for experiment is shown in Fig.5. If PLC is received more than one among SW12~SW27, the encoding module encodes the value of SW. And the value of encoding is D_3, D_2, D_1, D_0 .

The point of D_3, D_2, D_1, D_0 enable the expansion module. This program is shown Fig. 6.

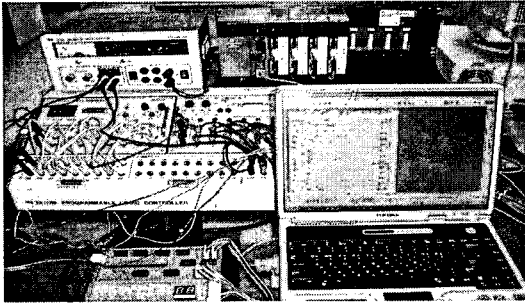


Fig. 5. PLC set for Experiment

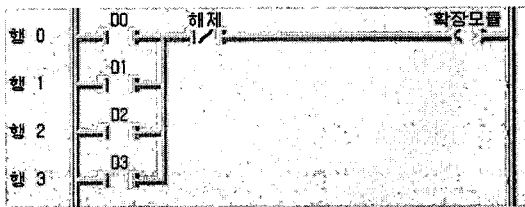


Fig. 6. Points of Encoding

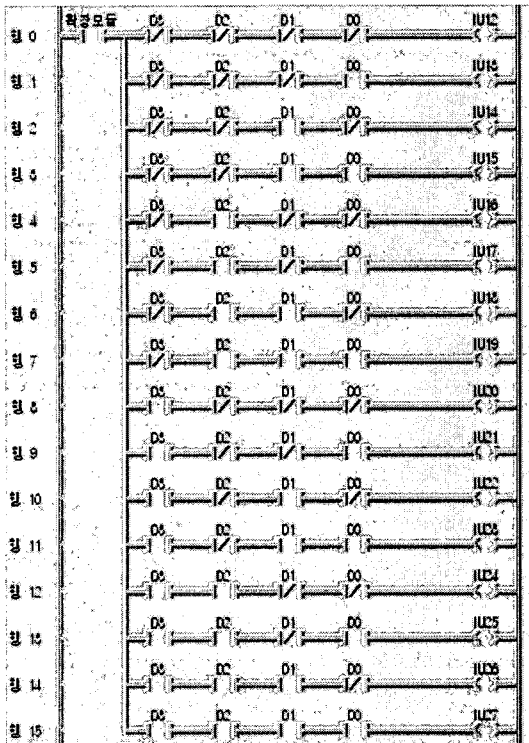


Fig. 7. Points of Input Decoding

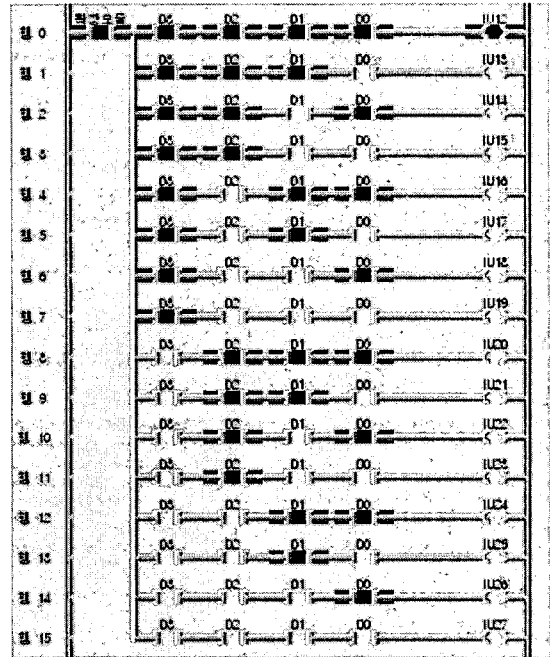
In Fig. 6, the point of D_3 , D_2 , D_1 , D_0 is decoded and allocated in internal memory.

This program is shown in Fig. 7.

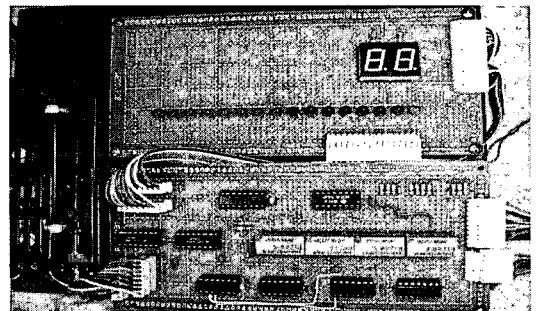
In Fig. 8, we confirmed an activity of PLC.

When SW12 of encoding module input is turned on, we can see that the IU_{12} is turned on in Fig. 8(a)

And we can see that the first LED is turned on and 7-segment displays the number.



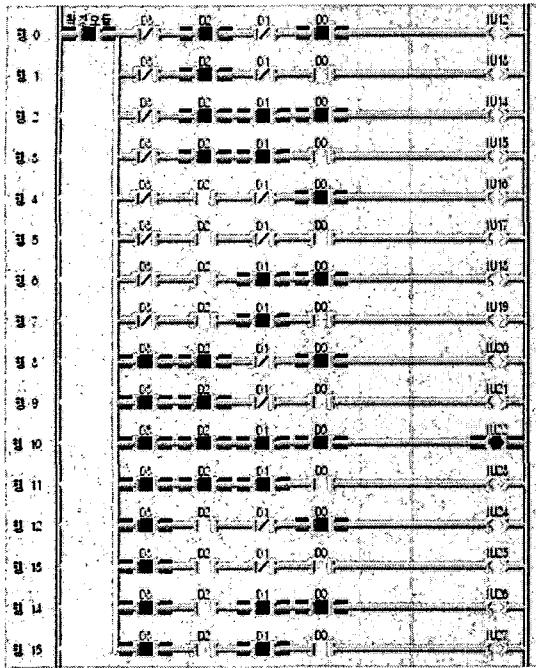
(a) Monitoring



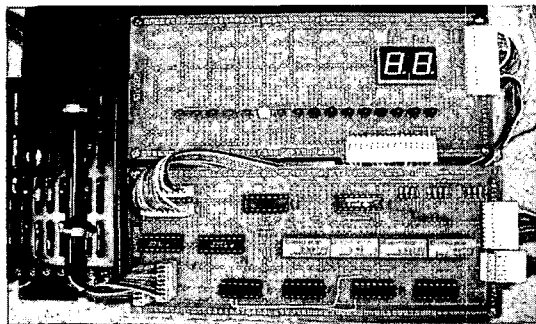
(b) Encoding Module

Fig. 8. When SW0 is turned On

Also, when SW22 is turned on, we can see that the IU_{22} is turned on in Fig.9,



(a)Monitoring



(b) Encoding Module

Fig. 9. When SW22 is turned On

5. Conclusion

In this paper, we proposed the method that we could extend input points by using the encoding module. And we confirmed his feasibility through a simulation. An input unit is extended to 31 points from 16 points by the encoding module. When we program the control system program and debug the control program with PLC, the proposed method is very efficiently usable.

In this paper, PLC of a LG GLOFA GM4 model was used and it was done a simulation. If the value of parameter is changed adequately, it can be used in all PLC.

References

- (1) IAN G. Warnock, "Programmable Controllers Operation and Application", Prentice Hall, 1992.
- (2) Bong-Suk Kang and Kwang-Hjun Cho, "Synthesis of Ladder Diagrams for PLCs Based on Discrete Event Models", Journal of Control, Automation and systems Engineering, Vol 7. No11, p939-943, Nov, 2001.
- (3) K.-H. Cho and J.-T. Lim, "Multiagent supervisory control for anti-fault-propagation in serial production systems," IEEE Trans. on Industrial Electronics, vol. 48, no. 2, pp460-466, 2001.
- (4) R.W.Lewis, "Programming Industrial Control Systems Using IEC1131-3", The Institution of Electrical Engineers, 1992.
- (5) M. Zhou and E Twiss, "Design of Industrial automated systems via relay ladder logic programming and Petrinets", IEEE Trans on Systems, Man and Cybernetics-part C : Applications and Reviews, Vol 28, No 1, pp 137- 150, 1998.
- (6) "Mitsubishi PLC Programming Manual", Mitsubishi, QnA series, 2004.
- (7) "LG Programmable Logic Controller Glofa-GM", LG Industrial Systems, 2004.

◇ 저자소개 ◇

유정봉 (庾正鳳)

1964년 3월 5일생. 1988년 2월 단국대학교 전자공학과 졸업. 1990년 8월 동대학원 전자공학과 졸업(석사). 1998년 8월 동대학원 전자공학과 졸업(박사). 1990년 7월~1993년 9월 (주)신도리코. 현재 공주대학교 전기 전자공학부 조교수. 주요관심분야는 PLC 제어, 마이크로프로세서 제어, BLDC 모터 제어, 디스플레이 장비 공장자동화 알고리즘 설계 등.