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공간-주파수 OFDM 전송 다이버시티 기법 기반 무선 LAN 기저대역 프로세서의 구현

(Implementation of WLAN Baseband Processor Based on Space-Frequency OFDM Transmit Diversity Scheme)

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요 약

본 논문에서는 공간-주파수 OFDM (SF-OFDM) 기법을 위한 효율적인 심볼 검출 알고리즘이 제안되고, 이를 기반으로 하는 SF-OFDM 무선 LAN 기저대역 프로세서의 구현 결과가 제시된다. SF-OFDM 기법에서 부반송파의 개수가 적은 경우 부채널간 간섭이 발생하게 되며, 이러한 간섭은 다이버시티 시스템의 성능을 크게 저하시킨다. 제안된 알고리즘은 부채널간 간섭을 병렬적으로 제거함으로써 기존 알고리즘에 비해 큰 성능 이득을 얻는다. 컴퓨터 모의실험을 통한 비트오류율 (BER) 성능 평가 결과, 두개의 송·수신 안테나를 사용하는 경우 10-4의 BER에서 기존 알고리즘에 비해 약 3 dB의 성능이득을 얻음을 확인하였다. 제안된 심볼 검출 알고리즘이 적용된 SF-OFDM 무선 LAN 시스템의 패킷오류율 (PER), link throughput 및 coverage 성능이 분석되었다. 최대 전송률의 80%를 목표 throughput으로 설정 했을 때, SF-OFDM 기반 무선 LAN 시스템은 기존의 IEEE 802.11a 무선 LAN 시스템에 비해 약 5.95 dB의 SNR 이득과 3.98 미터의 coverage 이득을 얻을 수 있었다. 제안된 알고리즘이 적용된 SF-OFDM 무선 LAN 기저대역 프로세서는 하드웨어 설계 언어를 통해 설계되었으며, 0.18um 1.8V CMOS 표준 셀 라이브러리를 통해 합성되었다. 제시된 division-free 하드웨어 구조와 함께, 구현된 프로세서의 총 게이트 수는 약 945K개였으며, FPGA 테스트 시스템을 통해 실시간 검증 및 평가되었다.

Abstract

In this paper, we propose an efficient symbol detection algorithm for space-frequency OFDM (SF-OFDM) transmit diversity scheme and present the implementation results of the SF-OFDM WLAN baseband processor with the proposed algorithm. When the number of sub-carriers in SF-OFDM scheme is small, the interference between adjacent sub-carriers may be generated. The proposed algorithm eliminates this interference in a parallel manner and obtains a considerable performance improvement over the conventional detection algorithm. The bit error rate (BER) performance of the proposed detection algorithm is evaluated by the simulation. In the case of 2 transmit and 2 receive antennas, at BER=10^{-4} the proposed algorithm obtains about 3 dB gain over the conventional detection algorithm. The packet error rate (PER), link throughput, and coverage performance of the SF-OFDM WLAN with the proposed detection algorithm are also estimated. For the target throughput at 80% of the peak data rate, the SF-OFDM WLAN achieves the average SNR gain of about 5.95 dB and the average coverage gain of 3.98 meter. The SF-OFDM WLAN baseband processor with the proposed algorithm was designed in a hardware description language and synthesized to gate-level circuits using 0.18um 1.8V CMOS standard cell library. With the division-free architecture, the total logic gate count for the processor is 945K. The real-time operation is verified and evaluated using a FPGA test system.

Keywords: Space-Frequency OFDM transmit diversity scheme, symbol detection, WLAN.

I. Introduction

The tremendous growth in WLANs has generated much interest in technologies that provide higher data rates and greater system capacities. The current IEEE 802.11a standards, based on coded orthogonal frequency division multiplexing (COFDM), support up to 54Mb/s transmission rate at 5GHz band. However, high-speed internet, video, and multi-media applications have created a need for even higher

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bandwidth efficiency and reliability from the next generation WLAN system[1].

Recently, the multiple transmit and receive antenna schemes have been proposed as an efficient solution for future wireless systems. Among them, transmit diversity schemes have shown a high potential for the greatly improved system performance over flat fading channels with reasonable complexity[2].

A number of orthogonal transmit diversity schemes have been proposed[3]-[4]. However, the large delay spreads in non-flat fading channels such as frequency-selective multi-path channels destroy the orthogonality of the received signals, which is a critical factor for the reliable operation of the diversity systems. Using orthogonal frequency division multiplexing (OFDM), the channel impulse response can be considered to be flat within each sub-carrier. Therefore, transmit diversity schemes with OFDM can be effectively used in non-flat fading channels.

Two transmit diversity schemes with OFDM, the space-time OFDM (ST-OFDM) and the space-frequency OFDM (SF-OFDM), are described in [5] and [6], respectively. In the ST-OFDM scheme, since adjacent OFDM symbols are encoded for the diversity gain, good performance is obtained over slow fading channel such as in an indoor environment. However, encoding between OFDM symbols results in large encoding and decoding processing delays which are not compliant with the short inter-frame space (SIFS) timing requirements for IEEE 802.11 MAC protocol's acknowledgement packet[7]. In the case of the SF-OFDM scheme, due to encoding among adjacent sub-carrier symbols, small delays are obtained in the encoding and decoding processing[8]. However, for the performance gain, SF-OFDM requires a large number of sub-carriers, typically 512 or 1024[9]. Therefore, the SF-OFDM scheme is not adequate for the systems with a few sub-carriers such as WLANs.

In this paper, we propose an efficient symbol detection algorithm for the SF-OFDM scheme and present the implementation results of the SF-OFDM WLAN baseband processor with the proposed algorithm. By eliminating the interference caused by a few sub-carriers, the proposed detection algorithm shows a considerable performance improvement over the conventional detection algorithm. Also, the SF-OFDM WLAN system with the proposed algorithm supports a better throughput and coverage performance than the conventional IEEE 802.11a system.

This paper is organized as follows. In Section II, the system model with SF-OFDM transmit diversity scheme is introduced, and the proposed detection algorithm is described in Section III. Performance analysis results such as PER, link throughput, and coverage are shown in Section IV, and implementation results of the SF-OFDM WLAN baseband processor with the proposed algorithm are presented in Section V. Finally, Section VI concludes the paper.

II. System Model

In this paper, we consider two-branch SF-OFDM transmit diversity scheme as the convenient benchmarking case. However, the proposed algorithm can be extended to other transmit/receive antenna cases. A block diagram of the two-branch SF-OFDM system is shown in Fig. 1.

Consider two adjacent sub-carriers k and $k+1$ (k=0, 2, 4,$\cdots$, N-2) for transmission. For the sub-carrier k, $X_{k,1}=X_k$ and $X_{k,2}=X_{k+1}$ are transmitted from transmit antenna 1 (TX1) and antenna 2 (TX2), respectively; for sub-carrier $k+1$, $X_{k+1,1}=-X_{k+1}^*$ and $X_{k+1,2}=X_k^*$ are transmitted from TX1 and TX2, respectively.

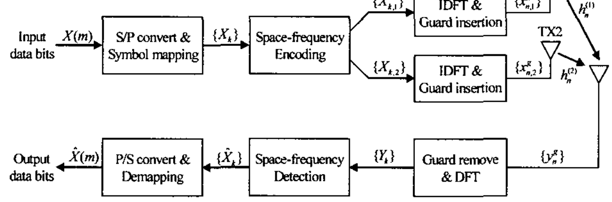

그림 1. Two-branch SF-OFDM 시스템의 블록도
Fig. 1. Block diagram of two-branch SF-OFDM system.

With perfect synchronization, the discrete Fourier transform (DFT) outputs at the receiver for sub-carriers k and k+1 are given by

$$Y_k = H_k^{(1)} \cdot X_k + H_k^{(2)} \cdot X_{k+1} + N_k \tag{1}$$

$$Y_{k+1} = H_{k+1}^{(1)} \cdot (-X_{k+1}^*) + H_{k+1}^{(2)} \cdot X_k^* + N_{k+1}, \tag{2}$$

where $H_k^{(i)}$ with $i \in \{1, 2\}$ denotes the DFT of the channel impulse response from transmit antenna i to the receiver and N_k denotes the DFT of AWGN. After conjugating (2), the DFT outputs can be written in the matrix notation,

$$\begin{aligned} \mathrm{Y} &= \begin{pmatrix} Y_k \\ Y_{k+1}^* \end{pmatrix} = \begin{pmatrix} H_k^{(1)} & H_k^{(2)} \\ H_{k+1}^{(2)*} & -H_{k+1}^{(1)*} \end{pmatrix} \cdot \begin{pmatrix} X_k \\ X_{k+1} \end{pmatrix} + \begin{pmatrix} N_k \\ N_{k+1}^* \end{pmatrix} \\ &= \mathbf{H} \cdot \mathbf{X} + \mathbf{N} \end{aligned} \tag{3}$$

Assuming that the complex channel gains between adjacent sub-carriers are approximately constant, the matrix $\mathbf{H}$ in (3) is orthogonal, i.e.,

$$\begin{aligned} &\mathbf{H}^H \mathbf{H} \\ &= \begin{pmatrix} \left|H_k^{(1)}\right|^2 + \left|H_{k+1}^{(2)}\right|^2 & H_k^{(1)*} \cdot H_k^{(2)} - H_{k+1}^{(1)*} \cdot H_{k+1}^{(2)} \\ H_k^{(1)} \cdot H_k^{(2)*} - H_{k+1}^{(1)} \cdot H_{k+1}^{(2)*} & \left|H_{k+1}^{(1)}\right|^2 + \left|H_k^{(2)}\right|^2 \end{pmatrix} \\ &= \begin{pmatrix} c_k & 0 \\ 0 & c_k \end{pmatrix} = c_k \cdot \mathbf{I}_2. \end{aligned} \tag{4}$$

Using (4), the transmitted symbol vector can be simply detected as follows:

$$\hat{\mathbf{X}} = Q(\mathbf{X}) = Q\left(\frac{\mathbf{H}^H \cdot \mathbf{Y}}{c_k}\right) = Q\left(\mathbf{X} + \frac{\mathbf{H}^H \cdot \mathbf{Y}}{c_k}\right) \tag{5}$$

where $()^H$ and $Q()$ denote the conjugate transpose and the quantization operation. However, in the case that the number of sub-carriers is small, the channel gains between adjacent sub-carriers are not constant, and the matrix $\mathbf{H}$ is non-orthogonal, i.e.,

$$\begin{aligned} &\mathbf{H}^H \mathbf{H} \\ &= \begin{pmatrix} \left|H_k^{(1)}\right|^2 + \left|H_{k+1}^{(2)}\right|^2 & H_k^{(1)*} \cdot H_k^{(2)} - H_{k+1}^{(1)*} \cdot H_{k+1}^{(2)} \\ H_k^{(1)} \cdot H_k^{(2)*} - H_{k+1}^{(1)} \cdot H_{k+1}^{(2)*} & \left|H_{k+1}^{(1)}\right|^2 + \left|H_k^{(2)}\right|^2 \end{pmatrix} \\ &= \begin{pmatrix} c_k & e_k \\ e_{k+1} & c_{k+1} \end{pmatrix} \neq c_k \cdot \mathbf{I}_2, \end{aligned} \tag{6}$$

where $e_k^* = e_{k+1}$. Therefore, by (6) the decision statistic vector can be rewritten as

$$\mathbf{X} = \begin{pmatrix} X_k \\ X_{k+1} \end{pmatrix} = \begin{pmatrix} X_k + \frac{e_k}{c_k} \cdot X_{k+1} + \frac{H_k^{(1)*} \cdot N_k + H_{k+1}^{(2)} \cdot N_{k+1}^*}{c_k} \\ X_{k+1} + \frac{e_{k+1}}{c_{k+1}} \cdot X_k + \frac{H_k^{(2)*} \cdot N_k + H_{k+1}^{(1)} \cdot N_{k+1}^*}{c_{k+1}} \end{pmatrix} \tag{7}$$

The second term of each element is the interference between adjacent sub-carriers. This interference seriously degrades the system performance of the SF-OFDM scheme.

III. Proposed Detection Algorithm

The proposed algorithm achieves the performance gain by eliminating the interference between adjacent sub-carriers with the parallel interference cancellation (PIC) method. Table I describes the proposed detection algorithm. After a symbol as expressed in (5) is detected in steps 1 and 2, the interference terms are cancelled in parallel in step 3. Finally, the transmitted symbols are detected in step 4.

Fig. 2 depicts the block diagram of the proposed detection algorithm. As shown in this figure, the proposed algorithm requires slightly more

표 1. 제안된 심볼 검출 알고리즘
Table 1. Proposed Symbol Detection Algorithm.

Step	Operation
1	$\tilde{X}_k = X_k + (e_k/c_k) \cdot X_{k+1} + N'_k, \tilde{X}_{k+1} = X_{k+1}(e_{k+1}/c_{k+1}) \cdot X_k + N'_{K+1}$
2	$\overline{X}_k = Q(\tilde{X}_k), \overline{X}_{k+1} = Q(\tilde{X}_{k+1})$
3	$\check{X}_k = \tilde{X}_k - (e_k/c_k) \cdot \overline{X}_{k+1}, \check{X}_{k+1} = \tilde{X}_{k+1} - (e_{k+1}/c_{k+1}) \cdot \overline{X}_k$
4	$\hat{X}_k = Q(\check{X}_k), \hat{X}_{k+1} = Q(\check{X}_{k+1})$

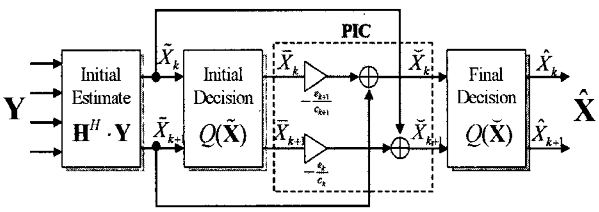

그림 2. 제안된 심볼 검출 알고리즘의 블록도
Fig. 2. Block diagram of the proposed detection algorithm.

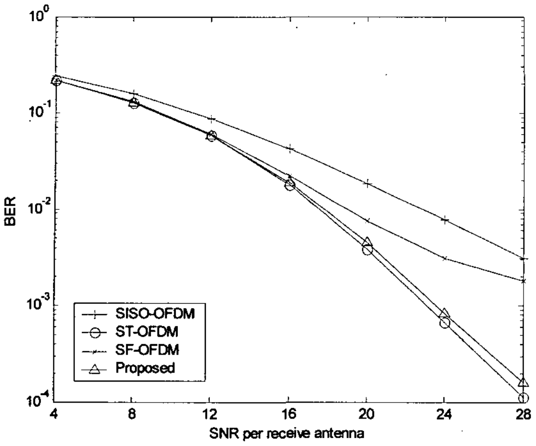

그림 3. 2 TX, 1 RX 경우에 대한 비트오류율 성능
Fig. 3. BER performance for 2 TX and 1 RX.

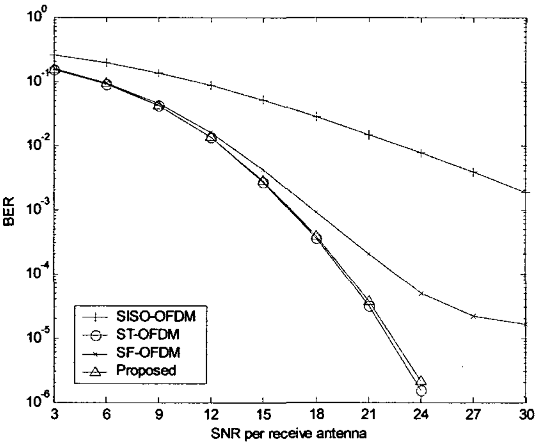

그림 4. 2 TX, 2 RX 경우에 대한 비트오류율 성능
Fig. 4. BER performance for 2 TX and 2 RX.

computation than the conventional algorithm. However, the proposed algorithm achieves much better performance gain as shown in Figs. 3-8.

The BER performance of the proposed detection algorithm is evaluated by the simulation. A 16QAM-OFDM system with 64 sub-carriers in a slowly time varying multi-path fading channel generated according to the channel model A for HIPERLAN/2[10] is considered. It is assumed that the channel state information (CSI) is available at the receiver except for the case in Fig. 5. Fig. 3 shows the BER performance of the SISO-OFDM, ST-OFDM, SF-OFDM, and SF-OFDM with the proposed algorithm for the case of 2 TX and 1 RX. It can be observed that at BER=10^{-3} the proposed algorithm achieves about 6-7 dB gain over the conventional SF-OFDM and maintains nearly the same

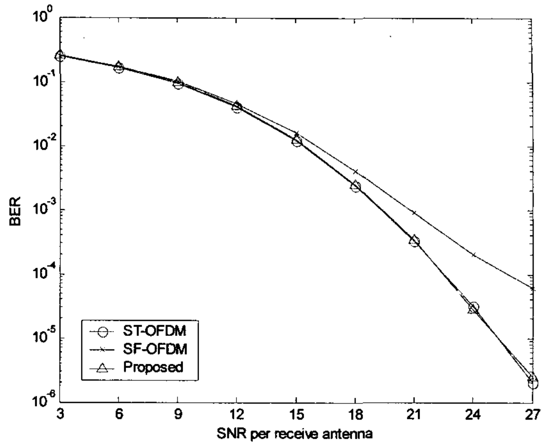

그림 5. 채널추정 오차가 존재하는 경우 비트오류율 성능
Fig. 5. BER performance for 2 TX, 2 RX, and imperfect channel estimation.

performance as the ST-OFDM.

The BER performance for the case of 2 TX and 2 RX is depicted in Fig. 4. The results similar to the case of 2 TX and 1 RX are observed. At BER=10^{-4} the proposed algorithm obtains about 3 dB gain over the conventional algorithm and also achieves perfectly the same performance as the ST-OFDM.

Fig. 5 shows the performance for the case of imperfect channel estimation. A least square (LS) estimation with orthogonal space-time pilot matrices [11] is used. Like the results in Fig. 3, the proposed algorithm shows a considerable performance improvement over the conventional algorithm.

Ⅳ. Performance Analysis Results

The PER performance of the conventional IEEE 802.11a WLAN and the SF-OFDM based WLAN with the proposed detection algorithm are shown in Fig. 6. The transmission modes 5-8, that support the peak data rates of 24-54 Mb/s, in IEEE 802.11a standards[12] are considered. As shown in this figure, at PER = 10-1 the SF-OFDM based WLAN with the proposed algorithm achieves the SNR gain of about 5-8 dB over the conventional IEEE 802.11a WLAN system for transmission modes.

By this SNR gain, the link throughput performance is improved as shown in Fig. 7. The link throughput is estimated by the methods in [13]-[14]. Assuming

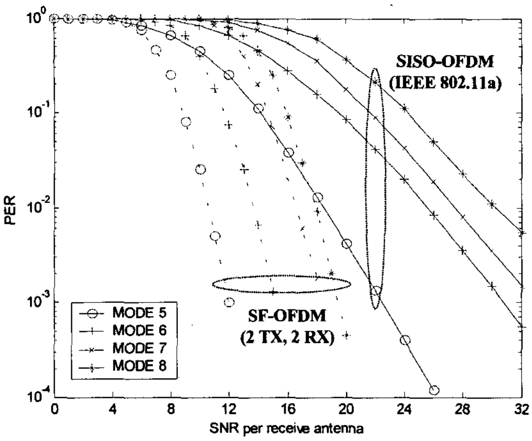

그림 6. 패킷오류율 성능

Fig. 6. PER performance (The solid line denotes the PER of the conventional IEEE 802.11a WLAN, while the dotted line does that of the SF-OFDM WLAN with the proposed algorithm).

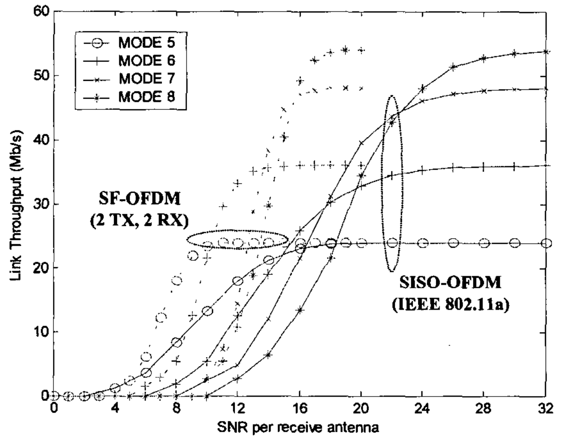

그림 7. Link throughput 성능

Fig. 7. Link throughput performance.

that the target throughput is set to 80% of the peak data rate, the SF-OFDM based WLAN obtains the SNR gain of about 4.6-7.0 dB over the conventional IEEE 802.11a WLAN.

Like the improvement of the link throughput, the coverage (operating range) performance is also enhanced as shown in Fig. 8. With the target throughput at 80% of the peak data rate, the conventional WLAN has the coverage of about 12.9-18.9 meter as the transmission modes, while the SF-OFDM based WLAN has the coverage of about 17.5-22.1 meter.

The comparison results of the PER, link throughput, and coverage performance are sum-

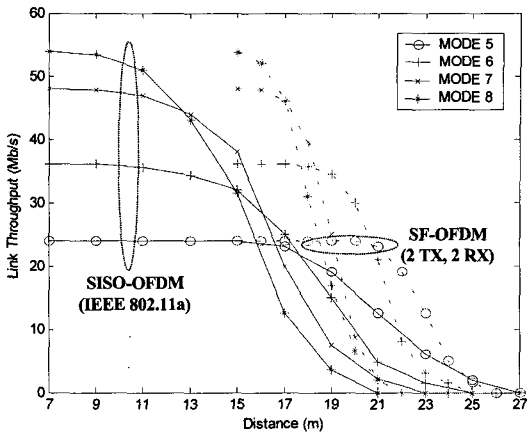

그림 8. Coverage 성능

Fig. 8. Coverage performance.

marized in Table II. For the target throughput at 80% of the peak data rate, the SF-OFDM based WLAN achieves the average SNR gain of about 5.95 dB and average coverage gain of 3.98 meter.

V. Implementation of SF-OFDM WLAN Baseband Processor

The block diagram of the SF-OFDM WLAN baseband processor is depicted in Fig. 9.

The transmitted baseband signals consist of packets composed of a preamble followed by OFDM symbols. The preamble in [11] is used for synchronization and channel estimation. Forward error correction is provided through the use of a rate 1/2 constraint length 7 convolutional code with selectable puncturing to provide rates of 2/3, 3/4, and 5/6. The coded bits are interleaved to prevent error bursts from being fed into the Viterbi decoder since the decoder does not work very well with burst errors. The interleaved coded bits are grouped together to form symbols. The symbols are modulated with one of BPSK, QPSK, 16QAM, and 64QAM.

The modulated symbols are encoded by the SF-OFDM encoder as transmission modes in Table III. The SF-OFDM encoded symbols are OFDM-modulated by 64-point inverse FFT (IFFT). Each output of the IFFT is converted to a serial sequence

표 2. 목표 throughput을 위한 SNR 및 coverage 비교
Table 2. Comparison of the required SNR and coverage for the target throughput.

TX mode	Thr. (Mb/s)	802.11a SNR (dB)	802.11a Coverage (meter)	Proposed SNR (dB)	Proposed Coverage (meter)	Gain SNR (dB)	Gain Coverage (meter)
5	19.2	12.9	18.9	8.3	22.1	4.6	3.2
6	28.8	17.3	15.8	10.7	20.2	6.6	4.4
7	38.4	19.6	14.5	14.0	18.2	5.6	3.7
8	43.2	22.2	12.9	15.2	17.5	7.0	4.6
Average						5.95	3.98

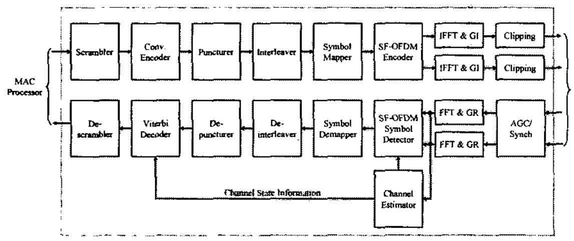

그림 9. SF-OFDM WLAN 기저대역 프로세서의 블록도
Fig. 9. Block diagram of the SF-OFDM WLAN baseband processor with the proposed detection algorithm.

표 3. 전송 모드
Table 3. Transmission modes.

Mode	Peak data rate	Modulation	Coding rate	MIMO scheme
1	6 Mb/s	BPSK	1/2	SF-OFDM
2	9 Mb/s	BPSK	3/4	SF-OFDM
3	12 Mb/s	QPSK	1/2	SF-OFDM
4	18 Mb/s	QPSK	3/4	SF-OFDM
5	24 Mb/s	16QAM	1/2	SF-OFDM
6	36 Mb/s	16QAM	3/4	SF-OFDM
7	48 Mb/s	64QAM	2/3	SF-OFDM
8	54 Mb/s	64QAM	3/4	SF-OFDM

and a cyclic prefix (CP) is added. After the CP is added, each OFDM symbol is clipped to reduce the effective peak-to-average power ratio (PAPR) for non-linear power amplifier.

In the receiver, an all-digital AGC detects RF amplifier gain error. After AGC tuning, time and frequency synchronization is performed. After the CP removal and FFT, interpolation-based channel estimation is performed to estimate the channel frequency response. Next, the transmitted symbols are detected by the SF-OFDM detector with the proposed algorithm.

As shown in Fig. 2, the proposed algorithm requires additional division operations. Since the division circuits require a much larger combinational

표 4. Division-free 심볼 검출 알고리즘
Table 4. Division-free symbol detection algorithm.

Step	Operation
1	$X'_k = c_k \cdot X_k + e_k \cdot X_{k+1} + N'_k, X'_{k+1} = c_{k+1} \cdot X_{k+1} + e_{k+1} \cdot X_k + N'_{k+1}$
2	$\bar{X}_k = Q(X'_k, c_k), \bar{X}_{k+1} = Q(X'_{k+1}, c_{k+1})$
3	$X''_k = \tilde{X}_k - e_k \cdot \bar{X}_{k+1}, X''_{k+1} = \tilde{X}_{k+1} - e_{k+1} \cdot \bar{X}_k$
4	$\hat{X}_k = Q(X''_k, c_k), \hat{X}_{k+1} = Q(X''_{k+1}, c_{k+1})$

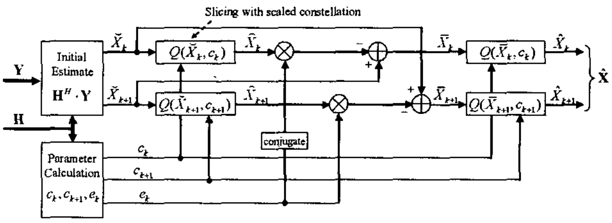

그림 10. 제안된 SF-OFDM 심볼 검출 알고리즘의 하드웨어 구조
Fig. 10. Hardware architecture for the proposed SF-OFDM symbol detection algorithm.

표 5. 게이트 수 및 전력소모 비교
Table 5. Comparison of the logic gate counts and power consumption of the conventional and proposed architecture.

	Conventional (w/ division)	Proposed (w/o division)	Reduction
Gate count	186 K	140 K	25 %
Power(mW)	123.6	54.9	55 %

logic delay, the design of the pipeline architecture incorporating them is very difficult. However, since the divisors, c_k and c_{k+1}, in the proposed algorithm are positive scalars, the division-free implementation with the scaled constellation in [14]-[15] can be possible.

Modified algorithm for the division-free implementation is depicted in Table IV. It can be observed that the division operation is removed.

Fig. 10 shows the hardware architecture of the proposed detection algorithm. As shown in this figure, the proposed algorithm was implemented without additional division circuits.

The results of logic synthesis and power analysis for the symbol detector with the modified division-free architecture using the 0.18um 1.8V CMOS standard cell library are shown in Table V. Power consumption is simulated using DesignPower

표 6. 구현된 프로세서의 논리 합성 결과
Table 6. Logic synthesis results for the SF-OFDM WLAN baseband processor.

Blocks	Gate count
SF-OFDM encoder & symbol detector	150 K
IFFT & FFT blocks	390 K
Symbol mapper & demapper	15 K
Conv. encoder & Viterbi decoder	190 K
Channel estimator	110 K
Other blocks	90 K
TOTAL	945 K

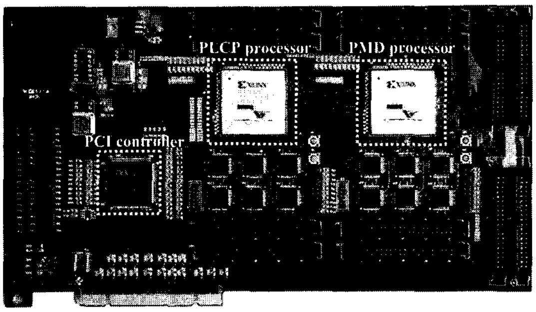

그림 11. FPGA 기반 테스트 시스템
Fig. 11. Test system implemented on FPGA chips.

from Synopsys. The DesignPower performs gate-level circuit simulation in measuring the power consumption 1,000 16QAM-OFDM symbols are used as input stimuli and the clock frequency is 20 MHz. By the division-free architecture, the proposed symbol detector results in the reduction of the logic gates by 25 % and the power consumption by 55 %.

Table VI depicts the logic synthesis results of the SF-OFDM WLAN baseband processor. With the proposed symbol detection algorithm and the division-free architecture, the total logic gate count for the processor is 945 K.

For the purpose of verifying the real-time operation, the SF-OFDM WLAN baseband processor with the proposed algorithm is implemented on FPGA chips operating at the clock speed of 80 MHz. Fig. 11 depicts the test system. The PLCP chip includes (de)scrambler, convolutional encoder, Viterbi decoder, (de)puncturer, and (de)interleaver, while the PMD processor has symbol (de)mapper, SF-OFDM encoder, SF-OFDM symbol detector, (I)FFT, channel estimator and synchronizer blocks. In the test results, it is verified that the preprocessor operates successfully in real-time mode.

Ⅵ. Conclusion

In this paper, we propose an efficient symbol detection algorithm for the SF-OFDM scheme and present the implementation results of the SF-OFDM WLAN baseband processor with the proposed algorithm. The BER performance of the proposed detection algorithm was evaluated by simulation. In the case of 2 transmit and 2 receive antennas, at BER=10-4 the proposed algorithm obtains about 3 dB gain over the conventional detection algorithm. The PER, link throughput, and coverage performance of the SF-OFDM WLAN with the proposed detection algorithm are estimated. For the target throughput at 80% of the peak data rate, the SF-OFDM WLAN achieves the average SNR gain of about 5.95 dB and the average coverage gain of 3.98 meter. The SF-OFDM WLAN baseband processor with the proposed algorithm is implemented with the 0.18um 1.8V CMOS standard cell library. With the division-free architecture, the total logic gate count for the processor is 945 K. Since the SF-OFDM WLAN with the proposed algorithm shows a considerable performance improvement over the conventional IEEE 802.11a WLAN, it can be a highly promising solution for the next generation WLAN.

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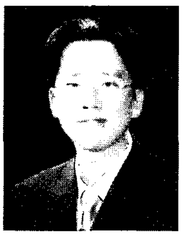

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