

## A DFT Based Filtering Technique to Eliminate Decaying dc and Harmonics for Power System Phasor Estimation

Yong-Taek Oh<sup>†</sup>, V. Balamourougan\* and T.S. Sidhu\*

**Abstract** - During faults, the voltage and current signals available to the relay are affected by the decaying dc component and harmonics. In order to make appropriate and accurate decisions, most of the relaying algorithms require the fundamental frequency phasor information that is immune to decaying dc effect and harmonics. The conventional Fourier phasor estimation algorithm is affected by the presence of decaying-exponential transients in the fault signal. This paper presents a modified Fourier algorithm, which effectively eliminates the decaying dc component and the harmonics present in the fault signal. The decaying dc parameters are estimated by means of an out-of-band filtering technique. The decaying dc offset and harmonics are removed by means of a simple computational procedure that involves the design of two sets of orthogonal digital DFT filters tuned at different frequencies and by creating three off-line lookup tables. The technique was tested for different decay rates of the decaying dc component. It was also compared with the conventional mimic plus the full cycle DFT algorithm. The results indicate that the proposed technique has a faster convergence to the desired value compared to the conventional mimic plus DFT algorithms over a wide range of decay rates. In all cases, the convergence to the desired value was achieved within one cycle of the power system frequency.

**Keywords:** DFT, mimic filter, phasor estimation

### 1. Introduction

Modern digital relaying techniques are generally based on phasor estimators for the protection of transmission lines, generators, transformers and bus bars. These phasor estimators approximate the current and voltage phasors of each phase of the power system. These phasor estimators must meet very stringent requirements. They should be of high-speed (usually converging within one cycle of the power system frequency), immune to frequency deviations, and insensitive to harmonics, sub-harmonics, high frequency oscillations, noise and decaying dc components. During a fault, the current and voltage signals from the power system contain some or all of the following components: fundamental frequency component, harmonic components that are multiples of the fundamental frequency, decaying dc component and noise.

In digital relays these signals are passed through a low pass anti-aliasing filter, which eliminates the high frequency components in the signal. Since the fundamental frequency (60 Hz) is generally the frequency of interest,

the cut-off frequency of the low pass filter is usually chosen well below half of the sampling frequency. For example, if the sampling frequency is taken as 5760 Hz, the cut-off frequency of the low pass filter according to Nyquist criterion [1] should be equal to or less than half the sampling frequency, which in this case would be 2880 Hz, to prevent aliasing. This will substantially eliminate high frequency noise present in the signal. Still, the anti-aliasing filter does not remove the effect of decaying dc.

The time constant and amplitude of the decaying dc are unknown and are associated with the fault resistance, fault position and the fault incipient time. The time constant of the decay is generally determined by the X/R ratio (inductive reactance to the resistance ratio) of the system. For high resistance earth faults the decay rates are very high, sometimes less than half the power system frequency cycle. Decaying dc is a non-periodic signal and its frequency spectrum encompasses all the frequencies. The decaying dc component therefore seriously affects the accuracy and convergence of digital filter algorithms such as Fourier, cosine, Walsh, Kalman and least-error-squares (LES) filters [2-4]. Due to this factor, the estimated phasors using these algorithms contain errors if decaying dc is present in the input signal.

Benmouyal proposed a digital mimic filter to suppress the effect of decaying dc over a broad range of time

<sup>†</sup> Corresponding Author: School of Information Technology, Electrical Engineering, Korea University of Technology and Education, Korea. (ytoh@kut.ac.kr)

\* Dept. of Electrical and Computer Science Engineering, University of Western Ontario, London, ON, Canada. (sidhu@eng.uwo.ca)

Received December 3, 2004 ; Accepted April 14, 2005

constants [5]. This filter requires the exact value of the time constant for a solid performance, which is usually not the case in real power system conditions. Sachdev et-al proposed the least error squares method to eliminate the effect of decaying dc by modeling the decaying dc parameters by the first two components of the Taylor series expansion of the decaying dc signal [3]. The recursive least error squares was proposed later to reduce the computational burden of conventional LES [7]. The performance of Kalman filtering to decaying dc was studied in [8-9]. It was concluded that the third order Kalman filter is sensitive to decaying dc components. Also in Kalman filtering, the time constant of the decaying dc has to be modeled to obtain good performance from the filter. Yong Guo et-al proposed a modified Fourier algorithm immune to decaying dc [10]. However, it demands extensive computations to remove the decaying dc offsets. Compared to any other technique available in the literature, the digital mimic filter is the most widely used technique in commercial relays to eliminate decaying dc, due to its simplicity in implementation.

Sidhu et al proposed a modified DFT based full cycle phasor estimation algorithm that is immune to decaying dc [11]. The algorithm effectively removes the decaying dc effect from the phasor estimates by means of two orthogonal digital DFT filters. However, the algorithm requires a tremendous amount of computations to calculate the decaying dc parameters and offsets its effect from the phasor estimate. This may not be suitable for some existing commercial relays because of their limited computing capability. As well, the use of high sampling rates may not be feasible because it reduces the inter-sampling time and hence, the time available for computations. High sampling rates may be desirable in a relay so that higher order harmonics can be computed for monitoring and power quality purposes. Furthermore, higher sampling rates will allow higher cut-off frequency of the low pass anti-aliasing filter, thereby reducing the order of the filter and its associated delays.

In this paper, the phasor estimates, which are immune to decaying dc and harmonics, are computed by extending the concept proposed in [11] with minimal computational requirements and which can be implemented in any modern commercial relay hardware platform. The performance of the proposed technique is compared with the most popular, digital mimic filter plus the full cycle DFT technique of phasor estimation.

## 2. The Proposed Technique

The proposed algorithm assumes that the input signal is pre-processed by an analog anti-aliasing filter, which

effectively removes very high frequency components present in the input signal. The proposed technique consists of two sets of orthogonal digital filters (Set I and Set II). Together they eliminate the decaying dc and harmonic components and, extract only the fundamental frequency component of the signal. It should be noted that each orthogonal filter set has a sine filter, which estimates the real part of the phasor, and a cosine filter, which estimates the imaginary part of the phasor.

### 2.1 Orthogonal Filter Design

As mentioned above, the proposed technique requires two sets of digital orthogonal filters. Filter Set I is tuned to fundamental frequency. This filter set is designed to not eliminate the decaying dc but to eliminate all other harmonics. Therefore, when a decaying dc signal is passed through this filter the output of this filter contains the fundamental distorted by the decaying dc component.

The second orthogonal filter set is tuned at a higher order harmonic. The order of this filter should be less than half the sampling frequency but more than the cut-off frequency of the low pass anti-aliasing filter. It is important to note that the low pass anti-aliasing filter has already eliminated this harmonic. Therefore, the output of this filter contains only the decaying dc component.

The decaying dc component effect can be removed from the output of the filter Set I by relating the outputs of the two orthogonal filter sets. This is achieved by means of creating three off-line look-up tables, which is explained in the next section.

The two orthogonal digital filter sets can be designed using LES or DFT techniques. The performance of the proposed algorithm is presented in this paper by designing the orthogonal filters using full cycle DFT, which provides superior noise suppression capabilities.

### 2.2 Look-up Tables

Look-up Table I is created from the outputs of the orthogonal filters of filter Set II. The orthogonal filters of filter Set II are given an input of a pure decaying dc with an initial magnitude of 1 pu and the time constants varying from 0 ms to 100 ms in steps of 1 ms. The ratios of the real part to imaginary part of these filters for each time constant are stored in this look-up table. This ratio is fixed for a given time constant, irrespective of the initial magnitude of the decaying dc. This ratio can be expressed as,

$$k_1(\tau) = \frac{fII_{realDC}(\tau)}{fII_{imagDC}(\tau)} \quad (1)$$

where,  $k_1(\tau)$  is the ratio at a given time constant  $\tau$ ,  $fII_{realDC}$

$(\tau)$  is the output of the sine filter, which computes the real part of the phasor defined at time constant  $\tau$ ,  $fI_{imagDC}(\tau)$  is the output of the cosine filter, which computes the imaginary part of the phasor defined at time constant  $\tau$ .

Look-up Tables II and III are created from the outputs of the sine and cosine filters of Filter Set I and II. The sine and cosine filters of the orthogonal Filter Set I are given an input of a pure decaying dc with an initial magnitude of 1 pu and the time constants varying from 0 ms to 100 ms in steps of 1 ms. The outputs of these filters will provide the real and imaginary parts due to the decaying dc alone for each time constant. In Look-up Table II the ratio of the real part of Filter I to the real part of Filter II is stored for each time constant. This ratio can be expressed as,

$$k_2(\tau) = \frac{fI_{realDC}(\tau)}{fII_{realDC}(\tau)} \quad (2)$$

where,  $k_2(\tau)$  is the ratio at a given time constant  $\tau$ ,  $fI_{realDC}(\tau)$  is the output of the sine filter of Filter Set I, which computes the real part of the phasor defined at time constant  $\tau$ , and  $fII_{realDC}(\tau)$  is the output of the sine filter of Filter Set II, which computes the real part of the phasor defined at time constant  $\tau$ .

Similarly, Look-up Table III is created, but with the imaginary parts of the two filter sets for different time constants. This ratio can be expressed as,

$$k_3(\tau) = \frac{fI_{imagDC}(\tau)}{fII_{imagDC}(\tau)} \quad (3)$$

where,  $k_3(\tau)$  is the ratio at a given time constant  $\tau$ ,  $fI_{imagDC}(\tau)$  is the output of the cosine filter of Filter Set I, which computes the imaginary part of the phasor defined at time constant  $\tau$ , and  $fII_{imagDC}(\tau)$  is the output of the sine filter of Filter Set II, which computes the real part of the phasor defined at time constant  $\tau$ . The ratios  $k_2$  and  $k_3$  are fixed for a given time constant, irrespective of the initial magnitude of the decaying dc. It is important to note that the orthogonal filters of Filter Set II contain only the effect of decaying dc offset in their outputs. Once the outputs of these filters are known, the effect of the decaying dc offset on the outputs of Filter Set I can be determined from Equations 2 and 3 with the help of the three look-up tables.

The next step is to use the look-up tables and perform error correction on the output of Filter Set I in order to obtain the correct phasor estimate.

### 2.3 Error Correction

The stepwise error correction procedure is given below:

- The low pass anti aliasing filter first filters the input signal.
  - The filtered signal is digitized and applied to the two sets of orthogonal filters. One set of filters is tuned to the fundamental and the other set is tuned to the  $m^{\text{th}}$  harmonic.
  - From the output of the orthogonal Filter Set II, the ratio of the real to imaginary part  $k_1$  is determined during each sampling interval.
  - The time constant  $\tau$ , corresponding to this ratio is obtained from Look-up Table I.
  - The ratios  $k_2$  and  $k_3$  corresponding to this time constant  $\tau$  are obtained from Look-up Tables II and III respectively.
  - The real part of the decaying dc component can be calculated now from Equation 2 since the ratio  $k_2$  and  $fII_{realDC}$  are known for the time constant  $\tau$ .
  - The imaginary part of the decaying dc component similarly can now be calculated from Equation 3 since the ratio  $k_3$  and  $fII_{imagDC}$  are known for the time constant  $\tau$ .
  - The error correction is carried out by subtracting the real and imaginary component values of the decaying dc obtained from the above step, from the respective real and imaginary parts of the outputs of the orthogonal Filter Set I. This now leaves only the real and imaginary components of the fundamental frequency phasor.
- In this way the decaying dc offset can be eliminated completely from the estimated phasors irrespective of the time constant of the decaying dc component.

### 2.4 Computations

The technique needs the following computations

1. Design of two sets of orthogonal digital filters
2. Creation of three look-up tables
3. Processing of the input signal using the two filters
4. Determining the time constant and the correction factors from the look-up table
5. Error correction
6. Estimation of the phasor

The first two are off-line computations and the rest are on-line computations. With modern microprocessor technology, the above-mentioned computations will not introduce significant computational burden. In the next section the performance of the algorithm for different time constants is shown.

## 3. Simulation Results

The sampling frequency of the input signal, the cut-off frequency of the low pass anti-aliasing filter and the center

frequency of the orthogonal Filter Set II are three very important parameters whose selection criterion is significant to this algorithm.

### 3.1 Low Pass Filter Parameter Selection

A higher sampling rate allows for a higher cut-off frequency of the low-pass anti-aliasing filter and a better response. A higher cut-off frequency for the low pass anti-aliasing filter means more harmonics are present in the signal available to the digital filters. It is important to realize that the low pass anti-aliasing filter is an essential element for all digital relaying algorithms. Since the digital orthogonal filters are designed using full cycle DFT, the integer harmonics are eliminated. The frequency responses of the combined filters are presented in the subsequent section, which shows considerable improvement in noise reduction compared to the mimic plus full cycle DFT filter. A sampling rate of 5760 Hz was selected for testing this algorithm. The cut-off frequency selected was 1800 Hz. A Butterworth 2<sup>nd</sup> order filter with a cut-off frequency of 1800 Hz was designed to test the algorithm.

### 3.2 Center Frequency Selection Criteria

The selection of the center frequency for the orthogonal digital Filter Set II depends on the cut-off frequency of the low pass anti-aliasing filter. The center frequency should be chosen well above the cut-off frequency of the low pass anti-aliasing filter. The significant criterion is that the center frequency signal should not be present in the filtered input signal. A higher center frequency allows a selection of higher cut-off frequency for the low pass filter and a better response speed. In a way these parameters are interdependent and their selection depends on the compromise the designer is willing to make for a particular application.

The centre frequency selected for designing the orthogonal Filter Set II is 2400 Hz. The data window taken for analysis is one complete cycle, which consists of 96 samples for the sampling frequency.

The orthogonal Filter Set I is tuned to extract the fundamental frequency and Filter Set II is tuned for 40th order harmonic, which is already eliminated by the low pass anti-aliasing filter. It is important to note that the filter Set II order can be anything greater than the cut-off frequency of the low pass anti-aliasing filter but should be less than half the sampling frequency.

In order to build the Look-up Table I, the orthogonal filters of DFT Filter Set I are given an input of a decaying dc signal of different time constants ranging from 0 ms to 100 ms in steps of 1 ms. The ratios of the real part to imaginary part of these filters for each time constant are

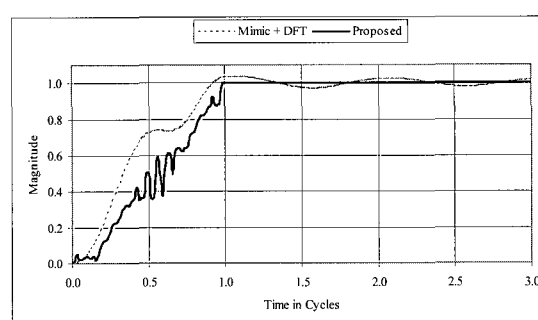
stored in this Look-up Table. This ratio is fixed for a given time constant, irrespective of the initial magnitude of the decaying dc. Look-up Tables II and III are designed as outlined in Section II.

### 3.3 Performance Evaluation

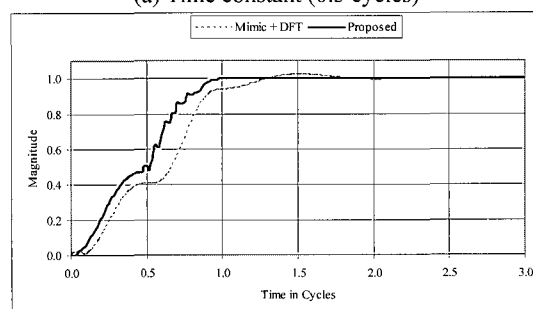
As mentioned before, the sampling rate is chosen at 96 samples per cycle. The input signal taken for analyzing the performance contains 1p.u of decaying dc and fundamental frequency component and 0.1p.u. of second, third and fifth harmonic components.

The time domain response of the algorithm is analyzed for the response speed and convergence. The time constant  $\tau$  of the decaying dc varies depending on the system configuration at the fault moment, fault location and fault resistance. Therefore, the sensitivity of the algorithm to variations of  $\tau$  is studied. The time constants are represented in terms of number of cycles. The time constants considered for testing are, 0.5, 2 and 5 cycles of the nominal frequency.

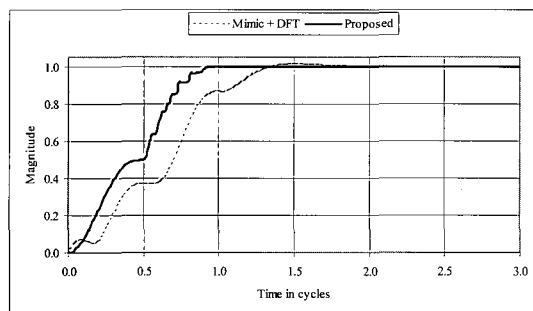
Fig. 1 (a), (b) and (c) show the phasors estimated by the proposed full-cycle algorithm orthogonal filters that are designed using DFT technique and the full-cycle mimic plus DFT. It can be seen from Fig. 1 that the proposed algorithm exhibits a faster convergence to the desired value within one cycle compared to the other algorithm. For a time constant of 0.5 cycles the proposed algorithm converges to the final value within one cycle, whereas the full-cycle mimic plus DFT exhibits oscillations even after 3 cycles. For rapid decaying rates it can be concluded that



(a) Time constant (0.5 cycles)



(b) Time constant (2 cycles)



(c) Time constant (5 cycles)

**Fig. 1** Time domain responses of the algorithms

the proposed algorithm has enhanced convergence and speed compared to the mimic plus DFT algorithm.

The performance index to compare both the phasor estimation algorithms is given by the following expression,

$$PI = \frac{\text{Number of samples to converge} - \text{signal window size}}{\text{signal window size}}$$

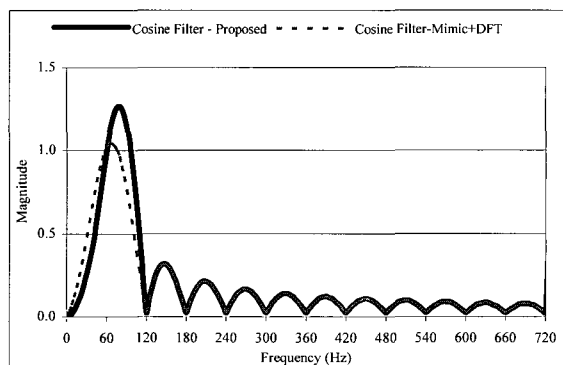
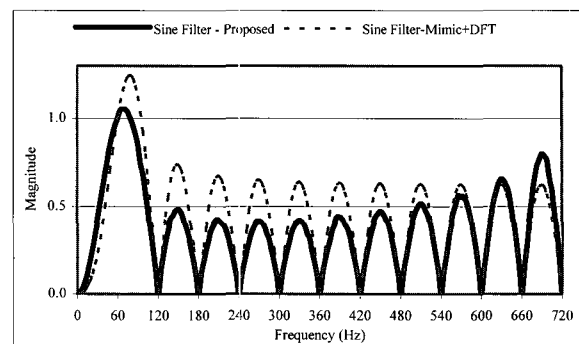
Table 1 gives the performance index of the proposed and mimic plus DFT algorithms for different time constants. From Table I it is evident that the accuracy and speed of convergence of the proposed algorithm is much better than the mimic plus DFT algorithms.

**Table 1** Performance index of the algorithms

Filters	Performance Index		
	$\tau=0.5$	$\tau=2$	$\tau=5$
Proposed	0%	0%	0%
Mimic plus Full-cycle DFT	large	35.2%	31%

### 3.4 Frequency Response of the Proposed Algorithm

Figs. 2 and 3 indicate the frequency responses of the proposed algorithm and the mimic plus full cycle DFT filters. Each filter has two parts, the sine filter and the cosine filter. The sine filter of the proposed algorithm has superior frequency response characteristics compared to

**Fig. 2** Frequency responses of cosine filters**Fig. 3** Frequency responses of sine filters

the full-cycle mimic plus DFT. The noise suppression capability of the proposed algorithm is much better than the other algorithm, which is evident from the frequency response characteristics shown in Fig. 2.

## 4. Conclusions

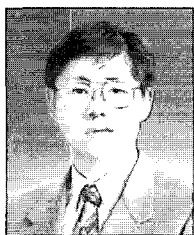
An algorithm for estimating power system phasors, which are immune to decaying dc offset and harmonics, is proposed in this paper. The proposed technique computes the phasors within one full cycle of the power system frequency. The technique needs three look-up tables and two digital orthogonal filter sets that are built off-line to remove the decaying dc offset effect from the input signal. Unlike the full cycle DFT plus mimic filter, this algorithm can dynamically estimate the decay time constant and eliminate it from the input signal thereby producing an accurate phasor estimate. The algorithm is computationally very efficient and can be implemented in any modern digital relay hardware.

## References

- [1] Lathi B. P., *Signal Processing and Linear Systems*, Oxford University Press, New York, 2001.
- [2] Sachdev. M. S, (Coordinator), *IEEE Tutorial Course, Microprocessor Relays and Protection Systems*, IEEE Service Center, Publication No. 97EH0269-1-PWR, 1997.
- [3] Phadke, A. G., and Thorp, J. S.: '*Computer Relaying for Power Systems*', Research Studies Press Ltd., Hertfordshire, UK, 1988.
- [4] Phadke, A. G, Hlibka. T, Ibrahim, M, "A Digital Computer system or EHV Substations: Analysis and Field Tests," *IEEE Trans. Power Apparatus and systems*,, vol. PAS-95, No. 1, pp. 290–301, Jan/Feb 1976.
- [5] Gabriel Benumouyal "Removal of DC-Offset in Current Waveforms Using Digital Mimic Filtering",

*IEEE Trans. Power Delivery*, vol. 10 pp. 621-630, 1995.

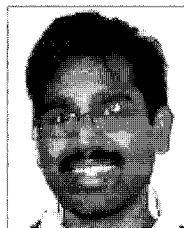
- [6] Sachdev, M.S., and Baribeau, M.A.: 'A New Algorithm for Digital Impedance Relays', *IEEE Trans. Power Delivery*, April 1995, 10, pp-
- [7] Sachdev, M.S., and Nagpal, M: 'A Recursive Least Error Squares Algorithm for Power System Relaying and Measurement Applications', *IEEE Trans. Power Delivery*, July 1991, vol. 6, pp 1008-1015.
- [8] Sachdev. M. S, H.C. Wood and N. G. Johnson, "Kalman Filtering Applied to Power System Measurements for Relaying," *IEEE Trans on PAS*, Vol. 104, No. 12, December 1985, pp. 3565-3573.
- [9] Girgis. A. A, and Brown. R. G., "Application of Kalman Filtering in Computer Relaying" *IEEE Trans. On Power Apparatus and Systems*, Vol. 100, No. 7, July 1981, pp. 3387-3397.
- [10] Yong Guo, Malden Kezunovic, and Chen. D., "Simplified Algorithms For the Removal of the Effect of Exponentially Decaying DC-Offset on the Fourier Algorithms", *IEEE Trans. Power Delivery*, Vol. 18, No. 3, July 2003.
- [11] Sidhu, T.S.; Zhang, X.; Albasri, F.; Sachdev, M.S., "Discrete-Fourier-transform-based technique for removal of decaying DC offset from phasor estimates", *Generation, Transmission and Distribution, IEE Proceeding* , Vol. 150, Issue: 6, 12 Nov. 2003, pp. 745 – 752.



#### Yong-Taek Oh

He received his B.S degree from the Sungsil University, Korea in 1980 and the M.Sc and Ph.D degrees Electrical Engineering from the Yonsei University, Korea, in 1982 and 1987 respectively in Electrical Engineering . From 1987 to 1991, He was with the

Computer Center of Korea Electric Power Corporation as a Section Chief. He joined the faculty of Korea University of Technology and Education, Cheonan, Korea in 1991 where he is currently a Professor in the School of Information Technology. His areas of research interest are power system protection and control, power system stability, fault analysis, A.I application to power system including distribution system.



#### Vinayagam Balamourougan

He received his B.Tech degree from the Pondicherry Engineering College, India in 1997 and the M.Sc degree in Electrical Engineering in 2002 from the University of Saskatchewan, Saskatoon, and SK, CANADA. He is currently pursuing PhD degree from the University of Western Ontario, London, ON in the Department of Electrical & Computer Engineering. He worked for ALSTOM Limited (AREVA T&D), India as an Application Engineer in the Protection Engineering Department from 1997-2000. His areas of research interest are power system protection and control, substation automation, power system dynamics, and FACTS.



#### Tarlochan S. Sidhu

He received the B.E (Hons.) degree from the Punjabi University, Patiala, India, in 1979 and the M.Sc. and Ph.D degrees from the University of Saskatchewan, Saskatoon, and SK, Canada in 1985 and 1989, respectively. From July 1990 to June 2002, he was with the Department of Electrical Engineering, University of Saskatchewan, where he served as Professor and Graduate Chairman of the Department. He is currently Chair of the Electrical and Computer Science Engineering Department at the University of Western Ontario, London, ON. He is also the Hydro one Chair in Power Systems Engineering. His areas of research interest are power system protection, monitoring and control. Dr. Sidhu is a Fellow of IEEE (USA), Fellow of the Institution of Electrical Engineer (U.K) and Fellow of the Institution of Engineers (India). He is also a Registered Professional Engineer in the Province of Ontario and a Chartered Engineer in the U.K.