Partial Matched Filter for Low Power and Fast Code Acquisition of DSSS-CPFSK Signals

Hyung Chul Park

Abstract—**A partial matched filter (PMF) for semi-coherent correlation code acquisition of the DSSS-CPFSK signal is proposed. It is a calculation-reduced structure of the hard-limited signal based FIR filter, yet its code acquisition time is equal to that of the hard-limited signal based FIR filter. The PMF eliminates duplicate calculations by utilizing the characteristic that the hard-limited DSSS-CPFSK signal has same value in several consecutive samples.**

For example, the PMF can achieve about 95% reduction in gate size, as compared to the hard-limited signal based FIR filter, when the modulation index of the DSSS-CPFSK signal is equal to 1.5 and the sample rate is equal to 40 sample/chip.

Index Terms—**CPFSK, DSSS, Hard-limiting, Semi-coherent correlation detection, Code acquisition, FIR filter**

I. INTRODUCTION

Wireless communication systems operating in the ISM band, e.g., WLAN(IEEE 802.11), Bluetooth, and WPAN(IEEE 802.15.4), use a direct sequence spread spectrum (DSSS) or a frequency hopping spread spectrum (FHSS) to resist interference or jamming. The continuous phase frequency shift keying (CPFSK) based DSSS (DSSS-CPFSK) signal has some advantages over other modulation based DSSS signals. First, since a CPFSK signal has a constant envelope, a high power amplifier (HPA) can operate in saturation mode, leading to higher power efficiency. Second, a DSSS-CPFSK signal can be generated using the phase locked loop (PLL) based direct modulation, allowing for low-complexity, low-cost and low-power consumption transmitters. Third, it is possible to use a non-coherent detection based receiver. Coherent receivers have a better bit error rate (BER) performance than non-coherent receivers. However, the BER performances of coherent receivers are greatly dependent on the accuracy of the carrier phase synchronization scheme. This requires that coherent receivers maintain increased processing power and hardware complexity. For the carrier phase synchronization, long preamble bits are also required. The phase noise, caused by oscillators and frequency synthesizers, and relatively large Doppler spread may increase synchronization time. On the other hand, non-coherent receivers do not require carrier phase recovery. Therefore, the achievement of simple and low-power receivers is possible. Non-coherent receivers also reduce the overhead of the long preamble bits required for the carrier phase recovery.

In wireless communication, the length of preamble bits must be as short as possible to attain high throughput. However, the preamble must provide sufficient information to initialize communication. In DSSS communication, the preamble is also used for pseudo noise (PN) code acquisition, utilizing either a FIR filter or a serial correlator. A serial correlator uses fewer gates, but requires a long acquisition time. This disallows high throughput, as more preamble bits are necessary to account for the long acquisition time. FIR filters have fast acquisition times (theoretically $2T_b$), but require more gates due to the large number of multiplication and addition operations.

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Hence, during the past decades, the reduction of the multipliers in the FIR filter has been studied extensively. By using the canonical signed digit (CSD) representation and the powers-of-two coefficients, the multipliers can be simplified [5-9]. In, it was shown that the dynamic range of the multiplication can be reduced using the differential coefficients. Even though the multipliers can be simplified with the aforementioned methods, the FIR filters are still complex by the high resolution data. In addition, the automatic gain control (AGC) is necessary to scale the analog input signal to appropriate level for the high-resolution analog-to-digital converter (ADC). The settling time and robustness of the AGC is affected by the channel and noise.

If the received signal is hard-limited, the receiver has the following advantages. First, multipliers are not necessary for the FIR filter. Second, the AGC is not necessary. Third, the ADC is also not necessary. Thus, the receiver can achieve the low complexity and low power consumption. Alternatively, the hard-limited signal based detection has worse BER performance than the high resolution signal based detection, as shown in Fig. 1. In Fig. 1, it is shown that the segmented semi-coherent correlation detection with the hard-limited received signal suffers about 1dB degradation at a BER of 10^{-4} from the performance of the same detection with analog received signal.

In this paper, a partial matched filter (PMF) based segmented semi-coherent code acquisition architecture for the hard-limited DSSS-CPFSK signal is proposed in order to simplify the hard-limited received signal based FIR filter further. Its complexity is comparable to that of the serial correlator of the high resolution received signal, while the acquisition time is identical to that of the FIR filter of the hard-limited received signal. The PMF utilizes that the consecutive values of a PMF output are not the same only by the correlation value associated with the certain expected signal, in which the consecutive data of the expected signal have opposite signs. Section 0 reviews the DSSS-CPFSK modulation and the segmented semi-coherent correlation method. In Section 0, PMF is proposed. In Section 0, the hardware complexity of the PMF is compared with that of the hard-limited signal based FIR filter. Finally, Section 0 presents the conclusion.

II. DSSS-CPFSK MODULATION

A DSSS-CPFSK signal is written as

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\begin{aligned}
s(t) &= \sqrt{2E_b/T_b}\cos(\omega_c t + \phi_a(t)), \qquad nT_b < t < (n+1)T_b \\
\phi_a(t) &= 2\pi h \sum_{i=0}^{10} a(t) b(i) q(t - nT_b - iT_c),\ a(t) = \pm 1 \\
q(t) &= \begin{cases} 0 & ,t<0 \\ 1/2 \cdot t/T_c & ,0<t<T_c \\ 1/2 & ,t>T_c \end{cases}
\end{aligned} \tag{1}
$$

where h denotes the modulation index and $b(i)$ is the i-th component of a PN code. In this work, the modulation

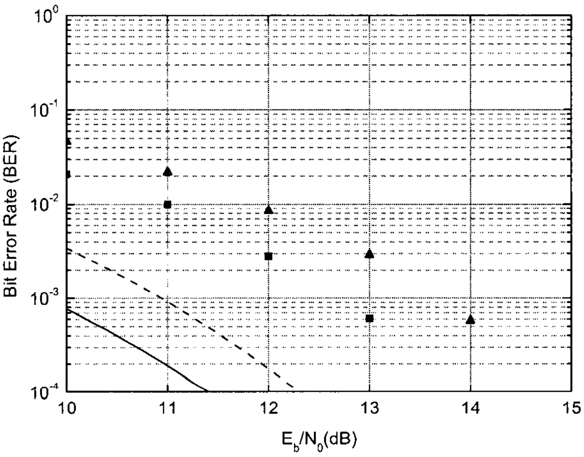

Fig. 1. BER performances of the detection schemes for the DSSS-CPFSK signals. Solid line is the analytical performance of coherent detection. Dashed line is the analytical performance of non-coherent detection. Solid square is the simulated performance of segmented semi-coherent correlation detection with analog received signal. Solid triangle is the simulated performance of segmented semi-coherent correlation detection with hard-limited received signal.

index is chosen to be 1.5 for the negligible power in the carrier frequency and signal spectrum spreading. The following 11-chip Barker sequence is used as the PN code sequence: -1 1 -1 -1 1 -1 -1 -1 1 1 1. T_c denotes the chip period, and is equal to $T_b/11$.

Either a coherent detector or a semi-coherent correlation detector can be used for the code acquisition of the DSSS-CPFSK modulated PN signal. In large carrier frequency offset, however, the code acquisition performances of both detectors are severely degraded. In order to overcome this problem, the segmented semi-coherent correlation detection based PN code acquisition scheme has been proposed. For this scheme, let the received signal be equal to $r(t)$. When the modulated phase with preamble code is equal to $\phi_p(t)$, let the expected signal be equal to $\cos(\omega_c t + \phi_p(t))$. The segmented semi-coherent correlation for the DSSS-CPFSK signal is then written as

$$\sum_{m=0}^{10}\left[\left(\int_{m*2T_b/11}^{(m+1)*2T_b/11} r(t)\cdot\cos(\omega_c t + \phi_p(t))dt\right)^2\right] \tag{2}$$

When both the received signal and the expected signal are sampled with N sample/chip, the complex baseband equivalent of (2) is written as

$$\sum_{m=0}^{10}\left\{\left|\sum_{i=0}^{2N-1} r(k+i+2N\cdot m)\cdot s^*(i+2N\cdot m)\right|^2\right\}, \tag{3}$$
$$k = 0,1,2,\cdots$$

where $s(k)$ denotes the complex baseband equivalent of the expected DSSS-CPFSK signal, which is written as

$$\begin{aligned} s(k) &= s_I(k) + js_Q(k) \\ &= \cos(\phi_a(t)) + j\sin(\phi_a(t))\Big|_{t=\frac{k}{N}T_c} \end{aligned} \tag{4}$$

where $r(k)$ denotes the complex baseband equivalent of the received signal. When the complex baseband equivalent of the noise is written as

$$n(k) = n_I(k) + jn_Q(k) = n_I(t) + jn_Q(t)\Big|_{t=\frac{k}{N}T_c} \tag{5}$$

$r(k)$ is then written as

$$\begin{aligned} r(k) &= s(k) + n(k) \\ &= (\cos(\phi_a(k)) + n_I(k)) + j(\sin(\phi_a(k)) + n_Q(k)) \end{aligned} \tag{6}$$

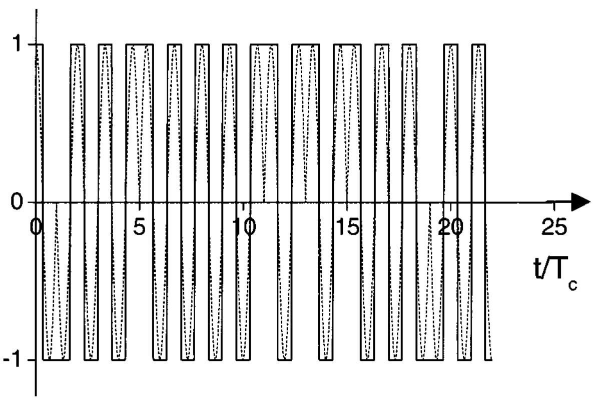

Fig. 2. Cosine term of the baseband DSSS-CPFSK signal. Solid line represents the hard-limited version of the baseband DSSS-CPFSK signal.

where $n_I(t), n_Q(t)$ denote independent baseband Gaussian processes with zero-mean and have a double sided power spectral density of $N_0/2$.

III. Partial Matched Filter

In Fig. 2, the dotted line represents the cosine term of the expected DSSS-CPFSK signal, as shown in (4). The solid line represents the hard-limited version of the DSSS-CPFSK signal. When the sample rate is equal to N sample/chip, the hard-limited CPFSK signal holds the same sign during N/*h* or 2N/*h* samples[1].

Let us define the *m*-th segmented correlation output as $y_{m,n}$ when the received signal $r(k),(k=(2N\cdot m+n),(2N\cdot m+n+1),\cdots(2N\cdot m+n+2N-1))$ is used for the correlation. Then, the difference between consecutive values of the *m*-th segmented correlation output is written as

$$\begin{aligned} y_{m,n} - y_{m,n-1} &= \sum_{i=0}^{2N-1} r(n+i+2N\cdot m)\cdot s^*(i+2N\cdot m) \\ &- \sum_{i=0}^{2N-1} r(n-1+i+2N\cdot m)\cdot s^*(i+2N\cdot m) \\ &= \sum_{i=0}^{2N-2} r(n+i+2N\cdot m)\cdot\{s^*(i+2N\cdot m) - s^*(i+1+2N\cdot m)\} \\ &+ r(n+2N-1+2N\cdot m)\cdot s^*(2N-1+2N\cdot m) \\ &- r(n-1+2N\cdot m)\cdot s^*(2N\cdot m) \\ &= d_1(m,n) + d_2(m,n) + d_3(m,n) \end{aligned} \tag{7}$$

Equation (7) shows that the difference between consecutive values of the *m*-th segmented correlation output is determined by three terms: (1) $d_1(m,n)$: the difference between the consecutive correlation data of the expected signal with the same received signal, (2) $d_2(m,n)$: the correlation data of the most recent received signal, and (3) $d_3(m,n)$: the correlation data of the oldest received signal. When both the received signal and the expected signal are hard-limited, $y_{m,n}$ and $y_{m,n-1}$ are differed by the following terms: (i) In $d_1(m,n)$, the correlation value associated with the expected signal, in which the consecutive expected signal are different, i.e., $s(i+2N\cdot m) \neq s(i+1+2N\cdot m)$, (ii) $d_2(m,n)$ and (iii) $d_3(m,n)$. When these differences are added to $y_{m,n-1}$, it becomes identical to $y_{m,n}$. The calculation of the aforementioned terms (i), (ii), and (iii) is defined as the partial matched filter (PMF).

In Fig. 2, it is shown that the number of zero-crossing

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[1] When the chip at $t = (n-1)T_c$ and $t = nT_c$ are different and the phase at $t = nT_c$ is equal to $\pm\pi/2$, 2N/*h* samples have the same sign.

for the DSSS-CPFSK signal with the modulation index of 1.5 is equal to 27 during $2T_b$ interval. Hence, for the term (i), 27 correlation values are necessary. Note that the number of zero-crossing is independent of the sample rate.

In [11] and [12], it was shown that the proposed method can be used for a DSSS-PSK signal. However, the proposed method can be used for the consecutive PN code, which has same sign. Hence, the area reduction rate for the DSSS-PSK is worse than that for the DSSS-CPFSK.

IV. Hardware Complexity Of PMF Based FIR Filter

The FIR filter for the semi-coherent correlation code acquisition scheme of the hard-limited received signal is shown in Fig. 4(a). Fig. 4(b) represents a schematic for the FIR filter shown in Fig. 4(a). In order to calculate the number of gates, the sample rate N_{sample} is chosen to be 40 sample/chip. Note that the adders in Fig. 4(b) operate at the sample rate. However, the adders require many gates; in this case about 25,000 gates.

Let N_{in} denote the number of input sample for FIR filter. In this work, N_{in} is equal to $22N_{sample}$. Since the input sample is 2's complemented hard-limited data, i.e., +1,0,-1, 3-bit adders are necessary for the first stage calculation. The number of 3-bit adder for the FIR filter is equal to $N_{3-bit} = \lfloor N_{in}/2 \rfloor$. When the number of (k-1) bit adder for the (k-3)-th stage calculation is equal to $N_{(k-1)bit}$, the number of k-bit adder for the (k-2)-th stage calculation becomes equal to $N_{k-bit} = \lfloor N_{(k-1)bit}/2 \rfloor$. When the number of m-bit adder for the (m-2)-th stage calculation is equal to 1, it becomes the final stage. Since the number of gates of the general k-bit adder is equal to about $7k$, the number of gates for the hard-limited signal based FIR filter is written as

$$\sum_{k=3}^{m} N_{k-bit} \cdot 7 \cdot k \quad \text{where} \quad N_{k-bit} = \lfloor N_{(k-1)bit}/2 \rfloor, \quad N_{3-bit} = \lfloor 11 \cdot N_{sample} \rfloor \tag{8}$$

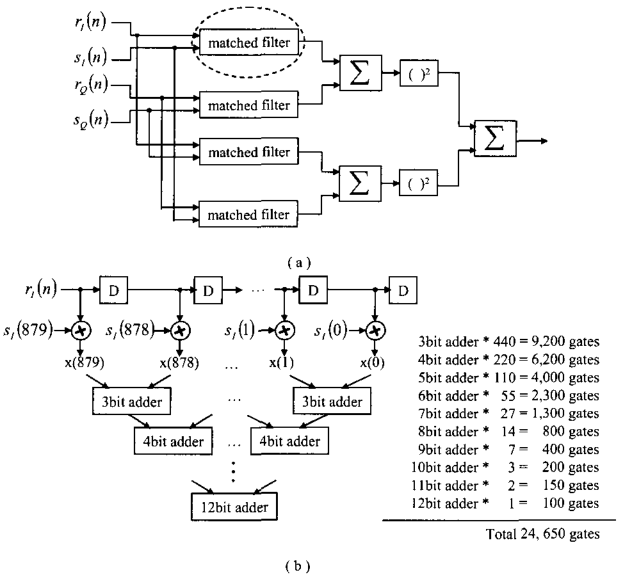

Fig. 3. Block diagram of the PMF based FIR filter for the semi-coherent correlation code acquisition scheme of the hard-limited DSSS-CPFSK signal. Note that the sample rate is equal to 40 sample/chip.

Fig. 4 shows the block diagram of the PMF based FIR filter for the semi-coherent correlation code acquisition scheme of the hard-limited received signal. The adders of 8-bit width and under in Fig. 4(b) are replaced by 8 bit accumulators. The accumulator is realized with PMF, such that the number of gates for the adder block can be reduced to about 1,300. This is only 5% of the number of gates required for the adder block in the FIR filter.

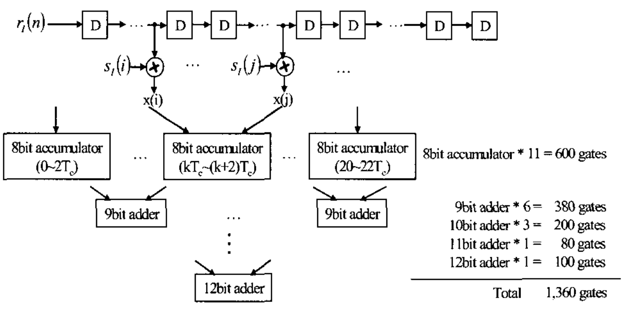

Fig. 4. Block diagram of the FIR filter for the semi-coherent correlation code acquisition scheme of the hard-limited DSSS-CPFSK signal. Note that the sample rate is equal to 40 sample/chip

Since the number of sample per chip is equal to N_{sample}, the number of sample used for the segmented correlation of $2T_c$ interval is equal to $2N_{sample}$. Hence, for the correlation result by the PMF, the necessary bit width of the accumulator is equal to $B_{acc} = \lfloor \log_2(2 \times 2N_{sample}) \rfloor$ bit. And, the number of accumulator for the segmented semi-coherent correlation detection is equal to 11, as shown in (3). The accumulator uses the result of the PMF of each segment. In Table 2, the data used for the PMF are represented. Table 2 shows that the number of zero-crossing is dependent on the modulation index of the DSSS-CPFSK signal. The bit width and number of adders for the next stage calculation are $(B_{acc}+1)$ and 6, respectively. Thus, the number of gates for the FIR filter using PMF is written as

$$\begin{aligned} &11 \cdot 7B_{acc} + 6 \cdot 7(B_{acc}+1) + 3 \cdot 7(B_{acc}+2) \\ &+ 1 \cdot 7(B_{acc}+3) + 1 \cdot 7(B_{acc}+4) + G_{PMF}(h) \\ &= 133 + 154B_{acc} + G_{PMF}(h) \\ &= 133 + 154 \cdot \lfloor \log_2(2 \times 2N_{sample}) \rfloor + G_{PMF}(h) \end{aligned} \quad (9)$$

In (9), $G_{PMF}(h)$ denotes the number of gates for the PMF. Table 1 compares the number of gates of the adder block in the PMF based FIR filter and the hard-limited signal based FIR filter in terms of the modulation index and the sample rate. In Table 1, it is shown that the number of gates of the FIR filter is proportional to the sample rate, while the number of gates of the PMF based FIR filter is proportional to the modulation index.

Table 2. Characteristics of data used for the PMF.

	Group 1	Group 2
Number of corresponding segment	6	5
Number of zero-crossing $(h = k + 1/2)$	$2k$	$2k+1$
Number of most recent data	1	
Number of oldest data	1	

Table 1. Gate size comparison of the adder block for the PMF based FIR filter and the hard-limited signal based FIR filter.

modulation index	sample rate (sample/chip)	number of gates	
		PMF	FIR filter
1.5	40	1,360	24,650
	60	1,360	37,000
2.5	40	2,400	24,650
	60	2,400	37,000
3.5	40	3,000	24,650
	60	3,000	37,000

V. CONCLUSIONS

In this work, a partial matched filter based semi-coherent correlation code acquisition scheme for the DSSS-CPFSK signal has been proposed. It has both the advantages of fast code acquisition and a small number of gates. It utilized that the consecutive values of the segmented correlation output are not the same only by the value associated with the certain expected signal, in which the consecutive data of the expected signal have opposite signs.

It has been shown that the PMF based FIR filter requires a number of gates only proportional to the modulation index, while the number of gates of the FIR filter must be proportional to the sample rate. Thus, using the PMF would be advantageous for large sample rate based systems. It has been shown that the PMF based FIR filter allows for about 95% reduction in gate size, in comparison to the FIR filter, when the modulation index of the DSSS-CPFSK signal is equal to 1.5 and the sample rate is equal to 40 sample/chip.

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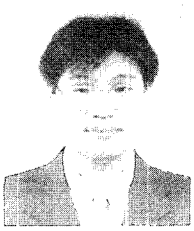

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