System Level Design of Multi-standard Receiver Using Reconfigurable RF Block

Changjae Kim, Young-Kyun Jang, and Hyung-Joun Yoo

Abstract – **In this paper, we review the four receiver architectures and four methods for multi-standard receiver design. Propose reconfigurable RF block can be used for both low-IF and direct conversion architecture. Also, using reconfigurable mixer method, it can be operated at 2~6 GHz range for multi-standard receiver. It consists of wideband mixer, filter, and automatic gain control amplifier and to get wide-band operation, 2~6 GHz, wide-band mixer use flexible input matching method. Besides, to design multi-standard receiver, LNA bank that support each standard is necessary and it has good performance to compensate the performance of wide-band mixer. Finally, we design and simulate proposed reconfigurable RF block and to prove that it has acceptable performances for various wireless standards, the LNA bank that supports both IEEE 802.11a/b/g and WCDMA is also designed and simulated with it.**

I. Introduction

Nowadays, the needs of multi-standard receiver that can support various wireless standards are rapidly increased, and a lot of architectures are proposed. Among them, the best architecture is the software defined radio (SDR), and the purist architecture of SDR is a digital RF (or RF direct digitization) shown in Fig. 1. This architecture performs the down-conversion, channel selection, and demodulation in digital domain. So it can get high programmability and reconfigurability. However, it needs a high performance analog-to-digital converter (ADC) as operating frequency goes high. Therefore, it can be used to the receiver that use low-frequency band [1].

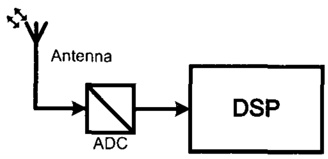


Fig. 1. Digital RF (or RF direct digitization) receiver architecture for SDR [1]

To implement the multi-standard receiver in high frequency band such as GHz, appropriate RF front-end and analog IF/baseband blocks are needed to down-convert the carrier frequency low in front of ADC. Typically, one analog IF/baseband block operated at low-frequency can be shared by each standard, but RF front-end block can not be shared because of their frequency sensitiveness.

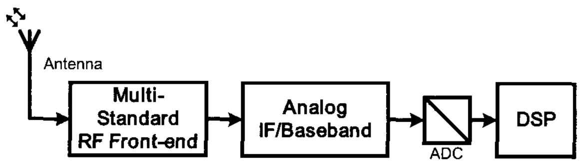


Fig. 2. Typical multi-standard receiver

As shown in Fig. 2, typical multi-standard receiver has frequency sensitive RF front-end. This means that the RF front-end can be used for specific standard operated at the particular frequency. Because of the frequency sensitive components, system designers have to design a new system with new components when a new wireless standard appeared. But if the components are reconfigurable, they

Manuscript received June 5, 2004; revised July 22, 2004.
School of Engineering, Information and Communications University (ICU) 119 Munjiro, Yuseong-gu, Daejeon, 305-714, Korea
TEL.: +82-42-866-6915, FAX.: +82-42-866-6923
E-mail: kimcj@icu.ac.kr, jjangyk@icu.ac.kr, hjyoo@icu.ac.kr

can be reused to a new standard, and it reduces the developing time greatly. Reconfigurability means the flexibility of the components. In the case of RF front-end, reconfigurable block means a block that can be used for any standard of any frequency band.

In this paper, we firstly review and categorize the multi-standard architecture and the methods of implementation. Subsequently, reconfigurable RF block (RRB) using flexibly input-matched mixer is proposed and specifications of it are described. Finally, as an example, the LNA bank and RRB that support both IEEE 802.11a/b/g and WCDMA standards are designed and simulated.

II. MULTI-STANDARD RF RECEIVER DESIGN TECHNIQUES

1. RF receiver architecture for multi-standard receiver

Multi-standard RF receiver architectures are typically categorized into four kinds; heterodyne, digital IF, direct conversion (or homodyne), and low-IF.

Heterodyne receiver is most reliable, but it has so many components. So, it is not used theses days because it is hard to make it small and integrate in single chip. The old version of multi-standard receiver used this architecture [14-15].

Digital IF architecture is used to overcome the integration problem of heterodyne architecture. RF front-end of a digital IF architecture is almost same as heterodyne architecture, but it performs IF signal processing in digital domain and the IF digitization can be performed by bandpass sampling technique. However, a power consumption problem that makes this architecture unsuitable for battery-operated mobile handset is remained. This is because high-resolution and high-speed ADC consumes high power. Therefore, it is commonly used in multi-standard base station, but there are some cases using this architecture to mobile terminal [7].

The most common architecture for multi-standard receiver is direct conversion, and many receivers adopt this architecture [4-6, 8-10, 12, 13]. Because of its simple structure, it is easy to make receiver small and integrate in shingle chip, but there are some drawbacks like DC offset problem. However, some techniques are developed to eliminate this problem.

To eliminate DC offset problem a low-IF architecture is used [4, 11]. Because it has almost same RF front-end as direct conversion, we can use both direct conversion and low-IF using one RF front-end [4]. However, it need image rejection mixer topology and digital baseband signal processing such as digital filtering for channel selection.

2. The method of multi-standard RF front-end implementation

The design methods of the multi-standard RF receiver are divided into four groups.

First, the old and easy method is parallel RF front-end method that uses several independent RF front-ends supporting each standard. It is used in [7, 11, 12-14], and Fig. 3 shows the simple block diagram. This method has a separated signal path whereas only one path is active at a time. So the receiver can get optimum performances for each standard. However, the cost, size and weight are high because it needs many components. In some cases [11], one path is used for several standard using similar frequency band; GSM850/GSM900 (869~960 MHz), DCS1800/PCS1900 (1805~1990 MHz).

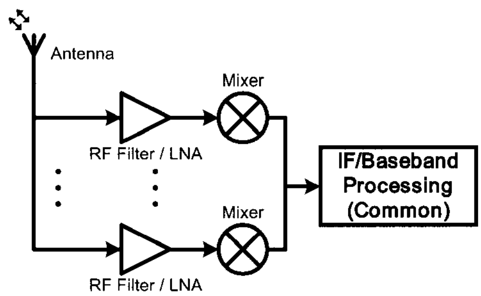


Fig. 3. Parallel RF front-end method

Second, the most common method is reconfigurable mixer method. It is used in [4-6, 9, 13, 15], and Fig.4 shows the simple block diagram. If the supported standards use the frequency band within the wideband mixer operation frequency, it can be used. The wider mixer operating frequency is, the lower mixer performance is. Therefore, the LNA must have more gain and lower noise figure than parallel RF front-end method to compensate the performance of wideband mixer. In some cases [6, 15], a dual band mixer is used to support only two standards.

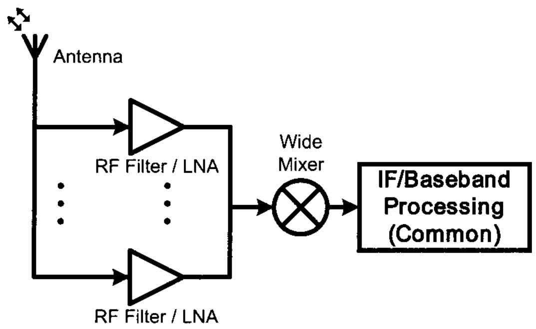


Fig. 4. Reconfigurable mixer method

Third, parallel reconfigurable mixer method depicted in Fig. 5 is used to get a both wide band operation and minimum number of components. It can be made by mixing parallel RF front-end method with reconfigurable mixer method. The reference [8] uses this method; GSM850/GSM900 use reconfigurable mixer method and DSC1800/PCS1900 use parallel RF front-end method. This method can support wide band operation, but it has many components and large size.

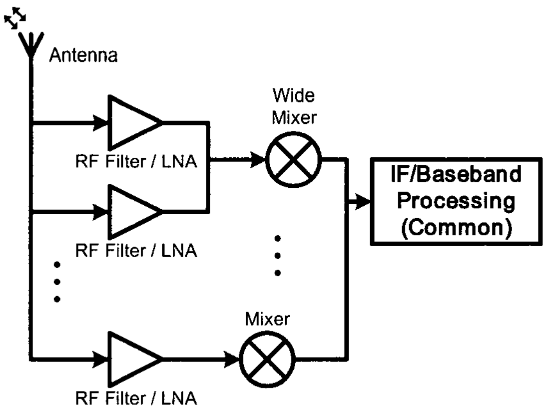


Fig. 5. Parallel reconfigurable mixer method

Finally, the simplest method is single path RF front-end method as shown in Fig. 6. In the case of reference [10], the receiver can support the wireless standard that uses the frequency from 0.9 to 2.5 GHz. This receiver uses wideband low noise variable gain amplifier (LNVGA) instead of wideband LNA to get a gain flexibility and wideband passive mixer to get a wideband operation. It is an ideal method of multi-standard RF front-end implementation, but it is hard to get both good performance and very wide operating frequency.

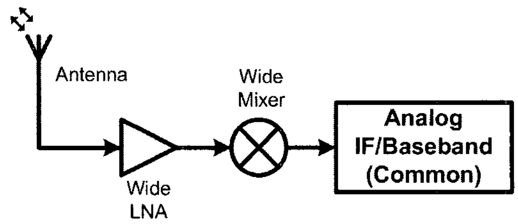


Fig. 6. Single path RF front-end method

III. Reconfigurable Rf block And Lna bank

Of above methods of multi-standard RF front-end implementation, reconfigurable mixer method can get not only a good performance, but also high integration. Therefore, we adopt the reconfigurable mixer method that uses several LNAs and one wideband mixer. Using this method, proposed receiver can be operated at very wide band frequency band, 2~6 GHz. Fig.7 shows the proposed reconfigurable receiver block which is divided into four parts.

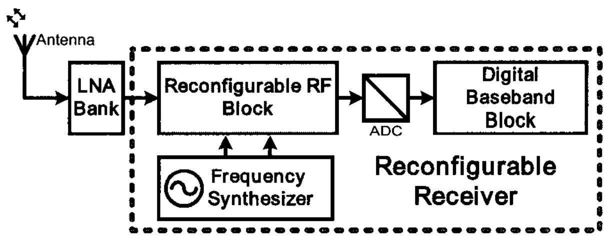


Fig. 7. Proposed multi-standard receiver

RRB can be implemented to the IP for SoC and used for a multi-standard receiver design. Moreover, it can be used for not only a direct conversion but also low-IF architecture. However, to support low-IF architecture, digital baseband part is necessary. Because low-IF signal is not down-converted yet, it has to be down-converted by digital mixer and filtered by digital filter. Moreover, the image rejection mixer topology must be used to convert low-IF signal properly. In this paper we focus on the RF part of reconfigurable receiver block. Therefore we design and simulate the RRB and LNA bank.

1. Reconfigurable RF block

The main purpose of the RRB is to down-convert input RF signal to baseband or low-IF. To do so, it contains wideband (2~6 GHz) mixers, automatic gain control (AGC) amplifiers, and filter blocks as shown in Fig. 8.

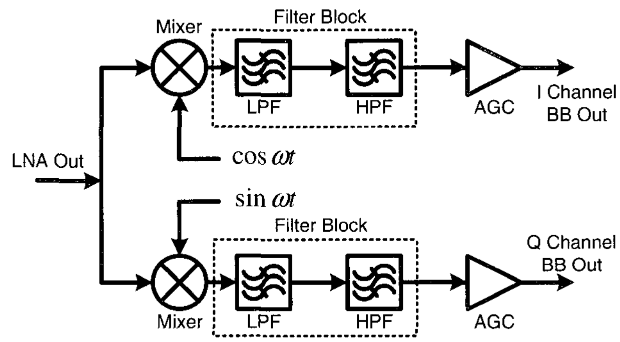


Fig. 8. Reconfigurable RF block

The main consideration factor for RRB is the performance of wideband mixer. Proposed wideband mixer operated at 2 ~ 6 GHz is made by the flexible input matching method using 0.25um CMOS process. The topology of this mixer is Gilbert cell that is widely used and Fig. 9 shows the mixer core and output buffer. The flexible input matching is the method of input matching using switching MOS transistors, inductors, and capacitors. The flexible matching network is connected to the mixer core input and shown in Fig. 10.

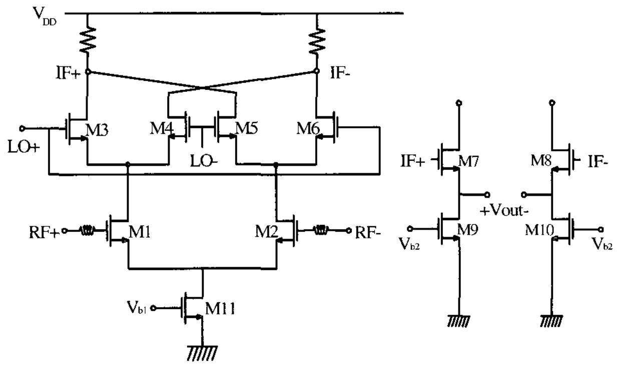


Fig. 9. Wideband CMOS mixer core and output buffer

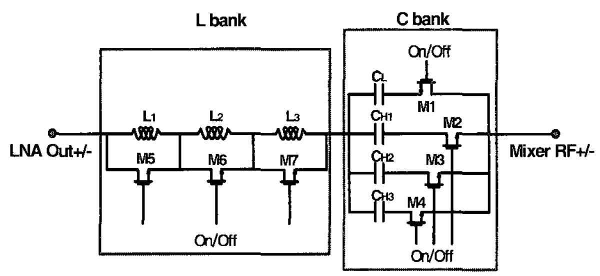


Fig. 10. The flexible matching network block

The flexible matching network consists of two parts, L bank and C bank; it needs seven MOS transistors to control the input impedance of the mixer. Among them, the capacitors and transistors, M1~M4 can be placed on a chip, but the inductors can not be integrated on a chip because of low Q value of on-chip inductor. Moreover, the transistors, M5~M7 are also external ones. If these transistors are integrated in the chip, bonding wires are needed to connect off-chip inductors; thus the inductance of the wire bonding affects the input impedance when switching transistor is on. Moreover, the variation of wire bonding inductance is high. In a word, to get a good performance, L bank must be implemented to off-chip components. However, the size of mixer is too big because of external L bank. Moreover, four L banks are needed; the mixer input is differential and two mixers are used to compose RRB. So, external L bank must use the system in package (SiP) technology to minimize external component size.

This mixer has two modes; low frequency mode (2~4 GHz) and high frequency mode (4~6 GHz) The combinations of L_1, L_2, L_3, and C_L is used for low frequency mode, while that of L_1, C_{H1}, C_{H2}, and C_{H3} is used for high frequency mode. Fig. 11 shows return loss of the mixer at the high and low frequency mode with flexible input matching. ①~⑦ is S_{11} of low frequency mode and ⓐ~ⓔ is that of high frequency mode.

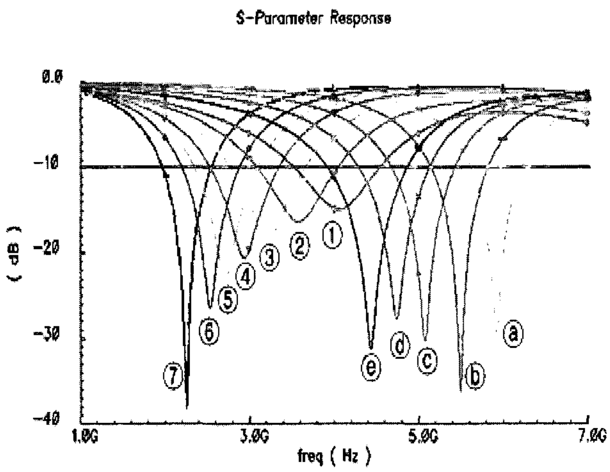


Fig. 11. Return loss with flexible input matching

Using 0.25 CMOS technology, we design and simulate reconfigurable mixer. The simulation result of the mixer at all operating frequency is shown in Fig. 12.

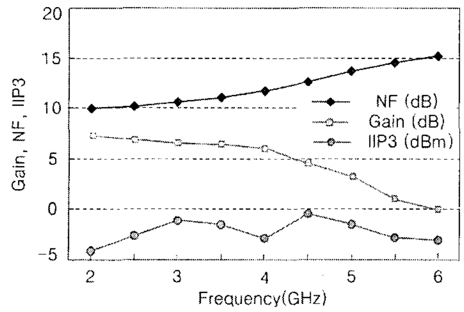


Fig. 12. The simulation result of wideband mixer

To support various standards, the dynamic range must have more than 82 dB; WCDMA has the widest dynamic range, 82 dB. There the AGC amplifier must have more than 70 dB gain variance when LNA must have more than 12 dB gain control. The specification of the AGC amplifier is shown in Table 1, and two stage AGC amplifiers are needed to get a wide dynamic range of the receiver.

Table 1. The specification of the AGC amplifier

NF	15 dB
IIP3 (Gain=0 dB)	20 dBm
Variable Gain Range	0 ~ 70 dB

Of the currently used wireless communication standards, the widest signal bandwidth is 20 MHz used by IEEE 802.11a/b/g WLAN standards. To support all standards, the bandwidth of RRB is more than 10 MHz that is the half of the widest bandwidth. Therefore proposed LPF is designed to 8th order 10 MHz Butterworth filter and HPF has 156.25 kHz stop-band to eliminate the effect of "DC offset."

$$NF_{RRB} = NF_{Mixer} + \frac{NF_{AGC} - 1}{Gain_{Mixer}} \tag{1}$$

$$\begin{bmatrix} NF_{RRB} & \text{: Noise factor of the RRB} \\ NF_{Mixer} & \text{: Noise factor of the mixer} \\ NF_{AGC} & \text{: Noise factor of the AGC amplifier} \\ Gain_{Mixer} & \text{: Gain of the mixer} \end{bmatrix}$$

$$IIP3_{RRB} = \left(\frac{1}{IIP3_{Mixer}} + \frac{Gain_{Mixer}}{IIP3_{AGC}} \right)^{-1} \tag{2}$$

$$\begin{bmatrix} IIP3_{RRB} & \text{: IIP3 of the RF/analog block} \\ IIP3_{Mixer} & \text{: IIP3 of the mixer} \\ IIP3_{AGC} & \text{: IIP3 of the AGC amplifier} \\ Gain_{Mixer} & \text{: Gain of the mixer} \end{bmatrix}$$

When we design the RRB using designed reconfigurable mixer and the AGC amplifier to fit the proposed specification shown in Table1, the specification of the RRB shown in Table 2 is easily calculated by Eq. (1) and Eq. (2). The mixer characteristics are worst case value.

Table 2. The specification of the RRB

Operating Frequency	2 ~ 6 GHz
RRB NF	< 18 dB
RRB IIP3	> -5 dBm
Output bandwidth	10 MHz
Controllable Gain Variance	> 70 dB

2. LNA bank

As shown in Table 2, the performance of RRB is lower than general mixer. This is because it is hard to get both the wide band operation and the good performance. However with this performance it is acceptable for designing multi-band receiver.

Because the noise figure, gain, and IIP3 point are the main specifications in the receiver side, we will analysis the system performance with these parameters. To get the gain at high gain mode and the noise figure of the LNA bank, the Eq. (3) is used.

$$NF_{Tot} = NF_{LNA} + \frac{NF_{RRB} - 1}{Gain_{LNA}} \tag{3}$$

$$\begin{bmatrix} NF_{Tot} & \text{: Noise factor of the receiver system} \\ NF_{LNA} & \text{: Noise factor of the LNA} \\ NF_{RRB} & \text{: Noise factor of the RRB} \\ Gain_{LNA} & \text{: Gain of the LNA at high gain mode} \end{bmatrix}$$

According to Eq. (3) and Table 2, the gain of the LNA bank must have more than 10 dB to get less than 10 dB noise figure, but LNA itself has more gain than LNA bank because the LNA bank has some lossy components; RF filter and Rx/Tx selection switch. As shown in Table 2, IIP3 of RRB is low. So, to avoid saturation, the output power of LNA bank is less than -30 dBm. Therefore, LNA bank must have both minimum and maximum gain mode. The equation to get a total system IIP3 at low gain mode is shown in Eq. (4) and we get the IIP3 value of RRB from the Table 2.

$$IIP3_{Tot} = \left(\frac{1}{IIP3_{LNA}} + \frac{Gain_{LNA}}{IIP3_{RRB}} \right)^{-1} \tag{4}$$

$$\begin{bmatrix} IIP3_{Tot} & : \text{IIP3 of the receiver system} \\ IIP3_{LNA} & : \text{IIP3 of the LNA} \\ IIP3_{RRB} & : \text{IIP3 of the the RRB} \\ Gain_{LNA} & : \text{Gain of the LNA at low gain mode} \end{bmatrix}$$

In summary, to get a acceptable noise figure and IIP3, the LNA bank can be composed with two-stage LNA and must have both high gain and low gain modes.

IV. Application Of Reconfigurable RF Block For Multi-Standard Receiver

Using proposed RRB and LNA bank, we can design and simulate the multi-standard receiver that supports IEEE 802.11a/b/g and WCDMA standards.

1. Receiver architecture

Available receiver architectures are direct conversion and low-IF architectures. In the case of IEEE 802.11a/b/g, the bandwidth is equal to the output bandwidth of designed the RRB. Therefore WLAN system must use direct conversion architecture. On the other hand, because WCDMA signal bandwidth is smaller than output bandwidth of the RRB, WCDMA system can use both low-IF and direct conversion architecture. However, direct converted signal lose their information near DC where HPF is used to eliminate the "DC offset problems." Therefore 5 MHz low-IF architecture is chosen for minimizing adjacent channel signal in the output spectrum. The output spectrum of RRB can be shown like Fig. 13.

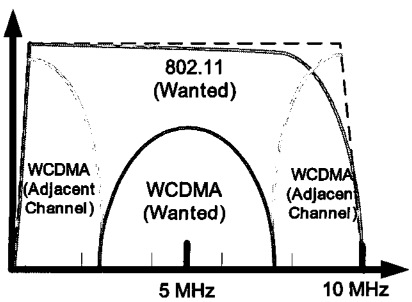


Fig. 13. Output spectrum of RF block (IEEE 802.11 Direct conversion, WCDMA 5MHz low-IF)

2. System level design and simulation

To prove an implementation possibility of multi-standard receiver using RRB, we design the receiver system using commercial components and proposed wideband mixer. Fig. 14 shows the schematic of designed receiver system.

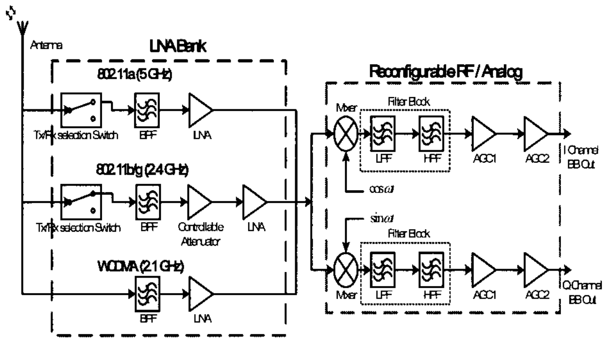


Fig. 14. The simple schematic of LNA bank and reconfigurable RF block

The RRB is designed using proposed reconfigurable mixer, filter block, and two AGC amplifiers. The LNA bank is designed using switches, filters and LNAs. The characteristics of these blocks are shown in Table 3; because the characteristics of reconfigurable RRB are changed by operation frequency, the values shown in Table 3 are worst case value of RRB but satisfy the specification shown in Table 2. The LNA block for IEEE 802.11b has a controllable attenuator because it has a high IIP3 specification.

Table 3. The simulation result of LNA bank and reconfigurable RF block

	LNA bank			RF Block
	802.11a	802.11b/g	WCDMA	
High Gain	11 dB	12	14.5 dB	70
Low Gain	-6 dB	-27 dB	-4.5 dB	-10
NF	5.1 dB	7 dB	3.5 dB	17 dB
IIP3	3 dBm	21 dBm	1.5 dB	-5 dBm

The system level simulation is performed using Agilent ADS simulation tool. Table 4 shows the simulation result. According to this result, the noise figure and IIP3 characteristics satisfies the specification of each standard.

Table 4. The simulation result of the multi-standard receiver

	802.11a	802.11b/g	WCDMA
High Gain	51.7 dB	46 dB	77 dB
Low Gain	0 dB	-20 dB	-5 dB
NF	8.1 dB (10 dB)	7.6 dB (10 dB)	4.3 dB (8.6 dB)
IIP3	0.2 dBm (-6 dBm)	18.8 dBm (14 dBm)	-3.2 dBm (-10 dBm)

* ( ): the specification of each standard.

V. CONCLUSION

Proposed RRB consists of wideband mixers, AGC amplifiers, and filter blocks and can be operated at 2~6 GHz. Its wide-band operation can be achieved by flexible input matching network of the mixer and flexible input matching network contains L and C bank and seven switching transistors. Among them L bank and three transistors that control L bank inductance must be implemented externally. In addition, to make external L bank small, SiP technique can be used. Therefore, the mixer has less than 15 dB noise figure, more than 0 dB gain, and more than -5 dBm IIP3 at 2~6 GHz. Moreover, using this mixer, designed RRB has 80 dB gain variance, 17 dB noise figure, and -5 dBm IIP3. To make multi-standard receiver, not only RRB, but also LNA bank is essential. Therefore, we designed LNA bank that support IEEE 802.11a/b/g and WCDMA and it was designed by commercial components and has low and high gain mode. Finally, using proposed RRB and LNA bank, multi-standard RF receiver was designed and simulated. It support both IEEE 802.11a/b/g and WCDMA and satisfy the system specification of each standard.

REFERENCES

[1] W.H.W. Tuttlebee, "Software-defined radio: facets of a developing technology," *IEEE Personal Communications Magazine,* Vol. 6 , Issue 2 , pp. 38 - 44, April 1999

[2] Georg Boeck, Dariusz Pienkowski, Radu Circa, Marius Otte, Benjamin Heyne, Piotr Rykaczewski, Reimund Wittmann, and Ralf Kakerow, "RF Front-End Technology for Reconfigurable Mobile Systems," *IEEE Microwave and Optoelectronics Conference 2003,* Vol. 2, pp. 863 - 868, 2003.

[3] J.A. Wepman and J.R. Hoffman, "RF and IF Digitization in Radio Receivers : Theory, Concepts, and Examples", http://its.bldrdoc.gov/pub/digradio/

[4] Brian J. Minnis and Paul A. Moore, "A Highly Digitized Multimode Receiver Architecture for 3G Mobiles," *IEEE Transactions on Vehicular Technology,* Vol. 52, No. 3, pp. 637 – 653, 2003.

[5] Aravind Loke and Mohy Abdelgany, "Multi mode wireless terminals – Key technical challenges," *IEEE RFIC Symposium,* pp. 11-14, 2003

[6] Mikko Hotti, Jouni Kaukovuori, Jussi Ryynanen, Kalle Kivekas, Jarkko Jussila, and Kari Halonen, "A Direct Conversion RF Front-End for 2-GHz WCDMA and 5.8-GHz WLAN Applications," *IEEE RFIC Symposium,* pp. 45-48, 2003.

[7] Raik Richter and H.-J. Jentschel, "An Integrated Wideband-IF-Receiver Architecture for Mobile Terminals," *IEEE RFIC Symposium,* pp. 583-586, 2003

[8] Rahul Magoon, Alyosha Molnar, Jeff Zachan, Geoff Hatcher, and Woogeun Rhee, "A Single-Chip Quad-band (850/900/1800/1900 MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer," *IEEE J. Solid-State Circuits,* Vol. 37, No.12, pp. 1710-1720, 2002.

[9] A. Savla, A. Ravindran, J. Leonard, and M. Ismail, "System analysis of a multi-standard direct conversion wireless receiver," *The 45th Midwest Symposium on Circuit and Systems,* Vol. 3, pp. 401-404, 2002

[10] Munenari Kawashima, Hitoshi Hayashi, Tadao Nakagawa, Kenjiro Nishikawa, and Katsuhiko Araki, "A 0.9-2.6 GHz Broadband RF Front-end For Direct Conversion Transceivers," *IEEE MTT-S Digest,* Vol. 2, pp 927-930, 2002.

[11] S. Dow, B. Ballweber, L. Chou, D. Eickbusch, J. Irwin, G. Kurtzman, P. Manapragada, D. Moeller, J. Paramesh, G. Black, R. Wollscheid, and K. Johnson, "A dual-band direct-conversion/VLIF Transceiver for 50GSM/GSM/DCS/PCS," *IEEE International Solid-State Circuits Conference*, Vol. XLV, pp. 230 - 231, February 2002

[12] Zhongming Shi and Reza Rofougaran, "A

singlechip and multi-mode 2.5/5 GHz RF transceiver for IEEE 802.11 wireless LAN," *IEEE ICMMT 2002,* pp. 229-232, 2002,

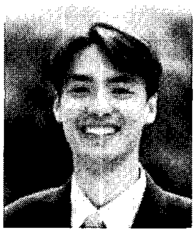
[13] Xiaopeng Li and Mohammed Ismail, "A Single-Chip CMOS Front-End Receiver Architecture for Multi-Standard Wireless Applications," *ISCAS 2001,* Vol. 4 , pp. 374 – 377, 2001.

[14] Masuo Umemoto, "An Experimental DSRC Multimode Terminal Using Software Defined Radio Technology," *IEEE RAWCON 2001,* pp. 165-168, 2001.

[15] Behzad Razavi, "A 900-MHz/1.8-GHz CMOS transmitter for dual-band applications," *IEEE J. Solid-State Circuits,* Vol. 34, Issue 5, pp. 573-579, 1999.

[16] Young-Kyun Jang, Changjae Kim, and Hyung-Joun Yoo, "Wide-band CMOS Mixer Design Using Flexible Input Matching Method," *IEEE ICMMT,* 2004.

Changjae Kim received his B.S. degree in electronics engineering from Pusan National University, Pusan, Korea, in 2001. He worked in LG CNS as system engineer. He is being enrolled in M.S. course in Information and Communications University, Daejeon, Korea. His research interests include RF systems for mobile communications, CMOS LNA design, and RF SoC.



Young-Kyun Jang received his B.S. degree in electronics engineering from Kwangwoon University, Seoul, Korea, in 2002. He is being enrolled in M.S. course in Information and Communications University, Daejeon, Korea. His research interests include CMOS RFIC design and RF systems for wireless communications.

Hyung Joun Yoo (M'95) received his B.S. degree in physics from Seoul National University in 1979, and M.S. and Ph.D. degrees, also in physics, from the Korea Advanced Institute of Science and Technology in 1990 and 1994, respectively. He had worked at the Agency for Defense Development from 1979 to 1982. He joined ETRI in 1983, where he had served as a director of the Advanced Technology Research Department. Since 1998 he is a professor at the Information and Communications University. His research interests include RF systems for mobile communications, RFICs, and nonlinear analysis of RF circuits.