Novel properties of erbium-silicided *n*-type Schottky barrier metal-oxide-semiconductor field-effect-transistors

Moongyu Jang, Yarkyeon Kim, Jaeheon Shin, Seongjae Lee, and Kyoungwan Park*

Abstract—**silicided 50-nm-gate-length *n*-type Schottky barrier metal-oxide-semiconductor field-effect-transistors (SB-MOSFETs) with 5 nm gate oxide thickness are manufactured. The saturation current is 120μA/μm and on/off-current ratio is higher than 10^5 with low leakage current less than 10 nA/μm. Novel phenomena of this device are discussed. The increase of tunneling current with the increase of drain voltage is explained using drain induced Schottky barrier thickness thinning effect. The abnormal increase of drain current with the decrease of gate voltage is explained by hole carrier injection from drain into channel. The mechanism of threshold voltage increase in SB-MOSFETs is discussed. Based on the extracted model parameters, the performance of 10-nm-gate-length SB-MOSFETs is predicted. The results show that the subthreshold swing value can be lower than 60 mV/decade.**

Index Terms—**SB-MOSFETs, Erbium-silicide, Novel phenomena**

I. Introduction

In Schottky barrier metal-oxide-semiconductor field-effect-transistors (SB-MOSFETs), source and drain regions are composed of silicide instead of impurity doped silicon. The structure of SB-MOSFETs is quite simple and ultra shallow junction can be formed easily and accurately with very low parasitic source and drain resistance, since the silicided junction depth is controlled by the deposited metal thickness and annealing temperature. The silicided junction formation temperature is very low in SB-MOSFETs, giving the opportunity to use metal as gate electrode and high dielectric materials as gate insulator. Moreover, the complicated channel doping steps can be eliminated because Schottky barrier exists between junction and channel. Thus, SB-MOSFETs have been proposed as an alternative to the conventional MOSFETs for decananometer-scale application [1-5].

But most of the experimental works are done in *p*-type SB-MOSFETs, especially by using platinum silicide [1, 3-5]. Also, there are many theoretical efforts to describe the current transport mechanism in SB-MOSFETs, which have different physical mechanisms with conventional MOSFETs, i.e., tunneling through the Schottky barrier exists in silicon/silicide interface [6-10]. But most of the previous theoretical results are not incorporated with experimental results.

In this paper, the theoretical and experimental current-voltage characteristics of erbium silicided *n*-type SB-MOSFETs are presented to describe the important current transport mechanisms in SB-MOSFETs.

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II. EXPERIMENTAL

In conventional MOSFETs, Titanium, Cobalt and Nickel are widely being used for the silicidation process to minimize the parasitic resistance of impurity doped source and drain [2]. But in this paper, erbium is chosen as source and drain metal of *n*-type SB-MOSFETs, because of its low Schottky barrier height (0.28 eV) for electrons [3]. The detailed device fabrication procedures are summarized in Fig. 1. As starting material, <100> *p*-type silicon-on-insulator (SOI) wafer is used. SOI wafer is boron doped with a resistivity of 13.5-22.5 Ω·cm and the corresponding doping concentration is about 1.0×10^{15} cm^{-3}. The thickness of the SOI and buried oxide (BOX) layer is 100 nm and 200 nm, respectively. The gate oxide is 5 nm thick SiO_2, grown by thermal oxidation and the gate electrode is highly phosphorus doped *n*-type polycrystalline silicon. Electron-beam lithography is employed to define gate pattern. After gate etching, 30 nm thick gate sidewall spacer is formed by using thermal oxidation method. After blanket dry etching of gate sidewall spacer, 100 nm thick erbium is sputtered. Erbium silicide is formed by using rapid thermal annealing (RTA) technique. Annealing temperature and time is 500 ℃ and 5 min, respectively. The non-reacted erbium is removed by using the mixture of H_2SO_4 and H_2O_2 (Sulfuric Peroxide mixture: SPM) for 10 min. The volume mixture ratio is 1:1. The formation of $ErSi_{1.7}$ phase is confirmed by x-ray diffraction (XRD) and Auger electron spectroscopy (AES) analysis. The sheet resistance is less than 30 Ω/□ even if the line width is less than 100 nm. Thus, erbium is applicable in sub-100 nm regime SB-MOSFETs manufacturing.

- Cleaning of <100> *p*-type SOI wafer
- Active lithography (e-beam) and dry etching
- Gate oxidation and n^+ polysilicon deposition.
- Gate lithography (e-beam) and dry etching
- Sidewall spacer oxidation and blanket etching
- Erbium deposition
- Annealing (500℃, 5min) and removal of non-reacted erbium

Fig. 1. Experimental procedures for erbium-silicided *n*-type SB-MOSFETs.

III. RESULTS AND DISCUSSION

Fig. 2 shows drain current (I_{DS}) to gate voltage (V_{GS}) characteristics of the 50-nm-gate-length erbium-silicided *n*-type SB-MOSFET. The open circle and solid line represents measured and simulation result, respectively. The gate voltage varied from 0 to 3 V and the drain voltage (V_{DS}) varied as 0.1 and 1.0 V. The off-leakage current is less than 10^{-4} μA/μm, and on/off-current ratio is larger than 10^5 for the 0.1 V drain voltage. The off-leakage current increases up to 10^{-2} μA/μm when the drain voltage is set to 1.0 V. The saturation current is 120 μA/μm when the gate and drain voltage is 3 and 1 V, respectively. Experimental results are well described by newly developed theoretical model [6], giving the model parameters of SB-MOSFET, which are compatible with MOSFETs except one additional parameter, i.e., Schottky barrier height (Φ_{bn}) [15]. In Fig. 2, I_{TH} and I_{TN} means thermionic and tunneling current dominant region, respectively, which are determined from the simulation results. From the curve fitting results, it is clear that the off- and on- current is mainly attributed to the thermionic and tunneling current component, respectively.

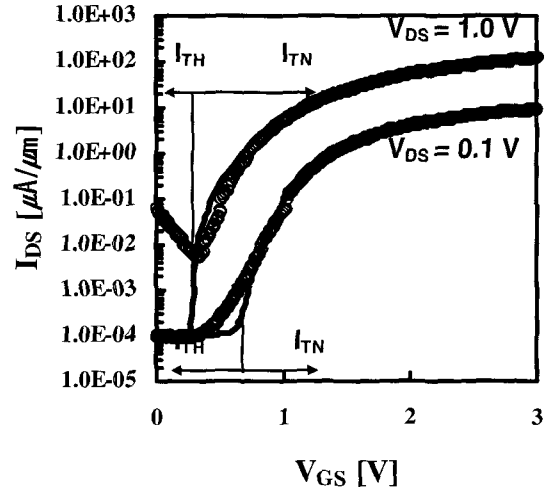


Fig. 2. Drain current to gate voltage characteristics of 50-nm-gate-length erbium-silicided *n*-type SB-MOSFET. The circle and solid line represents experimental and simulation results, respectively. In graph, I_{TH} and I_{TN} means thermionic and tunneling current dominant region, respectively.

The lowering of threshold voltage with the increase of drain voltage is attributed to the drain-induced barrier thinning (DIBT) effect [14], which is different from the drain-induced barrier lowering (DIBL) effect in conventional MOSFETs [11]. However, the major mechanism of the increase of drain current in SB-MOSFETs is not the lowering of Schottky barrier height but the thinning of Schottky barrier thickness. If barrier lowering is the major mechanism in the increase of drain current, the major turn-on current should be determined by thermionic component. But as shown in Fig. 2, the major turn-on current component is determined by tunneling current.

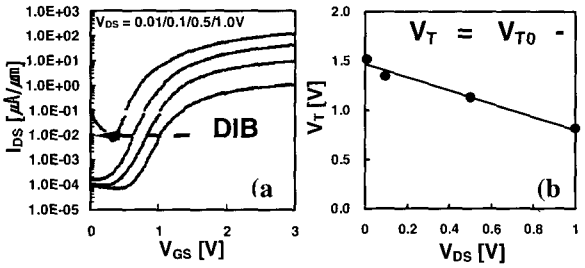


Fig. 3. Drain current to gate voltage characteristics of 50-nm-gate-length erbium silicided *n*-type SB-MOSFET with the increase of drain voltage (a) and the modeling of DIBT effect (b). The extracted threshold voltage (V_{T0}) and DIBT factor (σ_T) is 1.47 V and 0.59, respectively.

To analysis the DIBT effect quantitatively, more detailed drain current to gate voltage characteristics are measured. In Fig. 3(a), drain voltage varied as 0.01, 0.1, 0.5 and 1.0 V. As expected, the drain current increases at lower gate voltage as the drain voltage increases. Fig. 3(b) shows the extracted threshold voltage versus drain voltage characteristics. The threshold voltages are determined by using linear extrapolation method [12]. As shown in Fig. 3(b), threshold voltage varies linearly to the drain voltage. For the quantitative evaluation of DIBT effect, threshold voltage (V_T) is modeled as follows;

$$V_T = V_{T0} - \sigma_T V_{DS} \qquad (1)$$

where V_{T0} is the threshold voltage determined at very low drain voltage, σ_T is the DIBT factor and V_{DS} is the drain voltage. From the linear curve fitting, the extracted V_{T0} and σ_T value is 1.47 V and 0.59, respectively. The extracted V_{T0} value is comparable with the value in model parameters.

One more novel characteristic of SB-MOSFETs is that the threshold voltage (V_{T0}) is very large compared with that of conventional MOSFETs. To discuss this issue, conventional MOSFETs are manufactured using the same SOI substrate, gate oxide and the gate electrode with SB-MOSFETs. The gate length of conventional MOSFET is 10㎛. The extracted threshold voltage (V_{TC}) by linear extrapolation method is 0.2 V. So the channel region is inverted when the gate voltage is higher than 0.2 V. On the other hand, the threshold voltage of SB-MOSFET (V_{T0}) is 1.47 V as discussed in Fig. 3. The increase of threshold voltage in SB-MOSFETs can be explained with the existence of Schottky barrier. Although the channel is inverted, there is no tunneling current from source to channel region until the tunneling barrier becomes sufficiently thin. As the gate voltage increases over the threshold voltage of channel (V_{TC}), the number of electron carriers increases. The increase of the number of electron at channel decreases the Schottky barrier width, which gives the easy injection of tunneling electron from source to channel. From this reason, the existence of Schottky barrier gives the increase of threshold voltage (V_{T0}).

In Fig. 2, the abnormal increase of drain current with the decrease of gate voltage at drain voltage of 1 V can be explained by considering the hole carrier injection from drain into channel. In conventional *n*-type MOSFETs, the hole carrier injection from the source or drain is difficult because the junction can supply only one type of carrier, i.e., electron. But in SB-MOSFETs this is possible because the source and drain are composed with silicide. The metallic source and drain can supply both electron and hole. Recently, this phenomenon is also reported in carbon nanotube field effect transistor [13]. Fig. 4 shows the schematic diagram of *n*-type SB-MOSFETs with various bias conditions. Fig. 4(a) shows band diagram when no voltage is applied to the drain and the gate. The Schottky barrier is formed for hole at the source and drain. As shown in Fig. 4(b), as the negative gate voltage applied, channel region is filled with hole and the Schottky barrier becomes thinner for hole. As the drain voltage increases, the tunneled hole flows from drain to source,

which provides the drain current as shown in Fig. 4(c).

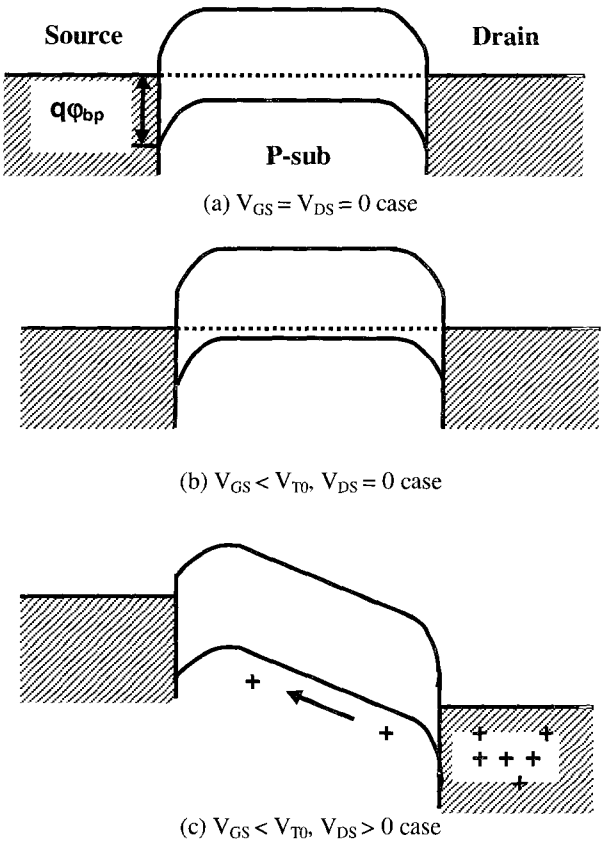


Fig. 4. Band diagrams for various biases. The barrier height of the silicide to *p*-substrate is $q\varphi_{bp}$. When the negative gate voltage is applied, hole carriers are accumulated in the channel region.

To confirm this, numerical calculation is done. The detailed calculation method is similar with the method in [6] except the consideration of hole carrier accumulation in channel region. Fig. 5 shows the calculation results when the drain voltage is 1 V. The circle and solid line represents experimental and theoretical result, respectively. The results clearly show that the increase of drain current with the decrease of gate voltage is caused from the hole injection from drain into channel when the negative gate voltage is applied. Thus, bipolar carrier can be injected into channel in SB-MOSFETs. Apparently, this phenomenon is similar with gate-induced-drain-leakage (GIDL) effect in conventional MOSFETs [11], which also gives the increase of the drain current with the decrease of gate voltage. But the detailed drain current flow mechanism is quite different.

In Fig. 6, drain current to gate voltage characteristics of 10-nm-gate-length *n*-type SB-MOSFET is simulated based on the extracted model parameters of erbium-silicided 50-nm-gate-length *n*-type SB-MOSFET. From the results, it seems that the attainable saturation current value is about 600㎂/㎛ in planar structure. One more important characteristic is that the subthreshold swing (SS) value can be less than 60mV/decade. This amazing characteristic is possible because there is no subthreshold drain current due to the existence of Schottky barrier.

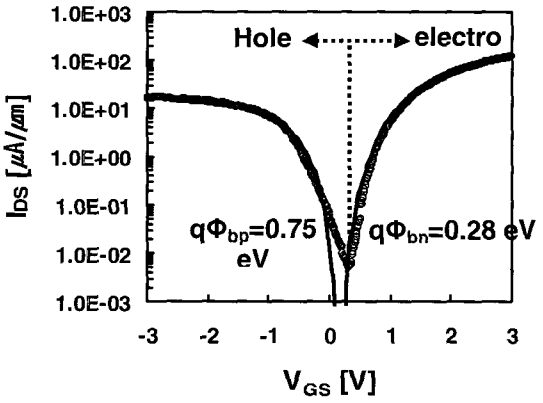


Fig. 5. Drain current to gate voltage characteristics for the negative gate voltage and the theoretical calculation results. The circle and solid line represents experimental and simulation results, respectively. When gate voltage is positive (negative), tunneled electron (hole) from source (drain) is the major component for the drain current.

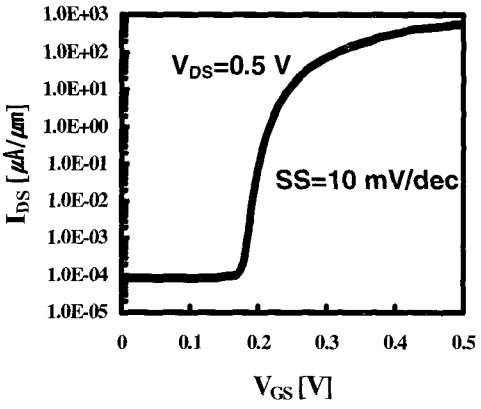


Fig. 6. Drain current to gate voltage simulation results of 10-nm-gate-length *n*-type SB-MOSFETs. Gate oxide thickness (T_{OX}) and power supply voltage (V_{dd}) is 1 nm and 0.5 V. $q\Phi_{bn}$, μ_0, Θ and λ values are from the model parameters of 50-nm-gate-length SB-MOSFET. Flatband voltage (V_{FB}) is -0.9 V and threshold voltage (V_{T0}) is 0.125V, respectively.

IV. Conclusion

In summary, erbium-silicided 50-nm-gate-length *n*-type SB-MOSFET shows excellent transistor characteristics. This device shows novel characteristics such as DIBT, ambipolar carrier injection, increase of threshold voltage and very low subthreshold swing characteristics. These results show the possible applicability of SB-MOSFETs for the decananometer-scale device applications.

References

[1] L. E. Calvet, H. Luebben, M. A. Reed, C. Wang, J. P. Snyder, and J. R. Tucker, "Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field-effect-transistors", *J. Appl. Phys.*, vol. 91, pp. 757-759, Jan. 2002.

[2] H. C. Lin, M. F. Wang, F. J. Hou, J. T. Liu, T. Y. Huang, and S. M. Sze, "Application of field-induced source/drain Schottky metal-oxide-semiconductor to fin-like body field-effect transistor", *Jpn. J. Appl. Phys.*, Part 2, vol. 41, pp. L626-L628, June. 2002.

[3] J. Kedzierski, P. Xuan, Erik H. Anderson, J. Bokor, T. J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime", Tech. Dig. – Int. Electron Devices Meet. **2000**, 57 (2000).

[4] A. Itoh, M. Saitoh, and M. Asada, "A 25-nm-long channel metal-gate p-type Schottky source/drain metal-oxide-semiconductor field effect transistor on separation-by-implanted-oxygen substrate", *Jpn. J. Appl. Phys.*, Part 1, vol. 39, pp. 4757-4758, Aug. 2000.

[5] S. A. Rishton, K. Ismail, J. O. Chu, K. Chan, and K. Y. Lee, "New complimentary metal-oxide semiconductor technology with self-aligned Schottky source/drain and low-resistance T gates", *J. Vac. Sci. Technol.* vol. B15, pp. 2795-2798, Nov. 1997.

[6] M. Jang, K. Kang, S. Lee, and K. Park, "Simulation of Schottky barrier tunnel transistor using simple boundary condition", *Appl. Phys. Lett.*, vol. 82, pp. 2718-2720, April. 2003.

[7] T. J. Thornton, "Physics and applications of the Schottky junction transistor", *IEEE Trans. Electron Devices*, vol. 48, 2421-2427, Oct. 2001.

[8] B. Winstead, and U. Ravaioli, "Simulation of Schottky barrier MOSFETs with a coupled quantum injection/Monte Carlo technique", *IEEE Trans. Electron Devices*, vol. 47, pp. 1241-1246, June. 2000.

[9] W. Saitoh, A. Itoh, S. Yamagami, and M. Asada, "Analysis of short-channel Schottky source/drain metal-oxide-semiconductor field-effect transistor on silicon-on-insulator substrate and demonstration of sub-50-nm n-type devices with metal gate", *Jpn. J. Appl. Phys.*, Part 1, vol. 38, pp. 6226-6231, Nov. 1999.

[10] J. R. Tucker, C. Wang, and P. Scott Carney, "Silicon field-effect transistor based on quantum tunneling", *Appl. Phys. Lett.*, vol. 65, pp. 618-620, Aug. 1994.

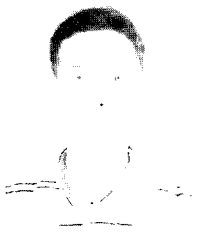
[11] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981) pp. 469-486.

[12] N. Arora, *MOSFET Models for VLSI Circuit Simulation* (Springer, New York, 1993), pp. 230-324.

[13] J. Clifford, and D. L. Pulfrey, "Bipolar conduction and drain-induced barrier thinning in carbon nanotube FETs", *IEEE Trans. Nanotechnology*, vol. 2, pp. 181-185, Sept. 2003.

[14] M. Jang, J. Oh, S. Maeng, W. Cho, S. Lee, K. Kang, and K. Park, "Characteristics of erbium-silicided n-type Schottky barrier tunnel transistors", *Appl. Phys. Lett.*, vol. 83, pp. 2611-2613, Sept. 2003.

[15] M. Jang, Y. Kim, J. Shin, S. Lee, and K. Park, "A 50-nm-gate-length erbium-silicided n-type Schottky barrier metal-oxide-semiconductor field-effect transistor", *Appl. Phys. Lett.*, vol. 84, pp. 741-743, Feb. 2004.



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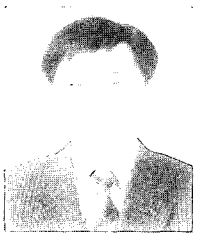

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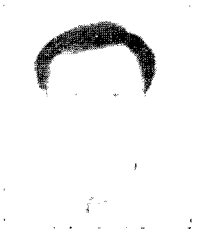

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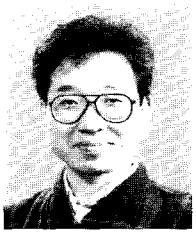

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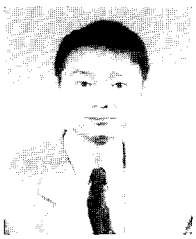

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