

A Study on the Parallel Multiplier over $GF(3^m)$ Using AOTP

AOTP를 적용한 $GF(3^m)$ 상의 병렬승산기 설계에 관한 연구

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Abstract

In this paper, a parallel Input/Output modulo multiplier, which is applied to AOTP(All One or Two Polynomials) multiplicative algorithm over $GF(3^m)$, has been proposed using neuron-MOS Down-literal circuit on voltage mode. The three-valued input of the proposed multiplier is modulated by using neuron-MOS Down-literal circuit and the multiplication and Addition gates are implemented by the selecting of the three-valued input signals transformed by the module. The proposed circuits are simulated with the electrical parameter of a standard $0.35\mu\text{m}$ CMOS N-well doubly-poly four-metal technology and a single +3V supply voltage. In the simulation result, the multiplier shows 4 uW power consumption and 3 MHzsampling rate and maintains output voltage level in $\pm 0.1\text{V}$.

요 약

본 논문에서는 다치 논리회로를 구현하는 방식 중 전압 모드 방식에서 neuron(v)MOS Down-literal circuit(DLC)의 다중 문턱전압 성질을 이용하여 유한체 $GF(3^m)$ 상에서 모든 항의 계수가 존재하는 기약 다항식에 대한 승산 알고리즘(AOTP)을 적용한 병렬 입-출력 모듈 구조의 승산기의 회로를 제안하였다. 3치 입력 신호가 인가되는 승산기는 뉴런모스 DLC를 이용하여 모듈화되고, 모듈에서 변환된 3치 입력 신호를 Pass 게이트를 통해서 선택하는 방식으로 승산 및 가산 게이트를 구현하였다. 설계된 승산기의 회로들은 +3V의 단일 공급 전원에서 $0.35\mu\text{m}$ N-well double-poly four-metal CMOS 공정의 모델 파라미터를 사용하여 모의실험이 수행되었다. 모의실험 결과를 통하여 승산기는 샘플링 레이트가 3MHz, 소비전력은 4uW, 출력은 $\pm 0.1\text{V}$ 이내의 전압레벨을 유지하는 것을 알 수 있다.

Key words : Parallel Multiplier, Multiple-Valued Logic, Neuron MOS, Down Literal Circuit

I. Introduction

Finite or Galois field has many important and practical applications in digital system. Finite fields can be applied in switching theory, error control coding, digital signal processing, image processing and an encryption block of telecommunication. In particular, the field $GF(2^m)$ is not only adopted to

the special calculation in digital image processing, digital signal processing but also used in the

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construction of computer architecture with high performance. And it has the property that is easily realized in a VLSI circuit [1].

In 1984, the parallel input/output systolic-array structure multiplier that can calculate $AB+C$ over $GF(2^m)$ was proposed by Yeh [2] and it has additional one AND gate and Ex-OR gate to extract the irreducible polynomial in each one-dimensional multiplier cell or two dimensional multiplier cell. The delay time for additional two gates is the disadvantage of such multiplier structure. The multiplier, proposed by Scott [3], has the bit-slice structure of serial input/output and it has the time delay according to the use of one AND gate and one Ex-OR gate to extract the irreducible polynomial in each multiplier cell.

Besides, Mastrovito [4-5] proposed the multiplication algorithm for the irreducible trinomial, such as x^m+x+1 , but it has the limitation to select the range because the irreducible polynomial is restricted to the order-three polynomial. Sunar[6] also proposed the multiplier using the irreducible trinomial, such as x^m+x^n+1 , but it needs the definition of n and the process of the equation arrangement by matrix and the trinomial for the irreducible polynomials.

On the other hand, Lee [7] proposed a effective algorithm for multiplication over $GF(2^m)$ with irreducible all-one polynomials(AOP). With that algorithm, they presented two low complexity bit-parallel systolic multipliers. Two architectures of multiplier which have low propagation delay are proposed by the AOP algorithm.

In MVL case, Muranaka [8] proposed a ternary systolic product-sum circuit over $GF(3^m)$ using neuron-MOS. They compared the ternary circuit for $GF(3^2)$ with the binary circuit for $GF(2^3)$ in terms of the priority of the number of transistors and inter-connections.

In this paper, we expanded the Lee's AOP multiplication algorithm to $GF(3^m)$ and applied the irreducible all one or two polynomials(AOTP) to the AOP algorithm. AOTP has non-zero coefficients over $GF(3^m)$, so all coefficients are one or two. On

condition that all multipliers calculates the same amount of information data, a multiplier over $GF(3^m)$ has the 1.5 times better data processing ability than a multiplier $GF(2^m)$. And if a multiplier over $GF(2^m)$ uses n -bit in the system, a multiplier over $GF(3^m)$ uses only $n(\log 2/\log 3)$ digits. So, a multiplier over $GF(3^m)$ has its originated benefits on the reduced digits. And we focused on designing of the expanded multiplier circuit over $GF(3^m)$ using neuron-MOS Down-Literal Circuit.

II. Multiplication over $GF(3)$

2.1 Addition and Multiplication over $GF(3)$

Important operations in finite fields are addition, multiplication, exponentiation, division, and computing multiplicative inverse. In those operations, multiplication is the key operation because computing exponentiation, division, and computing multiplicative inverse can be performed by computing multiplication iteratively. To implement the multiplier over $GF(3^m)$, we define the addition and multiplication over $GF(3)$. The elements of the $GF(3)$ are $\{ 0, 1, 2 \}$ and the set is closed to addition and multiplication and the operations are performed by modular 3 operation. Table 1 shows the truth table of addition and multiplication over $GF(3)$.

Table 1. The truth table of Addition and Multiplication over $GF(3)$

표 1. $GF(3)$ 에서의 승산과 가산에 대한 진리표

·	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

+	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

(a) Multiplication

(b) Addition

2.2 Multiplication algorithm for AOTPOver $GF(3)$

A polynomial of the form (1) over $GF(3)$ is called an all one or two polynomial (AOTP) of degree m if

$$a_i = 1 \text{ or } 2 \quad \text{for} \quad i = 0, 1, 2, \dots, m.$$

$$A = a_0 + a_1 \alpha + a_2 \alpha^2 + \dots + a_m \alpha^m \quad (1)$$

Suppose that α is a root of an irreducible AOTP of degree m . Two elements, multiplier A and multiplicand B in the Galois field $GF(3^m)$ can be represented as (2).

$$\begin{aligned} A &= a_0 + a_1 \alpha + a_2 \alpha^2 + \dots + a_m \alpha^m \\ B &= b_0 + b_1 \alpha + b_2 \alpha^2 + \dots + b_m \alpha^m \end{aligned} \quad (2)$$

where, the coordinates $a_i, b_i \in GF(3)$ for $0 \leq i \leq m$ and $\{1, \alpha, \alpha^2, \dots, \alpha^m\}$ are the extended basis of $GF(3^m)$.

Then the inner product of A and B is defined as (3)

$$\begin{aligned} A \bullet B &= (a_0 + a_1 \alpha + a_2 \alpha^2 + \dots + a_m \alpha^m) \\ &\bullet (b_0 + b_1 \alpha + b_2 \alpha^2 + \dots + b_m \alpha^m) \\ &= \left(\sum_{i=0}^m a_i \alpha^i \right) \bullet \left(\sum_{i=0}^m b_i \alpha^i \right) \end{aligned} \quad (3)$$

(3) is represented as (4) by replacing the product term with R.

$$\begin{aligned} R &= r_0 + r_1 \alpha + r_2 \alpha^2 + \dots + r_{2m} \alpha^{2m} \\ &= \sum_{i=0}^{2m} r_i \alpha^i = \sum_{i=0}^m r_i \alpha^i + \sum_{i=m+1}^{2m} r_i \alpha^i \end{aligned} \quad (4)$$

The second term of (4) can be represented as (5) by the multiplication property of finite field.

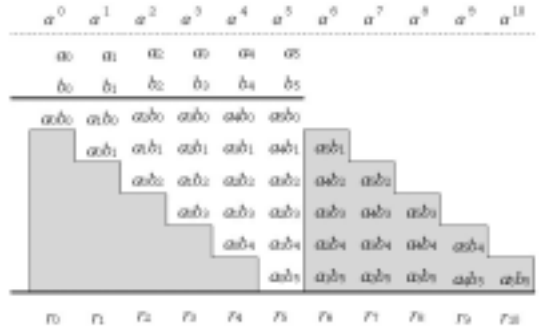
$$\begin{aligned} R &= \sum_{i=0}^m r_i \alpha^i + \sum_{i=0}^{m-1} r_{m+i+1} \alpha^i \\ &= \sum_{i=0}^{m-1} r_i \alpha^i + r_m \alpha^m + \sum_{i=0}^{m-1} r_{m+i+1} \alpha^i \\ &= \sum_{i=0}^{m-1} (r_i + r_{m+i+1}) \alpha^i + r_m \alpha^m \end{aligned} \quad (5)$$

In (5), let $r_i + r_{m+i+1} = R_i, r_m = R_m$, (5) is represented as (6).

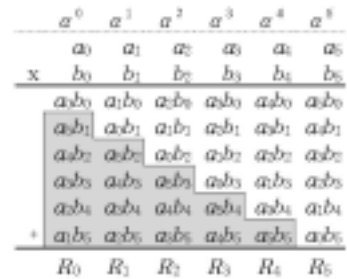
$$R = \sum_{i=0}^{m-1} R_i \alpha^i + R_m \alpha^m = \sum_{i=0}^m R_i \alpha^i \quad (6)$$

For example, the inner product of two polynomials of $GF(3^5)$ is represented as (7) by the definition and Fig. 1 shows the process of the multiplication of two AOTP A and B.

$$\begin{aligned} r_0 &= a_0 b_0 \\ r_1 &= a_1 b_0 + a_0 b_1 \\ r_2 &= a_2 b_0 + a_1 b_1 + a_0 b_2 \\ r_3 &= a_3 b_0 + a_2 b_1 + a_1 b_2 + a_0 b_3 \\ r_4 &= a_4 b_0 + a_3 b_1 + a_2 b_2 + a_1 b_3 + a_0 b_4 \\ r_5 &= a_5 b_0 + a_4 b_1 + a_3 b_2 + a_2 b_3 + a_1 b_4 + a_0 b_5 \\ r_6 &= a_5 b_1 + a_4 b_2 + a_3 b_3 + a_2 b_4 + a_1 b_5 \\ r_7 &= a_5 b_2 + a_4 b_3 + a_3 b_4 + a_2 b_5 \\ r_8 &= a_5 b_3 + a_4 b_4 + a_3 b_5 \\ r_9 &= a_5 b_4 + a_4 b_5 \\ r_{10} &= a_5 b_5 \end{aligned} \quad (7)$$



(a) Multiplication of two AOTP



(b) Represented form of coefficients

Fig. 1. Multiplication process of $GF(3^5)$.

그림 1. $GF(3^5)$ 에서의 승산

In this example, because of $m = 5$, we can get the R in (6) as (8).

$$\begin{aligned}
R &= \sum R_i \alpha^i \\
&= R_0 \alpha^0 + R_1 \alpha^1 + R_2 \alpha^2 \\
&\quad + R_3 \alpha^3 + R_4 \alpha^4 + R_5 \alpha^5
\end{aligned} \tag{8}$$

R_i are given by (5) and (6) as (9).

$$\begin{aligned}
R_0 &= r_0 + r_6, & R_1 &= r_1 + r_7 \\
R_2 &= r_2 + r_8, & R_3 &= r_3 + r_9 \\
R_4 &= r_4 + r_{10}, & R_5 &= r_5
\end{aligned} \tag{9}$$

with (7), (9) is represented as (10).

$$\begin{aligned}
R_0 &= a_0 b_0 + a_5 b_1 + a_4 b_2 \\
&\quad + a_3 b_3 + a_2 b_4 + a_1 b_5 \\
R_1 &= a_1 b_0 + a_0 b_1 + a_5 b_2 \\
&\quad + a_4 b_3 + a_3 b_4 + a_2 b_5 \\
R_2 &= a_2 b_0 + a_1 b_1 + a_0 b_2 \\
&\quad + a_5 b_3 + a_4 b_4 + a_3 b_5 \\
R_3 &= a_3 b_0 + a_2 b_1 + a_1 b_2 \\
&\quad + a_0 b_3 + a_5 b_4 + a_4 b_5 \\
R_4 &= a_4 b_0 + a_3 b_1 + a_2 b_2 \\
&\quad + a_1 b_3 + a_0 b_4 + a_5 b_5 \\
R_5 &= a_5 b_0 + a_4 b_1 + a_3 b_2 \\
&\quad + a_2 b_3 + a_1 b_4 + a_0 b_5
\end{aligned} \tag{10}$$

III. AOTP based Multiplier

This section presents the multiplication and addition gate which is the two main elements of the basic cell in the multiplier over $GF(3^m)$. The Down-Literal Circuit(DLC) [9] is mainly used to design the ternary gates. The multi-threshold property of DLC is applied with pass transistor logic.

3.1 The structure of multiplication gate

A multiplication gate follows the modular 3 multiplication operation over $GF(3^m)$, and the result value is obtained as Table 2 according to

multiplication truth table shown in Table 1. Fig. 2 shows the block diagram of the proposed multiplication gate.

V_x and V_y are the input voltage signals of the gate and the bias voltages are passed according to the condition of input signals. If input signals are 0 and 0, the pass transistor P_{33} , P_{34} , P_{35} and P_{36} are ON because each output signal of DLC is high. V_{out} is the output voltage signal of the gate which represents the ternary output value as 0 with 0 [V], 1 with 1.5 [V] and 2 with 3 [V], respectively.

To represent the symbol of ternary multiplication gate, we use the shape of AND gate in the binary logic because the output signals of the gate are similar to modular 3 multiplication results. To show the difference of the two gates, we added the character TMUL in the symbol. Fig. 3 shows the symbol of the multiplication gate.

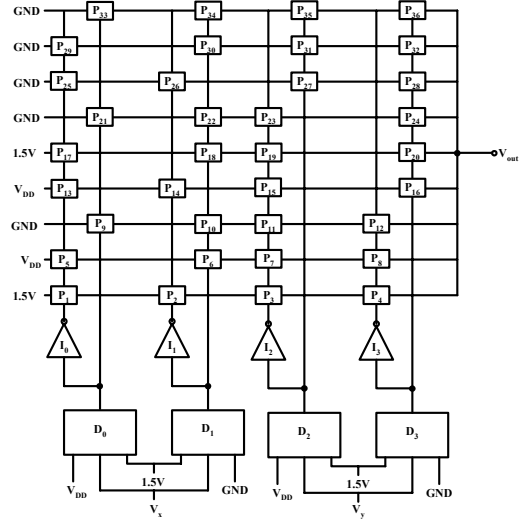


Fig. 2. The block diagram of ternary multiplication gate.

그림 2. 3차 승산 게이트의 블록도

Table 2. Output signal value of ternary multiplication gate

표 2. 3치 승산 게이트의 출력 신호표

V_{out}	V_x	V_y	D_0	D_1	D_2	D_3
1	2	2	L	L	L	L
2	1	2	L	H	L	L
0	0	2	H	H	L	L
2	2	1	L	L	L	H
1	1	1	L	H	L	H
0	0	1	H	H	L	H
0	2	0	L	L	H	H
0	1	0	L	H	H	H
0	0	0	H	H	H	H



Fig. 3. The symbol of ternary addition gate.

그림 3. 3치 승산 게이트의 심벌

3.2 The structure of multiplication gate

In the same manner as the multiplication gate, addition gate mainly consists of DLC and pass transistors. Addition gate follows the modular 3 addition operation over $GF(3^m)$, and the result value is obtained as Table 3 according to addition truth table shown in Table 1. Fig. 4 shows the block diagram of the proposed addition gate. And Fig. 5 shows the symbol of addition gate. We use the shape of Ex-OR gate in the binary logic because the output signals of the gate are similar to modular 3 addition results. To show the difference of the two gates, we added the character TADD in the symbol.

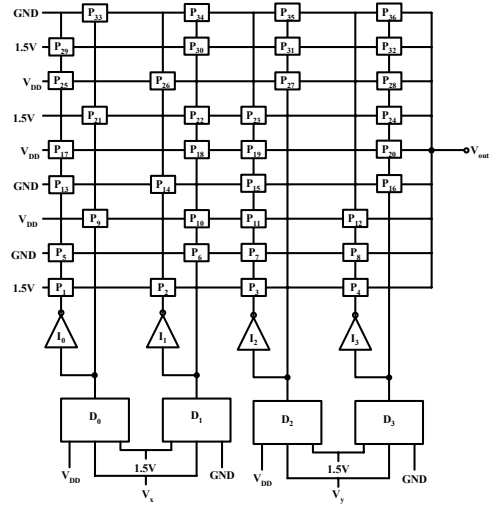


Fig. 4. The block diagram of ternary addition gate.

그림 4. 3치 가산 게이트의 블록도

3.3 Multiplier basic cell

In order to implement the AOTP multiplier over



Fig. 5. The symbol of ternary addition gate.

그림 5. 3치 가산 게이트의 심벌

Table 3. Output signal value of ternary addition gate

표 3. 3치 가산 게이트의 출력 신호표

V_{out}	V_x	V_y	D_0	D_1	D_2	D_3
1	2	2	L	L	L	L
0	1	2	L	H	L	L
2	0	2	H	H	L	L
0	2	1	L	L	L	H
2	1	1	L	H	L	H
1	0	1	H	H	L	H
2	2	0	L	L	H	H
1	1	0	L	H	H	H
0	0	0	H	H	H	H

$GF(3^m)$, we applied a multiplication algorithm over finite field $GF(3^m)$, and constructed the multiplier basic cell using addition and multiplication gate described in a previous section.

Fig. 6 shows the block diagram of basic cell in the multiplier over $GF(3^m)$. The cell input signals a_i and b_i represent the coefficients of the multiplier polynomial A and the multiplicand polynomial B, respectively. X is the other input signal which stems from the previous cell, and Y is the output signal of the cell.

Table 4 shows all 27 cases of the basic cell in the ternary multiplier. Signal flows are like this, first, the cell input ternary signals (a_i and b_i) are multiplied by ternary multiplication gate, and then the previous cell's output X and the output signal of multiplication gate are added by ternary addition gate. The output signal Y is not only the output of this stage but also the input signal of the next stage. In the multiplier, the cell's operation is processed iteratively.

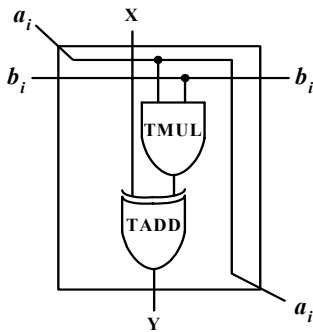


Fig. 6. Basic cell of multiplier over $GF(3^m)$.
그림 6. $GF(3^m)$ 상에서의 승산기 기본 셀

Table 4. Output signal value of basic cell in the ternary multiplier

표 4. 3차 승산기내 기본 셀의 출력 신호표

a_i	b_i	X	Y	a_i	b_i	X	Y	a_i	b_i	X	Y
2	2	0	1	2	2	1	2	2	2	2	0
1	2	0	2	1	2	1	0	1	2	2	1
0	2	0	0	0	2	1	1	0	2	2	2
2	1	0	2	2	1	1	0	2	1	2	1
1	1	0	1	1	1	1	2	1	1	2	0
0	1	0	0	0	1	1	1	0	1	2	2
2	0	0	0	2	0	1	1	2	0	2	2
1	0	0	0	1	0	1	1	1	0	2	2
0	0	0	0	0	0	1	1	0	0	2	2

3.4 The structure of ternary multiplier over $GF(3^m)$

This section presents the parallel-in parallel-out systolic architecture for computing ternary multiplication over $GF(3^m)$ in which the elements are represented with a root of an irreducible AOTP of degree m. For simplicity, the $GF(3^5)$ is used as example to illustrate the operation.

Fig. 7 shows the structure of ternary multiplier over $GF(3^5)$. a_i , b_i and R_i represent the coefficients of the multiplier polynomial A and the multiplicand polynomial B and multiplication result polynomial, respectively. The input 0 of the first stage represent that no input signals exist before the first stage.

IV. Simulation results and Comparison

The proposed ternary multiplier circuit has been simulated by HSPICE with model parameter for Hynix 0.35umCMOS process. Logical levels of the ternary input voltage(0,1,2)areassigned as 0, 1.5, 3 [V] and the reference voltages of the DLC block are 0 [V], $1/2V_{dd} = 1.5$ [V], and $V_{dd} = 3V$, respectively.

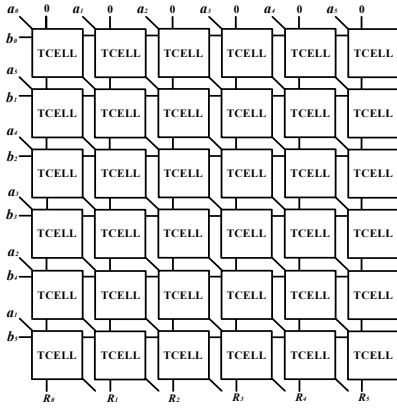
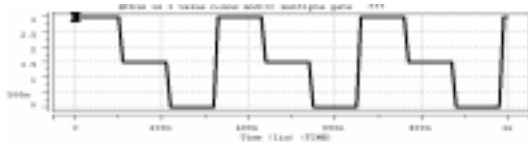


Fig. 7. The structure of AOTP multiplier over $GF(3^5)$.

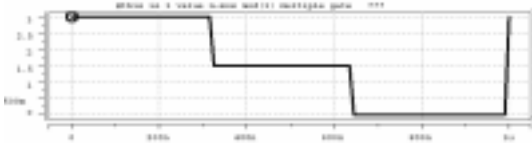
그림 7. $GF(3^5)$ 상에서의 AOTP 승산기 구조

4.1. Simulation results of gates

The input signals of the gate, V_x and V_y , are shown in Fig. 8(a) and (b), respectively. The cycle of the input signal is assigned as 300 [ns] and rising time as 10 [ns].



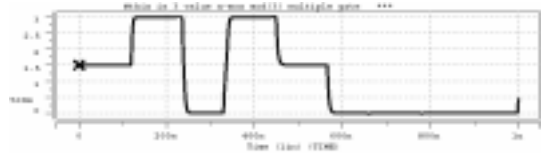
(a) Input signal V_x in the gate



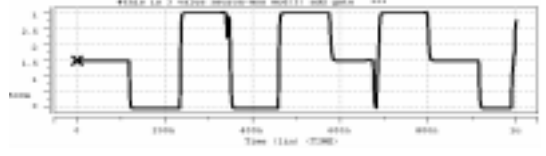
(b) Input signal V_y in the gate

Fig. 8. Input signals of the ternary gates
그림 8. 3치 게이트의 입력신호

Fig. 9 (a) and (b) show the output of the multiplication gate and addition gate. Simulation results represent the V_{out} of the table 3 and table 4, respectively. The output signals show 9 different stages in the table.



(a) The output signal of the multiplication gate



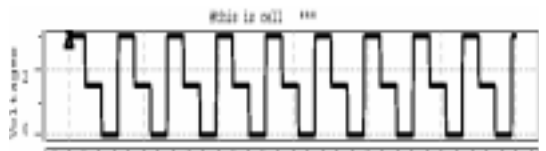
(b) The output signal of the addition gate

Fig. 9. Output results of the ternary gates

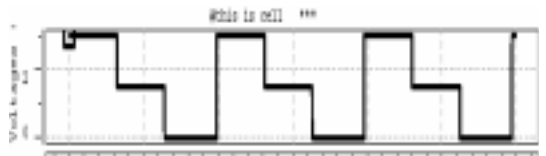
그림 9. 3치 게이트의 출력신호

4. 2. Simulation results of the basic cell

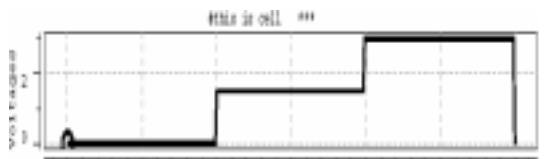
The input signals of the basic cell, V_x and V_y , are shown in Fig. 10 (a), (b), and (c), respectively. The cycle of the input signal is assigned as 300 [ns] and rising time as 10 [ns]. Fig. 10(d) shows the output of the basic cell. Simulation result represents the Y of the Fig. 6 and table 4. The output signals show 27 different stages in the table 4.



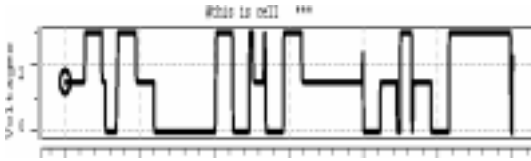
(a) Input signal V_x in the basic cell



(b) Input signal V_y in the basic cell



(c) Input signal X in the basic cell



(d) Output signal Y in the basic cell

Fig. 10. Simulation results of the basic cell in ternary multiplier.

그림 10. 3치 승산기의 기본셀 출력 결과

4.3. Multiplication over $GF(3^m)$

Assume that the coefficients of the AOTP A and B are $a_0=2, a_1=2, a_2=1, a_3=2, a_4=1, a_5=2$ and $b_0=1, b_1=1, b_2=2, b_3=1, b_4=2, b_5=1$. According to (3)-(8), the product of the multiplication A and B over $GF(3^m)$ can be obtained by (11).

$$\begin{aligned} A \bullet B &= R_0\alpha^0 + R_1\alpha^1 + R_2\alpha^2 \\ &+ R_3\alpha^3 + R_4\alpha^4 + R_5\alpha^5 \\ &= 2\alpha + \alpha^2 + 2\alpha^3 + \alpha^4 + 2\alpha^5 \quad (11) \end{aligned}$$

In this case, the coefficient outputs of the product result are static values, so we abbreviate the simulation results in this paper.

4. 4. Comparison

This section presents the compared data processing ability between the previous studies and this study.

We assumed that gates are same in all multipliers and focused on the number of gate in the multipliers. On condition that all multipliers calculates the same amount of information data, a multiplier over $GF(3^m)$ has the 1.5 times better data processing ability than a multiplier $GF(2^m)$. Though the proposed multiplier shows the similar number of gate with Lee's, the amount of processed data will be larger than that with the same propagation delay time.

Table 5 shows the structure comparison between this work and the previous works.

Table 5. Structure comparison table of multipliers
표 5. 승산기 구조 비교표

Multipliers Items	Yeh[2] $GF(2^m)$	Lee[7] $GF(2^m)$	This paper $GF(3^m)$
Gates per cell			
AND, 2 input	2	1	1
EX-or, 2 input	2	1	1
Ex-OR, 2 input	0	0	0
1 bit latch	7	3	0
Total Gates			
AND, 2 input	$2m^2$	$(m+1)^2$	$(m+1)^2$
EX-or, 2 input	$2m^2$	$(m+1)^2$	$(m+1)^2$
Ex-OR, 2 input	0	0	0
1 bit latch	$7m^2$	$(m+1)^2$	0
Gates with m = 5			
AND, 2 input	50	36	36
EX-or, 2 input	50	36	36
Ex-OR, 2 input	0	0	0
1 bit latch	175	144	0

V. Conclusions

In this paper, we have defined a ternary multiplication algorithm with AOTP over $GF(3^m)$ and designed the parallel-in parallel-out systolic multiplier circuit with using DLC and pass transistor logic.

Proposed multiplier has been constructed with lower number of gates and performs 1.5 times more information processing with comparing it with multipliers over $GF(2^m)$.

Simulations of the proposed ternary multiplier circuit were done by using HSPICE with model parameter for the Hynix 0.35m CMOS process. With the 3 [MHz] sampling rate, multiplier shows 4 [uW] power dissipation.

The layout of the proposed circuit is one of our further studies and extension of field over $GF(p^m)$ is expected.

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