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Design of a CMOS Time to Digital Converter with 25ps Resolution

25ps 해상도를 가진 CMOS Time to Digital 변환기설계

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ABSTRACT

This paper describes a CMOS time to digital converter (TDC) that measures the interval between two signals and converts to a digital signal. There are various methods to measure the time interval. But several architectures have a limitation in resolution and in conversion time. Moreover, they have complex algorithms. But the proposed TDC circuit has achieved a high resolution (25ps) by using a high-speed digital sampler and simple algorithm. The sampler detects when input signals comes into the TDC and output is coded. The proposed multiphase clock generator was also implemented to achieve 25p resolution.

요 약

본 논문은 두 신호의 시간 차이를 디지털 신호로 변환하는 시간디지털변환기(Time to Digital Converter) 변환기에 대해서 서술하였다. 시간 차이를 측정하는 방법에는 여러 가지가 있으나 변환시간이나 저해상도의 단점을 가지고 있으며 또한 복잡한 구조를 가지는 문제점이 있다. 그러나 본 논문에서 제안한 시간디지털변환기회로는 고속 디지털 샘플러를 사용함으로써 단순한 구조로 높은 해상도(25ps)를 실현할 수 있었다. 입력신호가 시간디지털변환기의 입력으로 들어오면 샘플러가 신호를 검출해내고 레지스터에 의해 처리된 후 코딩블럭에 의해서 코딩되게 된다. 또한 25ps의 해상도를 얻기 위해서 본 논문에서는 다중위상클록발생기를 구현하였다.

Keyword: 다중위상발생기, TDC

I. Introduction

The time to digital converter(TDC) is a device that measures the time difference between two signals. And it digitizes the time interval of these signals. CMOS time to digital converters are required in applications such as pulsed time of flight (TOF) laser range-finders and instrumentation for particle science experiment [1][2][3][4].

There are numerous methods to measure time difference of two signals. The simplest method for measuring signal time difference is to use a N-bit counter. When the first signal comes into the device, the counter starts to operate and it stops when the last signal gets into the counter. Though the upper method has a very simple architecture and a capability of measuring long time distance, it has a limitation on the timing resolution. Therefore it is impossible to measure difference among fine signals such as pico-scale pulses or jitters.

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One of most important design issues in TDC circuit is how precise the resolution can be achieved. In order to achieve very fine timing resolution, high-speed digital samplers in this paper were employed by TDC. The sampler can detect the time difference of input signals by means of 25ps resolution sampling. The time stamp information by samplers used to readout at coding block. Another important part to achieve fine resolution in the proposed TDC is a multiphase clock generator. The proposed multiphase clock generator will be mentioned later. In section 2, the proposed architecture and algorithm are presented. The multiphase clock generator is described in section 3. In section 4 we describes the interval calculation between two signals and HSPICE simulation followed by conclusion.

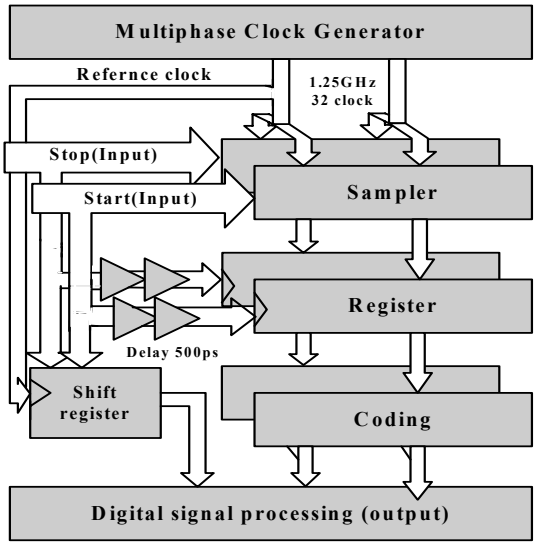

Fig.1. Block diagram
그림 1. 전체 블록도

II. Proposed Architecture and Algorithm

Figure 1 shows the block diagram of the proposed time to digital converter circuit. It is composed of a multiphase clock generator for achieving a very fine resolution of LSB, 5bit shift register block for long time measurement and coding block for readout..

This section explains how to detect START and STOP input signals and how to calculate the timing difference between two signals. First, 1.25GHz 32 multiphase clocks from the clock generator go into the two sampler blocks (start block and stop block). The sampler block is also composed of 2 sub-blocks. The first sub-block is sampler bunch that is composed of 32 samplers. There are two bunchs of sampler for processing each START and STOP input signals. All inputs of samplers are connected in parallel. The second sub-block is R-S latch bock for storing the sampled value. They are also connected in each sampler. Figure 2 shows the sampler used in this paper [5].

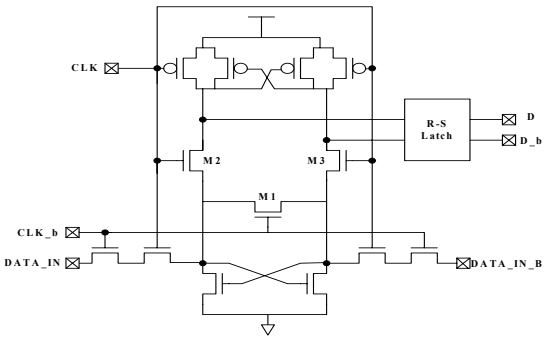

Fig. 2. Digital Sampler schematic
그림 2. 디지털 샘플러

The operation of sampler is as follow. If the START signal comes into the one sampler block, the 32 samplers start to sample it for detecting time stamp information of input signal. Each sampler generates 'high' signal when the input signal is sampled by clocks at higher voltage point than certain bias voltage(1.65V at 3.3V power supply). Figure 3 represents the sampling process. But if the sampler samples input signal forever, it is difficult to know when the START signal comes into the sampler block. Therefore it is required that a few

initial sampling values be stored. As shown in the figure 1, another delayed START signal comes into the register block for clocking. By HSPICE simulation the delay was set to be 500ps. The first sampling value has the latency 400ps and the next sampled data start to come out continuously in 25ps interval.

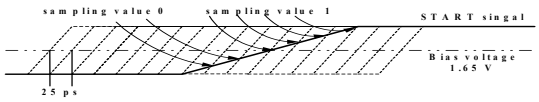

Fig. 3. Sampling process
그림 3. 샘플링 과정

Since there is a relation between input data (Start a nd Stop signal) and the sampling clocks, the time st amp information can be calculated based on the sam pler outputs. For example, if the third sampler's out put becomes firstly 'high', it can be said that the in put time of START or STOP signal is a middle poi nt of second and third clock.
The output information means that input data came apart 50ps from reference clock(1^{st} clock).

By the way, if the number of 'high' signals is not fixed exactly, there may be some problems at coding process. To prevent this problem, the other sampling data except for the first sampling datum must be changed to 'low' signals. Figure 4 represents 2:1 MUX block. It can detect when firstly high signal comes from samplers. if the first 'high' signal is generated by the third clock, the third MUX only generates 'high' signal and other MUXs generate 'low' signals.

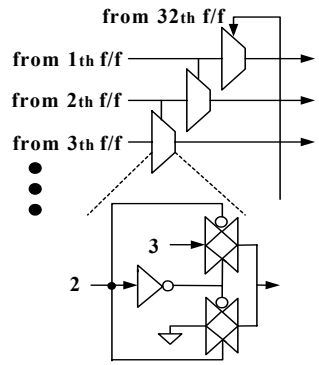

Fig. 4. 2:1 MUX block
그림 4. 2:1 MUX 블록

The each output of MUXs used for 5bit digital value of coding block. It means that the time interval between reference clock and START or STOP signal. The operation of shift register is as follow. The reference signal from clock generator goes into the shift register block at figure.1. When the START signal is loaded to the shift register, it counts every reference period (775ps). And then, when the STOP signal comes into the shift register, it is stopped because the STOP signal disconnects the reference clock from shift register.

Since the single sampler has 32 stamping stages,the time interval of 775ps (31*25ps) can be measured from the sampler. In order to increase the measuring range, the 5bit shift register is added and the measuring range is expanded to 4.775ns.The reference signal from clock generator goes into the shiftregister block as shown in figure. 1. When the START signal is clicking the shift register, the shift register records the number of reference clocks. And then, when the STOP signal comes into the shift register, it stops recording.

III. Multiphase clock generator

As mentioned before, it is very important to implement multiphase clock generator with fine resolution. This chapter describes a new approach to make a precise fine clock generator for sampling clocks. Delay locked loop structure is based on the

proposed multiphase clock generator. Generally, the delay locked loop circuit is composed of phase detector, loop filter and voltage controlled oscillator. It is fit for clock generator because jitter is not accumulated by feed back loop unlike phase locked loops [4]. The proposed clock generator circuit composed of charge pump, loop filter, phase detector and 19 delay stages including 2 dummy delay stages for equally keeping the load. The block diagram of the multiphase clock generator is presented in figure. 5. It has charge pump(CP), phase detector(PD) and delay chain(D).

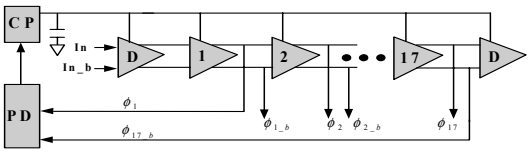

Fig. 5. Multiphase clock generator
그림 5. 다중위상클록 발생기

The clock generator makes 32 differential clocks which have 25ps resolution. But it is hard to implement a delay cell which has 25ps delay which is less than minimum gate delay. Normally the gate delay of simple static inverter at 0.35um process is about 100ps. And so the proposed method in this paper is to make a delay stage which has long delay of 425ps as shown in the figure 6.

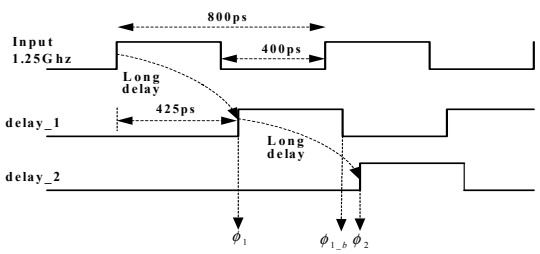

Fig. 6. Concept of Multi clock generator
그림 6. 다중위상클록 발생기의 개념

The delay value of 425ps comes from a half of external input clock period plus the required resolution 25ps. The delay drags 1.25GHz input clock signal by a half period. Among all signals from each delay stage the phase difference between clock signal from first delay stage and the signal from 17th delay stage become zero. After 8 cycles plus 1/2 cycle, 16 clocks with 25ps phase resolution can be obtained in a last half period. Including their differential signals, 32 signals can be obtained. The proof for the proposed clock generator is done by HSPICE simulation, which will be presented later.

IV. Calculation and Simulation Result

Figure 7 is the timing diagram for calculation of time difference between two input signals. Final 5bit data are a digital value for Tstart and Tstop. In case the time interval to be measured is more than 800ps, shift register counts until stop signal comes. Finally the time difference between two inputs is obtained by following equation.

(Shift register value) * (800ps) + (START digital value) * (25ps) (STOP digital value) * (25ps)
= Time difference between two signals.

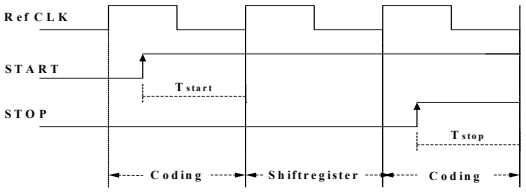

Fig. 7. Timing diagram
그림 7. 시간 흐름도

The HSPICE simulation was used to verify the proposed algorithm with following process. First, the simulation of 25ps multi-phase clock generator is done. Figure 8 represents 1.25GHz 32 different phase clocks with 25ps resolution and the control voltage to regulate delay of each delay stage.

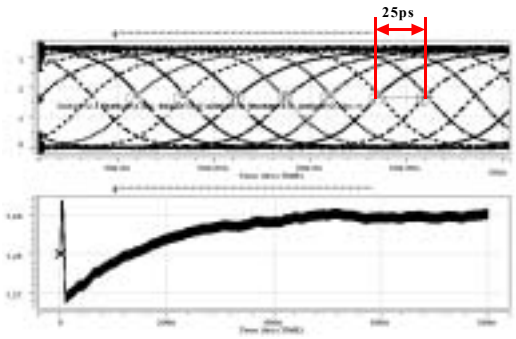

Fig. 8. 25ps resolution clocks and bias voltage
그림 8. 25ps 해상도를 갖는 클록들과 바이어스 전압

Figure 9 represents the results when the time difference between START and STOP signal has been set with 1700ps. Figure 9 indicates that digital value related START input signal is 11011(27) and STOP is 10111(23). Next information are measured data.

(START - STOP) = 27 - 23 = 4
Shift register value = 2
Total value = 2 * 800ps + 4 * 25 ps = 1700ps

Finally we can know that intended time interval equal to the value, which is measured by this time-to-digital converter.

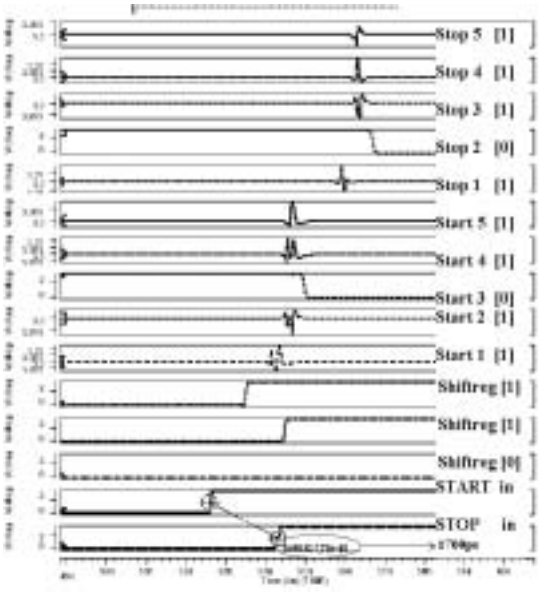

Fig. 9. Final simulation result
그림 9. 최종 모의실험 결과

V. Conclusion

This paper has described a time to digital converter that has a very fine timing resolution of 25ps. The high resolution can be realized by using a high-speed digital sampler. The sampler contributes to detect START and STOP input time. After detecting, data are coded. Total power dissipation was 177mW in simulation. This circuit was designed under 3.3v supply voltage and simulated 0.35um CMOS process. Figure 10 shows the proposed TDC layout.

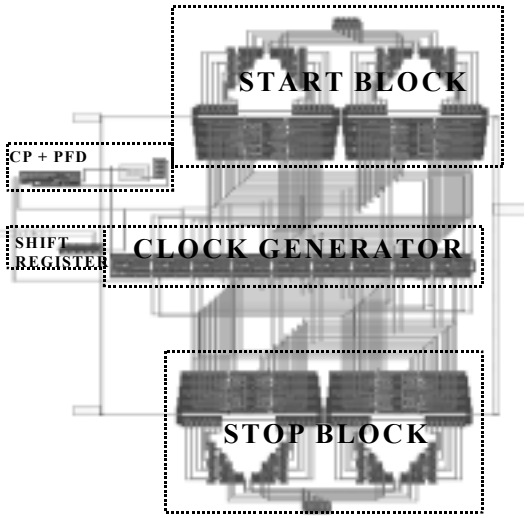

Fig. 10. TDC layout
그림 10. TDC 레이아웃

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