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Design of Quaternary Logic gate Using Double Pass-transistor Logic with neuron MOS Threshold gate

뉴런 MOS 임계 게이트를 갖는 2중 패스-트랜지스터 논리를 이용한 4치 논리 게이트 설계

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Abstract

A multi-valued logic(MVL) pass gate is an important element to configure multi-valued logic. In this paper, we designed the Quaternary MIN(QMIN)/negated MIN(QNMIN) gate, the Quaternary MAX(QMAX)/negated MAX(QNMAX) gate using double pass-transistor logic(DPL) with neuron MOS(νMOS) threshold gate. DPL is improved the gate speed without increasing the input capacitance. It has a symmetrical arrangement and double-transmission characteristics. The threshold gates composed by νMOS down literal circuit(DLC). The proposed gates get the valued to realize various multi threshold voltages. In this paper, these circuits are used 3V power supply voltage and parameter of 0.35um N-Well 2-poly 4-metal CMOS technology, and also represented HSPICE simulation results.

요 약

다치 논리 패스 게이트는 다치 논리를 구성하기 위한 중요한 소자이다. 본 논문에서는, 뉴런 MOS(νMOS) 임계 게이트를 갖는 2중 패스-트랜지스터 논리를 이용하여 4치 MIN(QMIN)/negated MIN(QNMIN) 게이트 그리고 4치 MAX(QMAX)/negated MAX(QNMAX) 게이트를 설계하였다. DPL은 입력 캐패시턴스의 증가 없이 게이트 속도를 향상 시켰다. 또한 대칭 배열과 2중 전송 특성을 갖는다. 임계 게이트는 νMOS 다운 리터럴 회로(DLC)로 구성된다. 제안된 게이트는 다양한 다치 임계 전압을 실현할 수 있다. 본 논문에서, 회로는 3V의 전원 전압을 사용하였고 0.35um N-Well 2-poly 4-metal CMOS 공정의 파라메터를 사용하였으며 모든 모의 실험은 HSPICE를 이용하였다.

Keyword : quaternary, DPL, QMIN/QNMIN, QMAX/QNMAX

I. INTRODUCTION

According to the development of MVL theory, the need for MVL circuit design is increased. Two kinds of MVL circuit generally used, voltage-mode and current-mode. Current-mode MVL circuits have power consumption serious problem. Conversely, voltage-mod MVL circuits have the advantage of low power consumption. But since they require the multi-level ion implantation process technology to realize multi-threshold voltages in MOS transistors, complex fabrication and high cost are inevitable[1].

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In order to solve these problems, we try to use a general CMOS process to realize voltage-mode MVL circuits. A pass gate is a popular way to realize a MVL function. The algorithm for simplification of pass gate has already been developed[2][3].

A neuron-MOS(νMOS) is a kind of novel transistor device with multi-input gates[4]. The ν MOS is characterized by a variable threshold voltage achieved by controlling the voltages of the multi-input gates.

To voltage-mode MVL circuits, we present a ν MOS down literal circuit(DLC) in this paper. νMOS DLC is applied to MVL pass gate as the threshold gate, and the MVL pass gate can be fabricated with the common CMOS process[5].

Double pass-transistor logics(DPL)[6] gain their speed advantage over CMOS due to their high logic functionality. Also DPL has been developed to improve circuit performance at reduced supply voltage. A symmetrical arrangement and the double-transmission characteristics of the DPL gate compensate for the speed degradation due to the usage of both PMOS and NMOS pass transistors.

In this paper, we designed the quaternary logic gate using the DPL with νMOS threshold gate that has multi-threshold voltage. The νMOS threshold gate is designed using DLC. The quaternary logic gates include the quaternary MIN(QMIN)/negated MIN(QNMIN) and quaternary MAX(QMAX)/negated MAX(QNMAX). These proposed gates are confirmed by HSPICE simulations with 0.35um 2-poly 4-metal CMOS technology and 3V power supply voltage.
The MOS MVL circuits can be realized without the multi-level ion implantation process technology. The ease of fabrication will make MVL circuits more practically.

II. QUATERNARY LOGIC GATES

2.1. νMOS

The basic structure of the functional νMOS transistor is shown in Fig.1. It is an n-channel ν MOS transistor having a gate electrode which is electrically floating. The multi-input gates are capacitively coupled to the floating gate. The terminal voltages and various capacitive coupling coefficients are defined in Fig.2, where Φ_F is the floating-gate potential, V_1, V_2,⋯,V_n are the input signal voltages, C_1, C_2,⋯,C_n the capacitive coupling coefficients between the floating gate and each of the input gates, C_0 is the capacitive coupling coefficient between the floating gate and the substrate, and Q_1, Q_2,⋯ ⋯,Q_n are the stored charges in each of the capacitors. A symbol representing the device is given in Fig. 3.

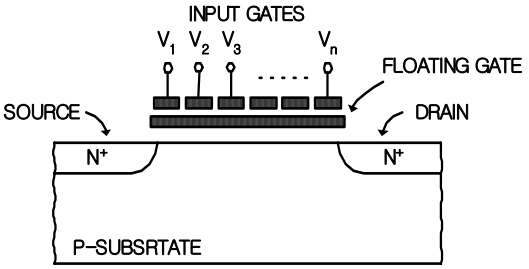


그림 1. MOS의 기본 구조
Fig. 1. The basic structure of MOS

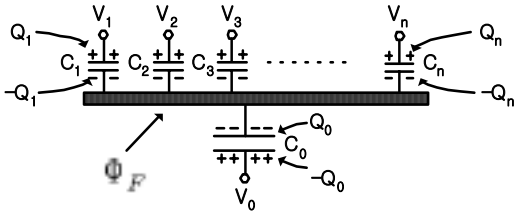


그림 2. 게이트 전압과 커패시터와의 관계
Fig. 2. Relationship among terminal voltages and capacitance coupling coefficients

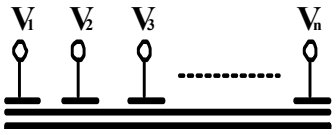


그림 3. νMOS 심볼
Fig. 3. The symbol of the νMOS

2.2. DLC

A DLC is the fundamental element in MVL circuits. MVL logic functions are almost always developed from the down literal function, and most MVL circuits consist of DLC. The down literal function is by Eq.(1).

$$D_i(x) = \begin{pmatrix} R-1 & x \le i \\ 0 & x \ge i+1 \end{pmatrix} \quad (1)$$

Where, $i \subseteq \{0,1,\cdots,R-2\}$, $x \subseteq \{0,1,\cdots,R-1\}$.

The ▼MOS DLC consists of p-channel ▼MOS (P▼MOS) and n-channel ▼MOS (N▼MOS) as shown Fig.4.

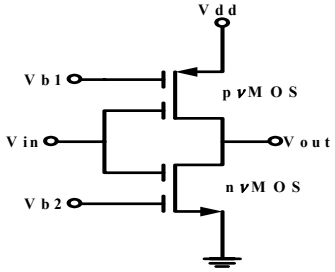


그림 4. ▼MOS DLC의 회로
Fig.4. Circuit description of ▼MOS DLC

The common input to P▼MOS and N▼MOS, V_{in} is taken as the input of the DLC, and V_{b1}, V_{b2} are bias voltages. V_{TC} shown in Eq.(2).

$$V_{TC} = V_{DD} - \frac{V_{b1} + V_{b2}}{2} \quad (2)$$

Here, the restriction of V_{b1}, V_{b2} is derived from saturation condition of ▼MOS transistors in the circuit. V_{TC} of this circuit can be varied by controlling the values of the bias voltages(V_{b1}, V_{b2}), and different down literal functions can be implemented.

2.3. Threshold gate

According to Eq.(2), the quaternary DLC can be designed. There are three kinds of down literal functions in the quaternary system. $D_i(x)(i=0,1,2)$ can be attained by setting V_{b1} and V_{b2} to the values stated in Table 1.

표 1. 바이어스 전압에 따른 V_{TC}의 변화
Table 1. The transformation of V_{TC} about Bias voltage

V_{DD}=3.3V	V_{TC}	V_{b1}	V_{b2}
V_{th}(0.5)	0.5V	3V	2V
V_{th}(1.5)	1.5V	2.2V	0.8V
V_{th}(1.5)	2.5V	1V	0V

The symbols of the threshold gates are show in Fig. 5 and also its transfer characteristic of the threshold gates.

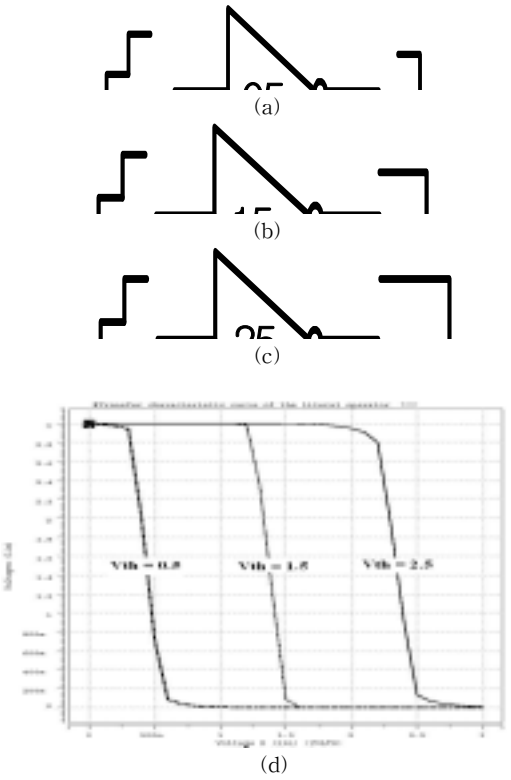


그림 5. (a)V_{th}=0.5 (b)V_{th}=1.5 (c)V_{th}=2.5 (d)전달 특성 곡선
Fig. 5. (a)V_{th}=0.5 (b)V_{th}=1.5 (c)V_{th}=2.5 (d)Transfer characteristic curve

The truth table of quaternary literals is listed in Table 2.

표 2. 4치 리터럴의 진리표
Table 2. The truth table of the quaternary literals

X	X^0	X^1	X^2	X^3	X^{01}	X^{02}	X^{12}	X^{13}	X^{23}
0	3	0	0	0	3	3	0	0	0
1	0	3	0	0	3	3	3	3	0
2	0	0	3	0	0	3	3	3	3
3	0	0	0	3	0	0	0	3	3

2.4. DPL

Suzuki et al.[6] proposed the DPL that overcomes all the problems of complementary pass-transistor logic(CPL), namely, when implementing CPL, particularly in reduced supply voltage designs, it is import to take into account the problems of noise margins and speed degradation.

DPL consist of both nMOS and pMOS pass

transistors, in contrast to CPL. So DPL give improved circuit performance at reduced supply voltage.

The CPL consists only of nMOS transistors, resulting in low input capacitance and high-speed operation. However, the abovementioned problems are caused by the high output signal level being lower than the supply voltage Vcc by the nMOS threshold voltage Vth. The usual way to avoid this is to use CMOS pass-transistor logic. Full-swing operation is attained by simply adding pMOS transistor in parallel with the nMOS transistors. In the DPL, the inputs to the gates of the pMOS transistor are changed. This arrangement compensates for the speed degradation of CMOS pass-transistors. DPL are symmetrical whereby the load in any DPL is distributed equally among the inputs. This result in a balanced input capacitance and reduces the dependence of the delay time on data. Also DPL has double-transmission characteristics[6].

2.5. QMIN/QNMIN,QMAX/QNMAX

We proposed the QMIN/QNMIN circuit. The QMIN operation is shown as Eq.(3). The operator $\cdot$ or $\wedge$ is QMIN operation.

$$x_1 \bullet x_2 \bullet \cdots \bullet x_n = QMIN(x_1, \cdots, x_n)$$
$$x_1 \wedge x_2 \wedge \cdots \wedge x_n = QMIN(x_1, \cdots, x_n) \quad (3)$$

A QMIN function shown in Table 3 is represented to Eq.(4).

표 3. QMIN 진리표
Table 3.The truth table of QMIN

B \ A	0	1	2	3
0	0	0	0	0
1	0	1	1	1
2	0	1	2	2
3	0	1	2	3

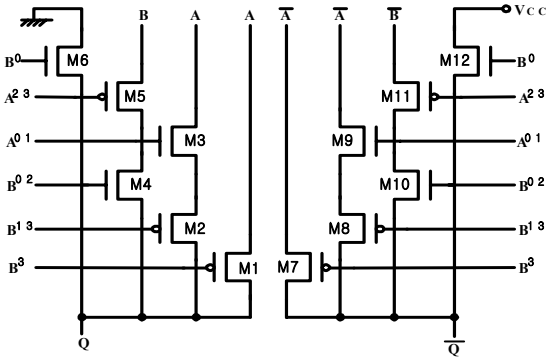
According to Eq.(4), (5) QMIN and QNMIN can be easily configured using DPL with MOS threshold gate.

$$Y = 0 < B^0 > + A < A^{01}, B^{13} > + B < A^{23}, B^{02} > + A < B^3 > \quad (4)$$

$$Y = 3 < B^0 > + \overline{A} < A^{01}, B^{13} > + \overline{B} < A^{23}, B^{02} > + \overline{A} < B^3 > \quad (5)$$

Where Fig.6(b), two input A and B are connected in the gate of pass transistor. MOS are turned on or turned off by the input value. Therefore, the output value is generated by QMIN/QNMIN operation.

(a)



(b)

그림 6. (a)QMIN/QNMIN의 심볼 (b)QMIN/QNMIN의 회로
Fig. 6. (a)Symbol of the QMIN/QNMIN. (b)A circuit of the QMIN/QNMIN.

For example, when input A is 2 and B is 3, M3, M9 are turned off and M5, M11 are turned on by input A, and M4, M10, M6, M12 turned off and M1, M7, M2, M8 turned on by input B, therefore, the output is "Q=2, $\overline{Q}$ =1"

Similarly, QMAX/QNMAX operation is shown as Eq.(6). The operator $\vee$ or $\oplus$ is QMAX operation.

$$x_1 \vee x_2 \vee \cdots \vee x_n = QMAX(x_1, \cdots, x_n)$$
$$x_1 \oplus x_2 \oplus \cdots \oplus x_n = QMAX(x_1, \cdots, x_n) \quad (6)$$

A QMAX function shown in Table 4 is represented to Eq.(7).

표 4. QMAX의 진리표
Table 4. The truth table of QMAX

A / B	0	1	2	3
0	0	1	2	3
1	1	1	2	3
2	2	2	2	3
3	3	3	3	3

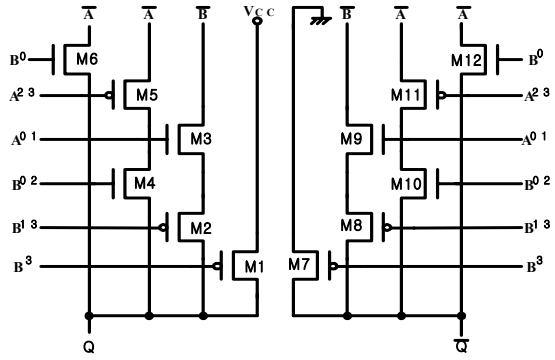
According to Eq.(7), (8) QMAX and QNMAX can be easily configured using DPL with MOS threshold gate.

$$Y = 3 < B^3 > + A < A^{23}, B^{02} > + B < A^{01}, B^{13} > + A < B^0 > \quad (7)$$

$$Y = 0 < B^3 > + \overline{A} < A^{23}, B^{02} > + \overline{B} < A^{01}, B^{13} > + \overline{A} < B^0 > \quad (8)$$

In Fig.7(b), the operation of QMAX/QNMAX same as the operation of the QMIN/QNMIN.
Also for example, when input A is 2 and B is 3, M3, M9 are turned off and M5, M11 are turned on by input A, and M4, M10, M6, M12 turned off and M1, M7, M2, M8 turned on by input B, therefore, the output is "Q=3, $\overline{Q}$ =0"

(a)



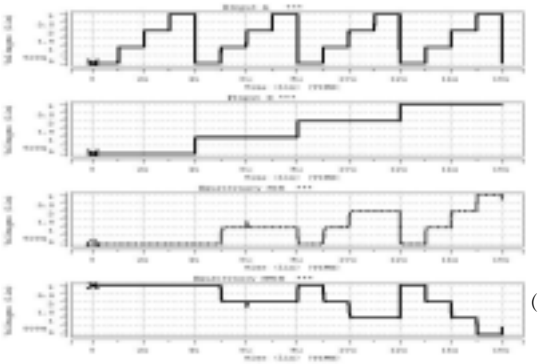
(b)

그림 7. (a)QMAX/QNMAX의 심볼 (b)QMAX/ QNMAX의 회로
Fig. 7. (a)Symbol of the QMAX/QNMAX. (b)A circuit of the QMAX/QNMAX

III. SIMULATION RESULTS

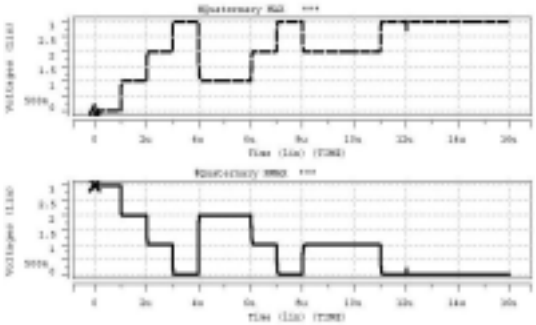
The HSPICE simulation of QMIN/QNMIN and QMAX/QNMAX are shown in Fig. 8(a) and (b), respectively.

The power dissipation, QMIN/QNMIN and QMAX/ QNMAX have 4.898uW. Each component is designed at the sampling speed of 0.25MHz.



a)

(b)



(c)

그림 8. 모의 실험 결과 (a) 입력 (b)QMIN/QNMIN (c)QMAX/QNMAX
Fig. 8. Simulation results (a) Input (b)The QMIN/QNMIN (c)The QMAX/QNMAX

IV. CONCLUSION

In this paper, we designed the quaternary logic gates such as QMIN/QNMIN and QMAX/QNMAX using double pass-transistor logic with neuron MOS threshold gate. The circuit verification of these logic circuits are verified by HSPICE simulation with CMOS 0.35um device parameter. Furthermore, we expect the implementation of quaternary full adder using the proposed the quaternary gates.

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