The Study for Transient Enhanced Diffusion of Indium and Its Application to 0.13 μm Logic Devices

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We developed a new systematic calibration procedure which was applied to the calibration of the diffusivity, segregation and TED model of the indium impurity. The TED of the indium impurity has been studied using 4 different groups of experimental conditions. Although the indium is susceptible to the TED, the RTA is effective to suppress the TED effect and maintain a steep retrograde profile. Like the boron, the indium shows significant oxidation-enhanced diffusion in silicon and has segregation coefficients at the Si/SiO_2 interface much less than 1. In contrast, however, the segregation coefficient of indium decreases as the temperature increases. The accuracy of the proposed technique is validated by SIMS data and 0.13 μm device characteristics such as V_{th} and Id_{sat} with errors less than 5 % between simulation and experiment.

Keywords : Indium, Transient enhanced diffusion, Logic devices, Calibration, Simulation

1. INTRODUCTION

Indium, an acceptor dopant in Si, is an alternative of the boron impurity in the channel region for achieving a retrograde channel profile and reduces the SCE (Short Channel Effect) in sub 0.13 μm MOSFETs. This SCE increases the sensitivity of the device electrical behavior to the technological process, via transient effects associated with RTP (Rapid Thermal Processing)[1,2]. Although some results have been published for the behavior of the indium impurity in the inert and oxidizing ambient[3-5], limited data exist for the TED (Transient Enhanced Diffusion) of indium in the RTA (Rapid Thermal Anneal) process[6]. Indium could make a steep channel profile due to its lower diffusivity and strong segregation into the oxide. In this study, the TED phenomena of the indium impurity in silicon are investigated in the range of damage generation from the high energy implantation for the well formation and heavy-dose implantation for the source/drain formation. In addition, the indium profile is systematically calibrated as a newly defined impurity in a process simulator. Finally, we demonstrate the results of 0.13 μm logic devices to which the indium impurity has been applied in the channel region to suppress the RSCE (Reverse Short Channel Effect) and enhance the device performance compared to the boron channel device.

2. EXPERIMENT AND CALIBRATION

The new systematic calibration procedure of a process simulator for the indium impurity is shown in Fig. 1. Unpatterned <100> oriented p-type silicon wafers were implanted with the indium impurity.

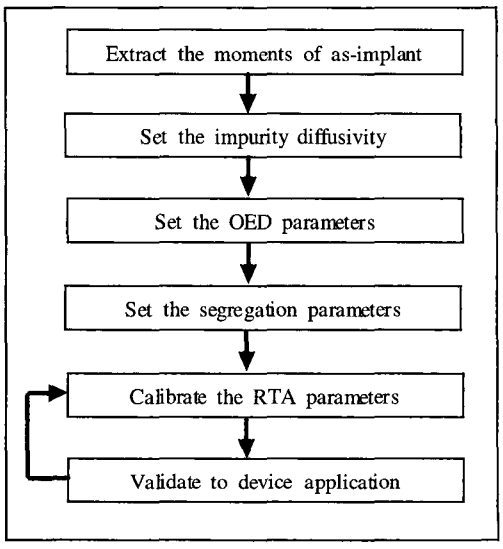

Fig. 1. The process simulator calibration procedure for indium impurity.

The implant energy was varied between 120 KeV and 180 KeV. The dose was varied between 6.0×10^{12} and 1.4×10^{13} cm^{-2}. First, from the as-implanted indium SIMS profiles, we extracted 9-moments of the dual-pearson model. The as-implanted calibration results agree well with SIMS data as shown in Fig. 2. Second, the diffusivity parameters and the enhancement factor with segregation parameters during oxidation for the simulation model were taken from the previous results [7,8]. It is assumed that the equations governing the diffusion of indium in silicon are identical to those for the other dopants[9]. These results show that both of indium and boron experience significant oxidation-enhanced diffusion in silicon and has segregation coefficients at the Si/SiO_2 interface much less than 1 at temperatures between 800 ℃ and 1050 ℃.

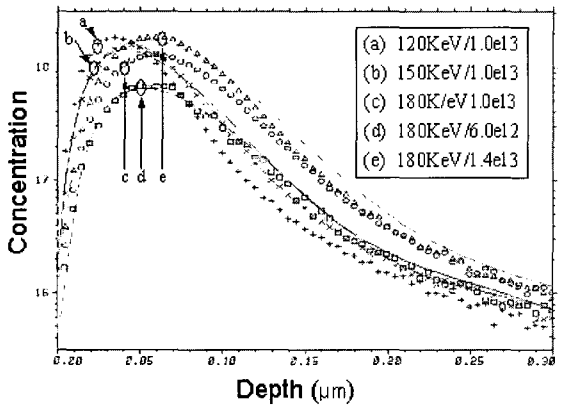

Fig. 2. The calibration results of the as-implanted indium impurity compared to SIMS data.

However, the segregation coefficient of indium decreases as the temperature increases. In order to analyze the TED phenomena of the indium, we performed 4 groups of experiments as listed in Table 1.

Table 1. Four groups of experimental conditions to analyze the TED phenomena of indium and boron in silicon.

Group	RTA	Oxidation	As-implant	RTA
A	X	O	X	O
B	O	O	X	O
C	O	O	O	O
D	X	O	O	O

The boron impurity was also experimented under the same conditions for comparison. The purpose of these conditions is to extract the damage effect of the phosphorus high-energy implantation for the well formation and the arsenic heavy-dose implantation for the source/drain formation. The experiment was carried out as follows. Starting from the as-implanted wafers, the first RTA is performed prior to the oxidation on B and C groups only. Then, dry oxidation (850 ℃/30 min.) and inert annealing (900 ℃/20 min.) are applied to all wafers. To monitor how the TED affects the channel impurity redistribution, the damage generation is made on C and D groups by high dose (5.0×10^{15} cm^{-2}) arsenic implantation which is the condition for the source/drain process. Finally, the second RTA (1000 ℃ /30 sec) is processed. The SIMS data were obtained after removing the oxide layer. The TED calibrations are done with TSUPREM4 using a fully coupled model for dopant diffusion and a scaled "+ 1" model to account for point defects created by the implant damage[10,11]. The scaled damage factor is approximately 1-1.2 interstitials per implanted ion for phosphorus and 2-2.3 for arsenic. The simulation profiles for the final indium dopant show good agreement with the SIMS profiles as shown in Fig. 3.

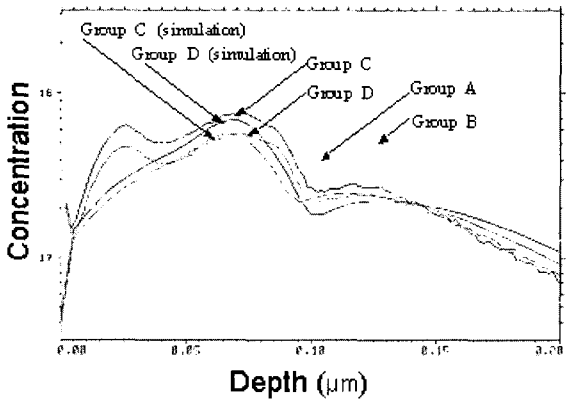

Fig. 3. The comparison of simulation results to SIMS data for the indium TED effects.

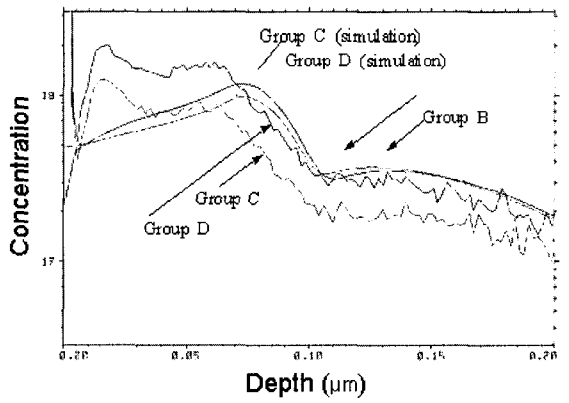

Fig. 4. The comparison of simulation results to SIMS data of the boron TED effects.

The diffusion profiles are also calibrated as accurately as possible, because we analyzed the accuracy of doping profiles according to the variation of threshold voltages in 0.13 μm device, where 1 % of channel profile can affect 50 % of threshold voltage variation. Thus, if we predict the accuracy of threshold voltage within 10 % compared to real data, we should calibrate the channel doping profile within 0.2 % error. The SIMS profiles of Figs. 3 and 4 have the first peak at 200 Å depth. However, the SIMS data seem to be not correct in this region so that we do not perform the calibration. Compared to the boron TED as shown in Fig. 4, the indium has the lower peak concentration and the surface concentration is much lower than the boron.

3. APPLICATION

To validate our calibrated RTA model parameters for the indium, we applied the parameters to the 0.13 μm logic devices. Table 2 is the process flow for CMOS logic transistors with cobalt silicide contacts.

Table 2. The process flow of CMOS logic devices with Co-salicide contacts.

• Active photo and trench etch for STI
• N-Well implantation
• RTA (Option)
• V_{th} implantation of NMOS and PMOS
• Oxidation for formation of gate oxide
• Deposition and pattering of gate poly-Si
• N- and P- source/drain implantation
• RTA (Option)
• Formation of Spacer
• N+ S/D implantation and RTP anneal
• P+ S/D implantation and RTP anneal
• Deposition of cobalt film
• Silicidation
• Metallization

In this process, the indium is implanted instead of the boron through a 110 Å screen oxide layer to adjust the threshold voltage. Figure 5 shows the simulated and experimental data of RSCE for both of the indium and the boron implanted devices. If the TED effect is not included in the indium implantation, the RSCE cannot be modeled[12,13]. Using the TED calibration, we can improve the RSCE estimation by about 20 %. The indium profile at the center of the channel gets broader and the surface concentration increases as the gate length reduces. As the interstitials diffuse laterally from the S/D to the channel region, the channel profile gets broader. In addition, the surface concentration pile-up is the result of the gradient in the interstitial concentration produced by recombination at the silicon/oxide interface. The gradient in the interstitial concentration produces the gradient of dopant/interstitial pairs resulting in the diffusion of these pairs towards the Si/SiO_2 interface. The gradient of interstitials towards the surface increases as the channel length decreases; thus, the flux of dopant/defect pairs increases. Due to the strong segregation combined with the TED effect of the indium impurity into the gate oxide, the indium pile-up near the surface is reduced, and consequently, the RSCE of an indium-channel device is smaller than that of a boron-channel device. The V_{th} roll-up is reduced from 70 to 40 mV and the slope of the roll-off is reduced from 150 to 90 mV. In Fig. 6, Id_{sat} vs. Id_{off} curves also show the excellent agreement between simulation and experiment results, which indicates that the slope of the indium curve is lower than that of the boron case and Id_{sat} is enhanced by 4.4 % at Id_{off} of 10 nA/μm.

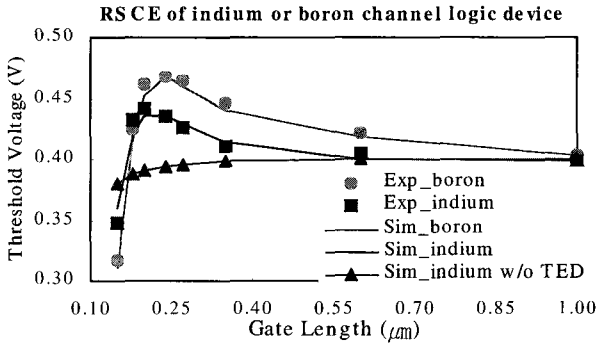

Fig. 5. The simulation and experimental data of RSCE of a logic device with the indium implanted channel.

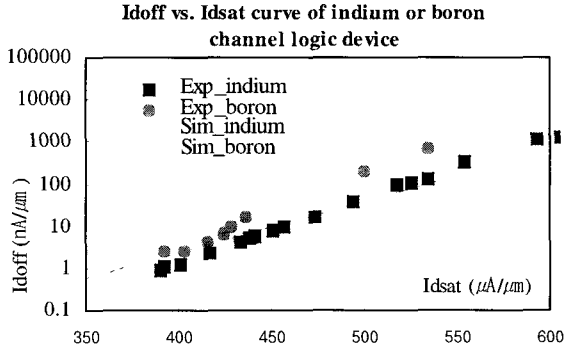

Fig. 6. The simulation and experimental data of Id_{sat} vs. Id_{off}.

4. CONCLUSIONS

We developed a new systematic calibration procedure which was applied to the calibration of the diffusivity and TED model of the indium impurity. The TED of the indium impurity has been studied using 4 different groups of experimental conditions. Although the indium is susceptible to the TED, the RTA is effective to suppress the TED and maintain a steep retrograde. The accuracy of the proposed technique is validated by SIMS data and 0.13 μm device characteristics such as V_{th} and Id_{sat} with errors less than 5 % between simulation and experiment. With this calibration tool, we can optimize and integrate the process conditions for developing high performance devices scaled down to the 0.1 -μm region by suppressing the RSCE and increasing the driving capability of a device.

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