낮은 Subthreshold 누설전류를 갖는 CMOS 논리회로

論 文
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CMOS Logic Circuits with Lower Subthreshold Leakage Current

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(Song, Sang-Hun)

Abstract - We propose a new method to reduce the subthreshold leakage current. By moving the operating point of OFF state MOSFETs through input-controlled voltage generators, logic circuits with much lower leakage current can be built with few extra components. SPICE simulation results for the new inverter show correct logic results without speed degradation compared to a conventional inverter.

Key Words : CMOS, Subthreshold, Leakage Current, Logic Circuit, Inverter

1. Introduction

The continuing trend of integrating more transistors in a chip faces quite a few challenges [1] in order to keep the current pace with Moore's law [2]. Of the challenges, the power consumption level in a single chip draws a lot of attention as the power consumption drastically increases with the integration. Currently, the easiest and most efficient way of reducing the power consumption of a chip is to scale down the supply voltages. The problem with the scaled-down supply voltage is the speed degradation due to the reduced current driving capability of the transistors [3]. In order to circumvent this problem, threshold voltage reduction should be implemented. However, this will inevitably cause an exponential increase in subthreshold current, which will, in turn, increase the power consumption of a chip. Although this subthreshold leakage current resulting from the OFF state transistors is not large compared to the switching current from the ON state transistors in today's chips, Sakata et. al. [4] estimated the situation would be reversed in future chips. There has been much effort put into low-power circuit techniques in order to reduce the subthreshold current, including Hierarchical power-line scheme [4], Switched-power-supply inverter with level holder [4], Multithreshold-voltage CMOS scheme [5], Switched-source-impedance CMOS scheme [6], and Substrate controlled variable threshold voltage scheme [7]. However, some of them suffer from limited applications and others from design and process complexities. This paper proposes a new method that warrants pin-to-pin compatibility with the conventional logic circuits and can substantially reduce the subthreshold leakage current without speed degradation

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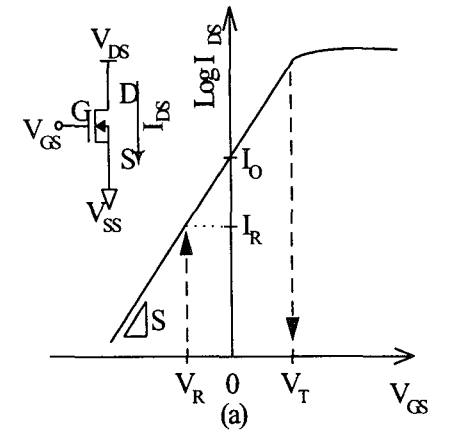
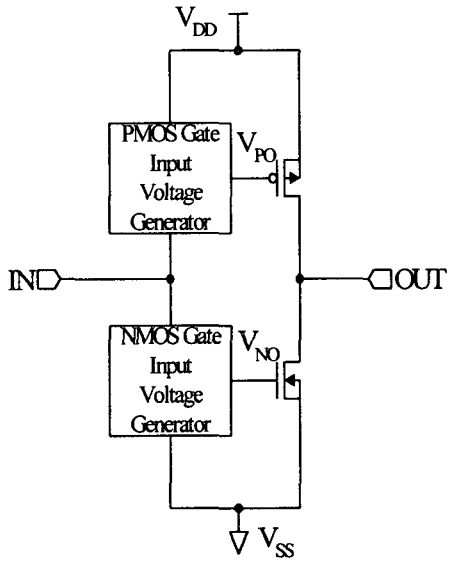
2. Proposed CMOS Logic Circuits

The operating principle of the proposed method is illustrated in Fig. 1. In Fig. 1 (a), the drain-to-source current (IDS) of a typical NMOSFET with respect to the gate-to-source voltage (VGS) for a fixed drain-to-source voltage (VDS) is shown in a log versus linear scale. The notations and bias conditions are depicted in the top-left inset. For conventional CMOS circuits, the OFF state transistors have VGS = 0 with a subthreshold current IO that can be large when the threshold voltage (VT) is reduced, provided that the subthreshold swing, S, does not change. However, the subthreshold current can be exponentially reduced to IR if a reverse voltage (VR < 0 for NMOS or VR > 0 for PMOS) can be applied to the gate-to-source of the OFF state transistors. The simplest logic gate, an inverter, can be constructed employing this idea to reduce the subthreshold current, as is shown in Fig. 1 (b). In addition to conventional inverter, 2 gate input





• Output Characteristics of Voltage Generators

IN	V_{PO}	V_{NO}
Low	$V_{PO} < V_{DD} - \|V_{TP}\|$	$V_{NO} < V_{SS}$
High	$V_{PO} > V_{DD}$	$V_{NO} > \|V_{TN}\| - V_{SS}$

where V_{TP} and V_{TN} are the threshold voltages of PMOS and NMOS, respectively.

(b)

Fig. 1. The operating principle of the proposed inverter.
(a) IDS versus VGS characteristics of a typical NMOSFET. The top-left inset shows the bias conditions. IO is the subthreshold current at VGS = 0 and IR at VGS = VR where the switching transistors will be operated in this paper.
(b) The new inverter circuit proposed. Two voltage generators are inserted to produce the gate inputs for the transistors. Bottom table lists the output characteristics for the generators.

voltage generators are inserted to produce gate input voltages for PMOS and NMOS switching transistors. In order to satisfy the function table of an inverter and, at the same time, to reduce the subthreshold current, the generators should produce the voltages listed in the table at the bottom of the figure, i.e., the reverse gate voltages for the OFF state transistors and the turn-on voltages for the ON state transistors. Notice that this approach, to say the least, is successful as long as the subthreshold currents of the generators are smaller than those of the switching transistors that drive the output.

The question is now shifted to whether we can implement such generators, preferably using a small number of additional components. In Fig. 2, we show an inverter circuit with the generators implemented only with 2 additional transistors and 2 capacitors. The gate input voltage generator for NMOS (PMOS) is composed of an NMOS (PMOS) and a capacitor. Minimum-sized transistors for both NMOS and PMOS can be used to save layout area and the capacitors used need to be adjusted in size through circuit simulation to achieve the desired optimum performance.

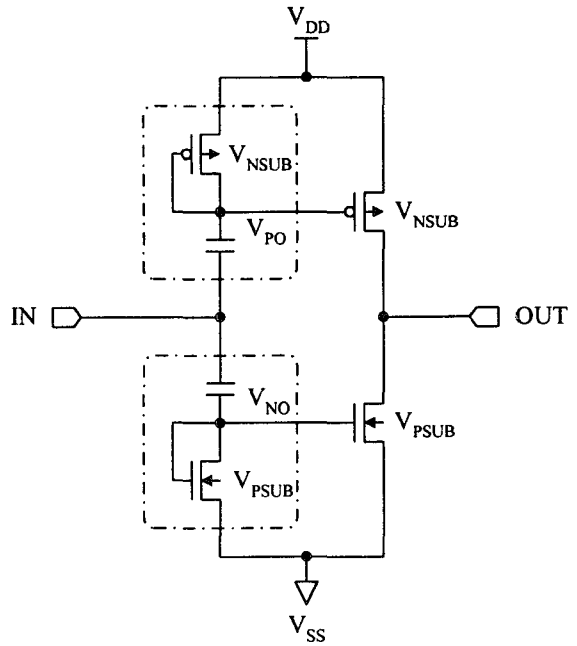


Fig. 2. The new inverter implemented with 2 additional transistors and 2 capacitors. The width of the generator transistors is 0.25um and that of the switching transistors is 4um. All transistors have a channel length of 0.25um. The capa- citors used in the generators have the magnitude of 50fF.

3. Results

The voltage waveforms of the generator outputs and the input/output are shown in Fig. 3. They are obtained from the SPICE simulation with a capacitive load of 60fF using BSIM2 (the 2nd Berkeley Short Channel Igfet Model) MOSFET model.

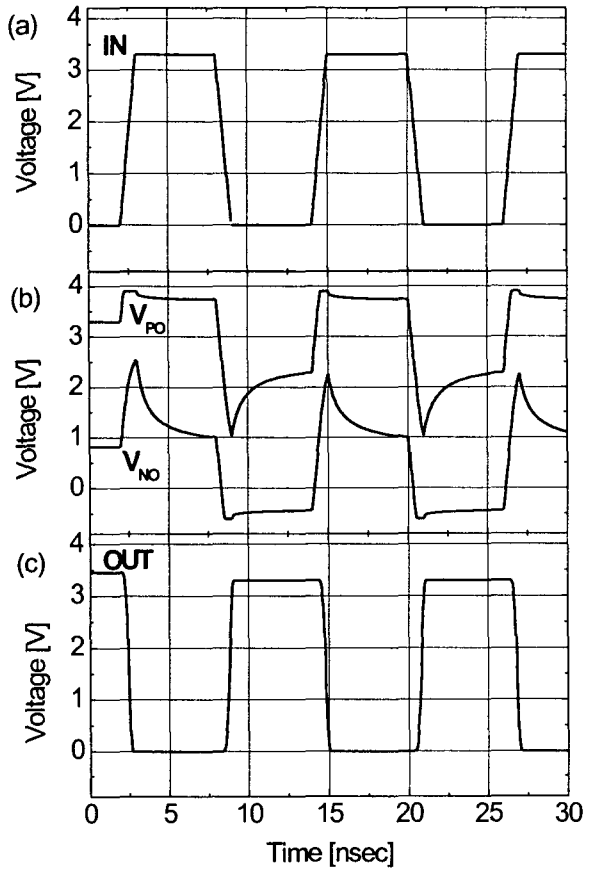


Fig. 3. The SPICE simulated waveforms for the new inverter using BSIM2 model for MOSFETs. (a) Input, (b) Outputs, VPO and VNO, from the gate input voltage generators, and (c) Output

In Fig. 3 (a), (b) and (c), we plot the input waveform, the outputs of the gate voltage generators and the output of the inverter, respectively. The output of the inverter correctly performs the logic operation as can be seen in Fig. 3 (a) and (c). The generator outputs are capacitively coupled to the input so that the coupling is inactive until the input makes the first transition after power up. Therefore, an initialization procedure is required for this inverter to function properly afterwards. Nevertheless, this will not be a big problem because today's systems normally have initialization sequences during which the chips in the systems go into predefined states.

As is shown in the simulated waveforms in Fig. 3 (b), after the input makes the first transition, the voltage generators correctly produce the voltages listed in Fig. 1 (b). As the input makes an upward transition, the VPO node voltage moves up via capacitive coupling to the input. This elevated node voltage will turn on the p+ drain contact to n substrate junction and the current from the VPO node to VNSUB will flow which will lower the VPO voltage until this p+-n junction turns off at about 0.44V. This current is flowing in opposite direction to the switching current and can be recycled during switching if VNSUB is connected to VDD. The generated VPO provides the required bias for the switching PMOS, thus reduce the subthreshold current of the switching transistors substantially. Similar explanations can be applied to the VNO voltage. However, the subthreshold currents of the transistors used in the generators are of concern. For the OFF state transistors after the first transition, the roles of source and drain are exchanged since the voltage at node VPO is higher than VDD and the voltage at VNO lower than VSS, resulting in VGS = 0, in contrast to VGS = VR for the switching transistors. It seems as if what was gained in the switching transistors is lost in the generators. However, as mentioned earlier, the size of transistors in the generators is usually much smaller than that of the switching transistors. Thus, the subthreshold current is reduced by a factor defined by the size ratio of the transistor in the voltage generator to the output driving transistor since the subthreshold current is directly proportional to the size of a transistor, i.e., the gate width of a MOSFET [8]. The leakage can be further reduced by the narrow-channel effect [8] because the subthreshold current exponentially decreases as VT goes up in magnitude for small-sized transistors. Another factor that reduces the leakage is the applied VDS of the OFF state transistors in the generators. Instead of the full VDD, much lower voltages are applied to the drain-to-source nodes as can be seen in Fig. 3 (b). For short channel transistors, it is well known that the subthreshold current is exponentially dependent on VDS [9]. Therefore, the reduced VDS will lead to exponentially reduced leakage current in the generators. All in all, a subthreshold leakage current reduction factor can be roughly estimated as written in Eq. (1).

$$\frac{I_{sub(proposed)}}{I_{sub(conventional)}} \approx \left(\frac{W_{generator}}{W_{switching}}\right)^2 e^{-\alpha(V_{DS(switching)}-V_{DS(generator)})} \quad (1)$$

where Isub's are the subthreshold leakage currents, W's are the widths of the transistors, α is the proportionality constant for DIBL[9], and VDS's are the drain to source

voltages of the transistors.

One thing to notice is that, thanks to the capacitors in the generators, there exists no direct DC current leakage path between the voltage sources, IN, VDD, or VSS. Thus, the leakage will eventually stop when VPO and VNO reach steady-state values. The next issue that deserves mentioning is the switching speed of the proposed inverter compared to that of a conventional one. We observed a 0.1nsec delay in response time compared to the conventional one with switching transistors of equal sizes.

We show the implementations of the other typical logic gates in Fig. 4 (a) NAND gate and (b) NOR gate. While the generator is required for each parallel connection of switching transistors, only a single generator is enough for serially connected transistors.

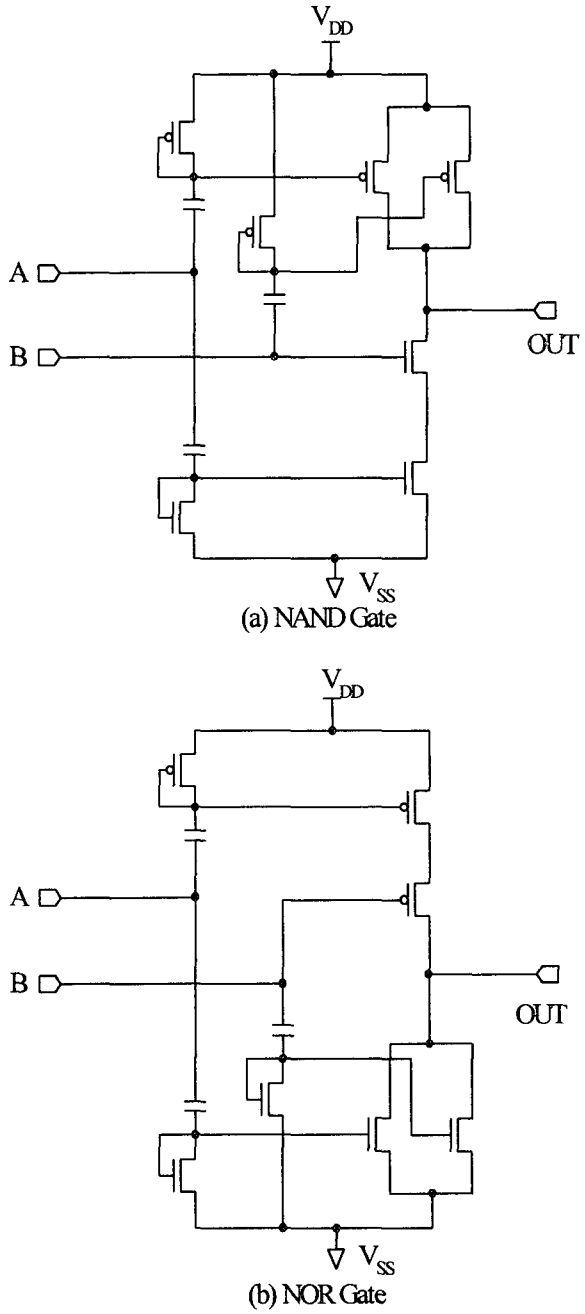


Fig. 4. The implementations of other logic gates, (a) NAND gate and (b) NOR gate

4. Conclusions

In conclusion, we proposed a new circuit technique to reduce the subthreshold leakage current. By placing gate input voltage generators between the input and the gates of the switching transistors, we showed the subthreshold leakage current of logic circuits can be drastically reduced. Furthermore, we implemented the generators only with a small number of additional components. The reduction in subthreshold current mainly comes from 2 factors. One is the transistor sizes used compared to those of the switching transistors and the other is the applied voltage between the drain and source as was explained earlier. In addition, our logic circuits possess pin-to-pin compatibility with the corresponding conventional ones.

Acknowledgement

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