Progress in Superconductivity Vol.6 No.1 pp7-12 31 October 2004

INVITED PAPER

Development of Superconductive Arithmetic and Logic Devices

J. H. Kang*
University of Incheon, Incheon, Korea
Received 18 August 2004

초전도 논리연산자의 개발

강준희*

Abstract

Due to the very fast switching speed of Josephson junctions, superconductive digital circuit has been a very good candidate for future electronic devices. High-speed and Low-power microprocessor can be developed with Josephson junctions. As a part of an effort to develop superconductive microprocessor, we have designed an RSFQ 4-bit ALU (Arithmetic Logic Unit) in a pipelined structure. To make the circuit work faster, we used a forward clocking scheme. This required a careful design of timing between clock and data pulses in ALU. The RSFQ 1-bit block of ALU used in this work consisted of three DC current driven SFQ switches and a half-adder. We successfully tested the half adder cell at clock frequency up to 20 GHz. The switches were commutating output ports of the half adder to produce AND, OR, XOR, or ADD functions. For a high-speed test, we attached switches at the input ports to control the high-speed input data by low-frequency pattern generators. The output in this measurement was an eye-diagram. Using this setup, 1-bit block of ALU was successfully tested up to 40 GHz. An RSFQ 4-bit ALU was fabricated and tested. The circuit worked at 5 GHz. The circuit size of the 4-bit ALU was 3 mm × 1.5 mm, fitting in a 5 mm × 5 mm chip.

Keywords : single, flux, quantum, Josephson, logic, superconductor, digital, microprocessor

I. Introduction

Superconductive digital electronics is a very attractive technology because of its high operating speed and ultra-low power dissipation. In the early 1990s, Nb technology had advanced enough to build LSI circuits. Several Japanese laboratories attempted to develop a superconductive computer by using this technology [1-2]. These efforts led to a few successful demonstrations, including an 8-bit microprocessor [3]. However, these circuits employed voltage-state (latching) logic that does not fully utilize the high switching speed of the Josephson junctions. The operating speed of these circuits was less than 2 GHz.

Due to recent advancements in telecommunication technologies, higher processing speeds and larger amount of the transmission data are required. Semiconductor technology has been slowly developing to meet these requirements. Ultimately, the appearance of quantum computers and DNA computers, which are anticipated to be available by

*Corresponding author. Fax : +82 32 766 8018
e-mail : jhkang@incheon.ac.kr

the middle of the 21th century, can be a solution of the requirements [4]. In the mean time, a rapid single flux quantum (RSFQ) device has been suggested to overcome the limitations of semiconductor devices. Successful developments of various RSFQ logic circuits [5], including a digital-to-analog converter [6], an analog-to-digital converter [7], a switching device [8], a router, and a voltage standard [9], have been reported. In RSFQ logic circuits, a magnetic-flux quantum stored in an inductor and controlled by a Josephson junction is used to build a fast digital logic circuit [10,11]. The development of new RSFQ logic circuits has been significant in recent years, and a toggle flip-flop (TFF) circuit was built with this technology and was operated at 770 GHz [12].

There have been several approaches to the design of RSFQ ALU, the main component of an RSFQ processor [13-14]. The traditional ALU architecture employs a variety of logic cells, resulting in higher complexity of design. Therefore, we tried a non-standard approach to simplify the design, thus adapting it to the still imperfect superconductor fabrication process.

In this work, we have designed a simple 1-bit ALU and 4-bit ALU as a first step toward developing a parallel pipeline 8-bit ALU. In contrast to the conventional design employing numerous logic cells, we used only a Half Adder (HA) cell [15] and three switches and a merger to construct a high-speed 1-bit ALU block. Testing was conducted on a computerized test setup, and an analog test setup showed the correct operations of the ALU and its components.

II. Circuit design

The conventional approach to designing ALU leads to quite cumbersome circuitry in the case of RSFQ logic. We used a Half-Adder (HA) cell as a basic element of the ALU because the required speed of the ALU implies the parallel pipeline architecture, and the fast HA cell is very suitable for this purpose.

Fig. 1 shows a simplified schematic block diagram of the 1-bit ALU block (a) and the simplest two-bit ALU constructed of these blocks (b).

The half-adder naturally performs XOR and AND

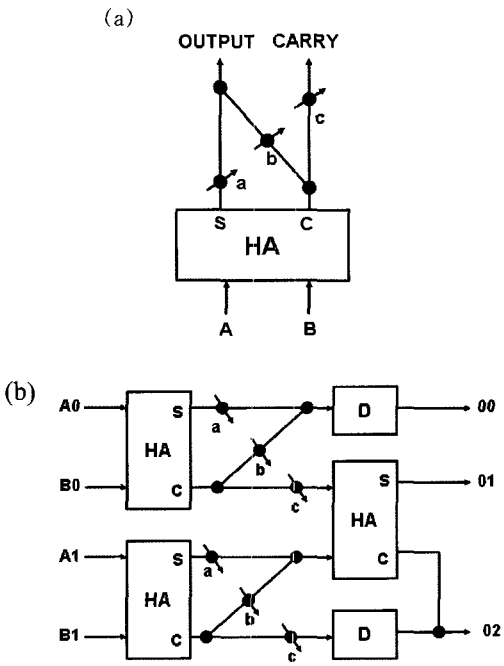

Fig. 1. (a) A simplified block diagram of a 1-bit ALU block based on a half adder cell. Four logic functions of OR, AND, ADD, and XOR are selected by the three switches a, b, and c. (b) The simplest two-bit ALU constructed of these blocks.

Table 1. Switch selections for each logic function.

	OR	AND	ADD	XOR
a	1	0	1	1
b	1	1	0	0
c	0	0	1	0

operations, and such operations as OR and addition could be done by the commutation of the two half-adder outputs. We could select the proper outputs of the half-adder cell with three switches. Table 1 shows the logic table for the instruction decoder. If both switches "a" and "b" are "ON," the ALU operates as an OR. If only switch "b" is "ON," the ALU operates as an AND. If both switch "a" and switch "c" are "ON," the ALU operates as an adder. If only switch "a" is "ON," the ALU operates as an XOR.

Noting that the race is the key, we designed an SFQ switch based on the race conditions of two Josephson junctions. Fig. 2 shows how the designed SFQ circuit operates. The operation of the circuit is based on the race conditions between the two junctions J_{on} and J_{off} illustrated with pendula, where the race is initiated by the arrival of a data pulse. If there is not enough bias current to J_{on} the initial Josephson phase of J_{on} is smaller than the Josephson phase of J_{off}. In that case, J_{off} wins the race when a data pulse enters, and the data pulse escapes, as shown in Fig. 2(a). However, if there is enough bias current to J_{on}, the initial Josephson phase of J_{on} is larger than the Josephson phase of J_{off}. In that case, J_{on} wins the race when a data pulse enters, and the data pulse transmits. This is shown in Fig. 2(b). By supplying an appropriate control signal to I_{sw}, we can control the SFQ switch. To make the junction J_{off} more favorable to switching when $I_{sw} = 0$, we made the I_c of J_{off} smaller than the I_c of J_{on}. We optimized the circuit parameters by using WRspice™ and Julia, circuit simulation programs developed for Josephson circuits.

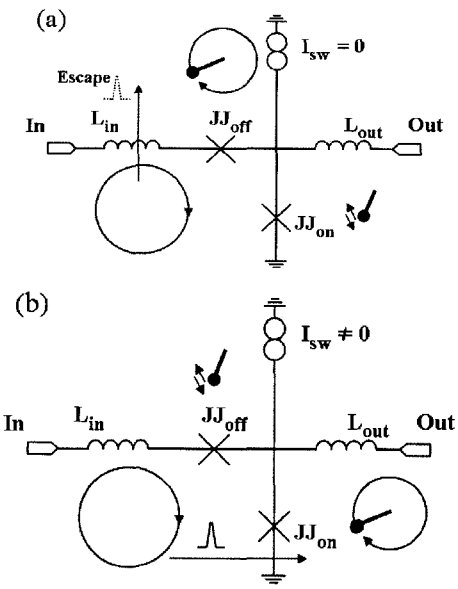

Fig. 2. Circuit schematics and the operational principle of the designed SFQ switch. (a) When there is no bias current to J_{on}, J_{off} wins the race and the data pulse escapes. (b) When there is enough bias current to J_{on}, J_{on} wins the race and the data pulse transmits.

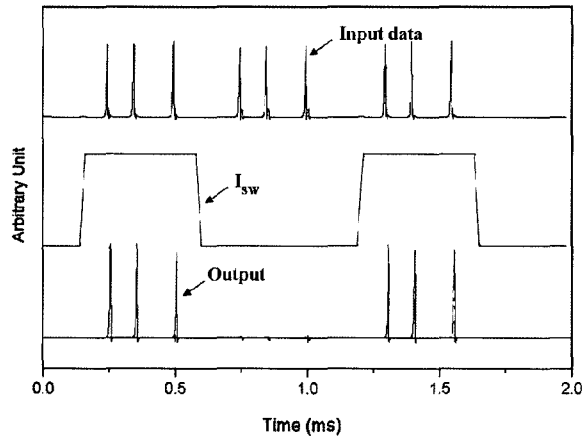

Fig. 3. Circuit simulation results for the designed SFQ switch. (1101) data patterns were used in the simulations.

To estimate the circuit performance of the designed SFQ switch, we simulated the circuit by using WRspice™. Fig. 3 shows the simulation results. To effectively simulate the circuit, we used a DC/SFQ circuit to generate SFQ pulses and a Josephson transmission line (JTL) to transfer them to the SFQ switch. Output pulses from the SFQ switch were terminated through a JTL, and the output voltage pulses were monitored. In the real world, monitoring these output SFQ pulses is very difficult, so an SFQ/DC circuit is normally used. In simulations, however, we could monitor the transient electrical behaviors of every circuit elements. We normally monitored the voltages, the currents, and the Josephson phases. As shown in Fig. 3, the circuit performed as designed. To perform the circuit simulations, we generated two sets of signal patterns, the input data and the switch control. In Fig. 3, we can see that the input data were transmitted through the switch when the switch control signal was on and that the data were blocked from transmission when the switch control signal was off. In the simulations, we repeated the (1101) signal patterns in the input data.

Prior to designing ALU, we drew the circuit schematics of the 1-bit block of ALU with Xic. We simulated the circuit using WRspice™, and the results are shown in Fig. 4. As can be seen in the figure, the correct operation of the circuit was observed. Margins for all parameters were more than ± 25%.

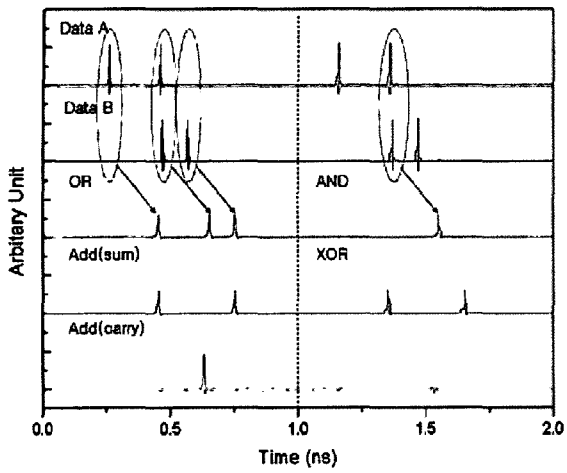

Fig. 4. SPICE simulation results of the 1-bit ALU. Due to the propagation delay, there was about 180 psec delay between the inputs and the outputs. Correct operation of the circuit was observed with all the margins of more than ± 25%.

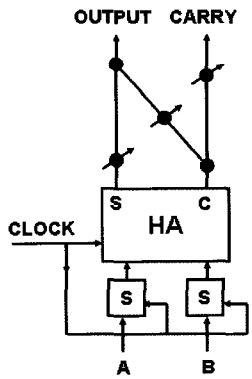

Fig. 5. The simplified block diagram of the fabricated 1-bit ALU. For high speed tests, clock pulses were fed into the two inputs where the high-speed data pulses were gated with DC switches.

Fig. 5 shows the simplified block diagram of the fabricated 1-bit block of ALU, inserted into the high-speed test environment. In this on-chip test frame, high-speed clock pulses are gated with switches producing two data input streams. Timing is a bottleneck of RSFQ circuit design. To avoid racing between clock and data pulses, we employed a counter-flow timing scheme. This technique allowed us to observe the circuit's operation at high speed on a low bandwidth oscilloscope.

1-bit ALU block can be connected to produce a multi-bit ALU with the method shown in Fig. 1(b). In this work, we have designed 4-bit ALU and obtained the mask layout. The most important point in the layout was in the timing of the clock pulses distributed throughout the 4-bit ALU circuit. By using the forward clocking scheme, we could optimize the operation speed of the circuit.

III. Circuit tests

The SFQ switch circuit was fabricated by using the ten-level Nb process with a junction critical current density of 1 kA/cm^2 [16]. The fabricated chip was immersed into a liquid He dewar to test the circuit at 4.2 K. A specially designed cryo-probe was used to transmit the data between the cooled chip and the room temperature instruments.

We used a computerized test setup to test the RSFQ digital circuits more effectively. Finding optimum DC bias current values was essential to operating the RSFQ circuits. By using the computerized test setup, we could find the optimum bias current values with minimum effort.

For the high-speed test, we employed data-from-clock technique. All inputs of the circuit under test were continuous streams of clock pulses controlled by the switches. All output signals were monitored with TFF type SFQ-to-DC converters. Each output SFQ pulse causes the SFQ-to-DC monitor to toggle its DC voltage state. At high frequency, this toggling gets averaged on a low-speed oscilloscope into a single line. If there is no output signal, the output monitor is in a random voltage state giving us a double line ("0"/"1") on the oscilloscope. Applying some low-speed pattern to the input switches, we observed a sort of "eye-diagram" on the outputs.

Fig. 6 shows the high-speed eye diagram test results of the 1-bit block of ALU. The clock frequency used in the test was 20 GHz, and the data inputs were gated at 100 kHz. By using the switches as an instruction decoder, we were selecting the ALU operation of ADD, OR, AND, and XOR. Fig. 6 shows four figures that show OR, AND, XOR and ADD operations, respectively.

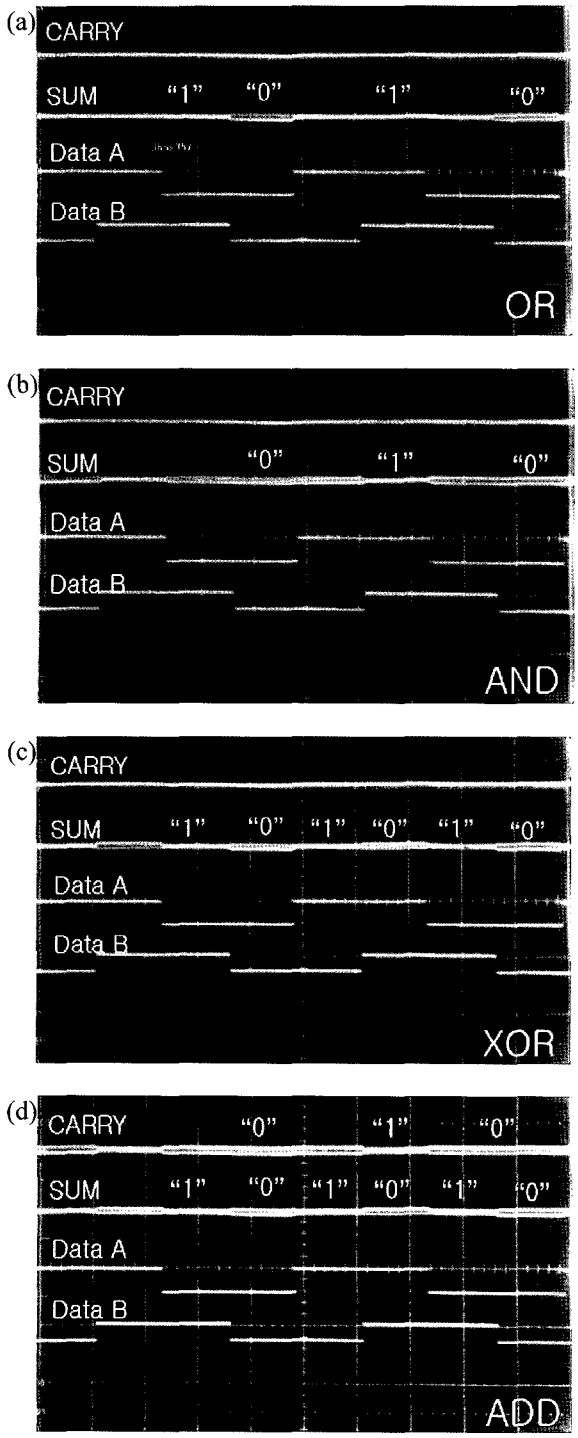

Fig. 6. Test results of the 1-bit ALU at 20GHz. By controlling the three DC switches, we could obtain ALU operations of (a) OR, (b) AND, (c) ADD, and (d) XOR.

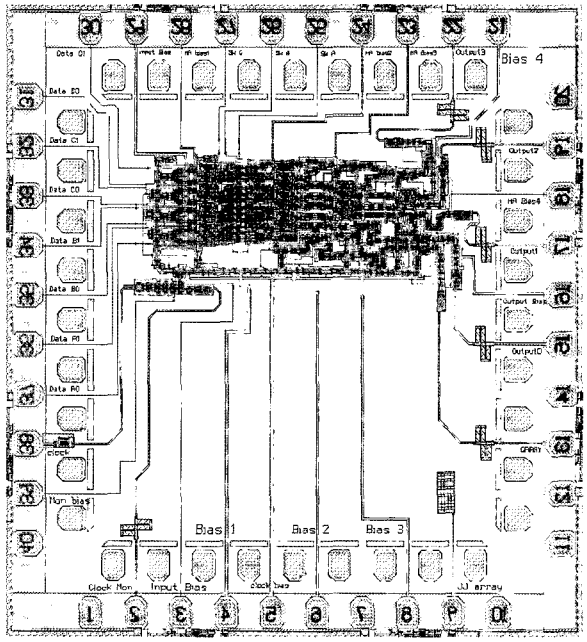

Fig. 7. Chip layout of 4-bit ALU. The circuit size of the 4-bit ALU was 3 mm x 1.5 mm, fitting in a 5 mm x 5 mm chip.

Fig. 7 shows the chip layout of the 4-bit ALU. The fabricated circuit operated correctly at low speeds and high speeds. We tested the circuit at 5 GHz with an eye diagram technique. The circuit operated correctly for all four operations of ADD, OR, AND, and XOR at 5 GHz.

IV. Conclusion

In this work, we have designed, fabricated, and successfully tested an RSFQ 4-bit ALU, along with a 1-bit ALU block. The 1-bit block of ALU consists of a half adder and three switches. The instruction set of the ALU includes AND, OR, XOR, and addition. The low-speed (functionality) test showed correct operation of the ALU within wide margins of the DC bias currents. The high-speed test showed that the half adder operated correctly at 20 GHz with an operational margin of +/- 9%. DC switches used for instruction decoding operated with plenty of bias margins. The 1-bit ALU block was tested at the high speed up to 20 GHz and the 4-bit ALU was tested at the high speed up to 5 GHz. Correct operations for

each of the four functions were obtained for both circuits.

Acknowledgments

This research was supported by a grant from the Center for Applied Superconductivity Technology of the 21st Century Frontier R&D Program funded by the Ministry of Science and Technology, Republic of Korea. The work at the University of Incheon was partly supported by the Korea Science and Engineering Foundation through the Multimedia Research Center at the University of Incheon.

References

[1] Takada S, Nakagawa H, Kurosawa I, Aoyagi M, Kosawa S, Okada Y, and Hamazaki Y "A 4-bit Josephson computer ETL-JC1," IEEE Trans. on Magnetics 27 2610-2617 (1991).

[2] Yano S, Hatano Y, Mori H, Yamada H, Nakahara K, Hirano M, and Kawabe U, "A 1-GHz-clock Josephson microcomputer system," IEEE Trans. on Magnetics 27 2618-2625 (1991).

[3] Hasuo S, Kotani S, Inoue A, and Fujimaki N, "High-speed Josephson processor technology," IEEE Trans. on Magnetics 27 2602-2609 (1991).

[4] D. K. Brock, Int. J. High-Speed Elec. and Sys., "RSFQ Technology: Circuits and Systems," **11**, 307 (2001).

[5] Q. P. Herr, N. Vukovic, C. A. Mancini, K. Gaj, Q. Ke, V. Adler, E. G. Friedman, A. Krasniewski, M. F. Bocko, and M. J. Feldman, "Design and low speed testing of a four-bit RSFQ multiplier-accumulator," IEEE Trans. Appl. Supercond. 7, 3168 (1997).

[6] R. D. Sandell, B. J. Dalrymple, and A. D. Smith, "An SFQ digital to analog converter," IEEE Trans. Appl. Supercond. 7, 2468 (1997).

[7] V. K. Semenov, "Digital to analog conversion based on processing of the SFQ pulses," IEEE Trans. Appl. Supercond. 3, 2637 (1993).

[8] N. B. Dubash, P. F. Yuh and V. V. Borzenets, "SFQ data communication switch," IEEE Trans. Appl. Supercond. **7**, 2681 (1997).

[9] C. J. Burroughs, S. P. Benz, T. E. Harvey, and C. A. Hamilton, "1 volt DC programmable Josephson voltage standard," IEEE Trans. Appl. Supercond. **9**, 4145 (1999).

[10] C. A. Hamilton and Frances L. Lloyd, "100 GHz binary conter based on DC SQUID," IEEE Electron Dev. Lett. EDL-3, 335 (1982).

[11] K. Likharev and V. Semenov, "RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," IEEE Trans. Appl. Supercond. 1, 3 (1991).

[12] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid single flux quantum T-flip flop operating up to 770 GHz," IEEE Trans. Appl. Supercond. 9, 3212 (1999).

[13] Bunyk P, Dorojevets M, and Zinoviev D "FLUX chip: design of a 20-GHz 16-bit ultrapipelined RSFQ processor prototype based on 1.75-μm LTS technology," IEEE Trans. on Appl. Supercond. 11 326-332 (2001).

[14] Takahashi K, Miyahara K, Takai H, Nagasawa S, Hasegawa H, and Enomoto Y "Design of a superconducting ALU with a 3-input XOR gate," IEEE Trans. on Appl. Supercond. 13 551-554 (2003).

[15] Semenov V K, and Polyakov Y A "Superconducting delta ADC with on-chip decimation filter," IEEE Trans. on Appl. Supercond. 9 3026-3029 (1999).

[16] HYPRES design rules can be found at Hypres web site at www.hypres.com.