An LTCC Linear Delay Filter Design with Interdigital Stripline Structure

Hee-Yong Hwang*, Seok-Jin Kim and Hyeong-Seok Kim†**

Abstract - In this paper, new design equations based on the pole-zero analysis for multi-layered interdigital stripline linear group delay bandpass filter with tap input ports are presented. As a design example, a four-pole group delay filter with center frequency of 2.14GHz, bandwidth of 160MHz, and group delay variation of ±0.1nS for LTCC technology or multilayered PCB technology is designed. In the design process, it is not necessary to simulate the entire structure, as the simulation of half structures is sufficient. Good results can be attained after the optimizing process was performed three times using the proposed equations and a commercial EM simulator.

Keywords: BPF, linear group delay filter, multilayer, planar filter, pole-zero analysis.

1. Introduction

Linear group delay filters are widely used to cancel distorted signal of feed forward power amplifiers or substitute some long heavy delay lines, or as a symbol delay element of digital-communication systems, and various theoretical studies to obtain desired delay response according to ripple levels have been performed [1-4]. However, for the complexity to control both the amplitude and the phase characteristics simultaneously, the studies for realizations of the physical linear delay filter are less active compared to Equal-ripple, Maximally-flat, and Elliptic filters, in which only amplitude characteristics are considered. In order to design a practical linear phase filter, moreover, we have to consider coupling structures for input and middle parts, and the frequency dependent characteristic of the coupling structures.

LTCC has many advantages over other technologies to realize interdigital stripline linear phase filters with small planar structure, good power capability, high temperature stability, and other physical stabilities. The tap coupling structure is simple and beneficial for input and output coupling on the LTCC process, though it involves some complexity in dealing with exact electrical properties. To design physical interdigital stripline linear delay filters, design equations and an optimizing method are mandatory, unless there exists a full-wave numerical simulator specialized to the given structure, which requires a lengthy time period and great effort to establish.

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Considering the above situations, we derive a design equation set based on pole-zero analysis of the filter. This allows the straightforward design and optimization of the dimensions and parameters of the linear delay filter using the equations.

2. Design Equations

Fig. 1 shows the equivalent network of the generalized interdigital linear phase filter with two n+1 degree cross-coupled interdigital lines. The element values, which are normalized to the load admittance Y_l, are given by (1) in Fig. 1 [3] [6]. The admittance inverters are expressed as $Y_{i,j}$ in the figure.

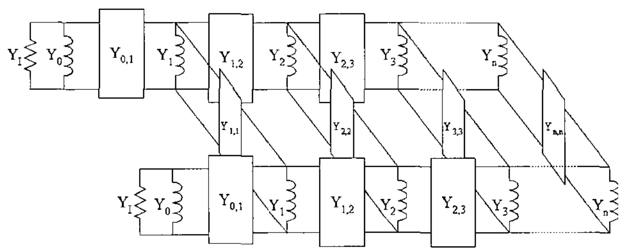

Fig. 1 Equivalent circuit for generalized interdigital linear phase filter.

$$Y_{r-1,r} = \frac{1}{\alpha\sqrt{C_{r-1}C_r}}$$

$$Y_{r,r} = \frac{K_r}{\alpha C_r}$$

$$Y_r = 1 - Y_{r-1,r} - Y_{r,r+1} - Y_{r,r} \quad \text{for r= 1→n, with}$$

$$C_0=\frac{1}{\alpha},\quad C_{n+1}=\infty \text{ , and } Y_0=1-\frac{1}{\alpha\sqrt{C_1}} \tag{1}$$

where $\alpha=\omega'\mathrm{cosec}\left(\frac{\pi(f_2-f_1)}{2(f_2+f_1)}\right)$, ω' is the cutoff frequency of the low pass prototype, and K_r and C_r are low pass prototype element values available in [7].

The input and output parts are modified to inverter input Y'_{01} of (2) by use of the corresponding equivalent circuits supplied in Fig. 2 (a), (b). Hence, the equivalent circuit of the given interdigital linear phase filter is represented as in Fig. 3 in which all elements are a quarter wavelength at the filter center frequency f_0.

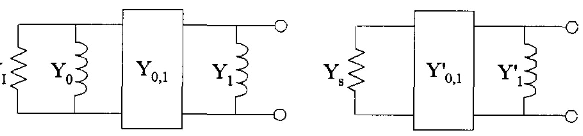

Fig. 2 The input or output part (a) and its equivalent circuit (b) for input or output part

$$Y'_{01}=Y_{01}\sqrt{\frac{Y_s}{Y_I}} \text{ and } Y'_1=1-Y_{01}^2+Y_1-Y_0 \tag{2}$$

where the phase difference of 90 degrees is ignored.

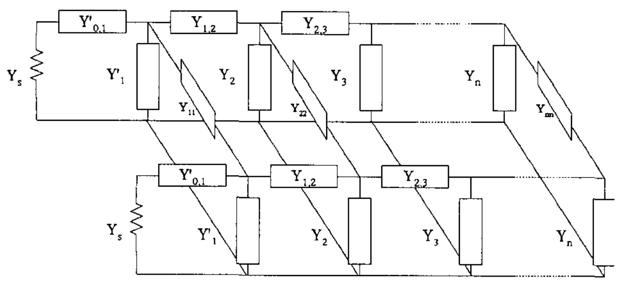

Fig. 3 Equivalent circuit for linear phase filter with quarter wavelength transmission lines.

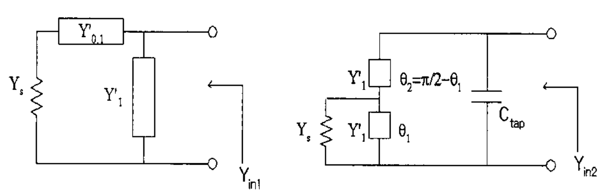

Fig. 4 Inverter input (a) and Tapped input (b)

For changing inverter input circuit to tapped input circuit, we compare the two input circuits shown in Fig. 4. Appendix A1 is used to consider the frequency dependent characteristics of the transmission line inverter Y'_{01}, while deriving susceptance B_1 and its slope parameter b_1.

$$Y_{in1}=\frac{Y'^2_{01}}{Y_s}+jB_1$$

$$Y_{in2}=\frac{Y_sB}{D}+jB_2 \tag{3}$$

where $B_1=\left(Y'_{01}\frac{Y_s^2-Y'^2_{01}}{Y_s^2}-Y'_1\right)\cot\theta$,

$B_2=\left[\omega C_{tap}+\frac{ED-BC}{D}\right]$, $B=Y_s^2+Y_1^2\left(\tan\frac{\theta_2}{2}-\cot\theta_1\right)^2$,

$C=\frac{B}{Y'_1}\sin\theta_2-Y'_1\left(\tan\frac{\theta_2}{2}-\cot\theta_1\right)$, $D=Y_s^2+C^2$, and

$E=Y'_1\tan\frac{\theta_2}{2}$.

In order to obtain the tapped input parameters θ_1, Y'_1 and C_{tap}, we equated the real parts and slope parameters b_1, b_2 of Y_{in1}, Y_{in2} with each other at the center frequency f_0.

$$b_1=\frac{\pi}{4}Y'_{01}\left[\frac{Y_s^2-Y'^2_{01}}{Y_s^2}\left(\frac{K}{\beta}\right)^2+1\right]$$

$$b_2=\frac{\omega_0}{2}\frac{\Delta B_2}{\Delta\omega}\Big|_{near\ \omega_0} \tag{4}$$

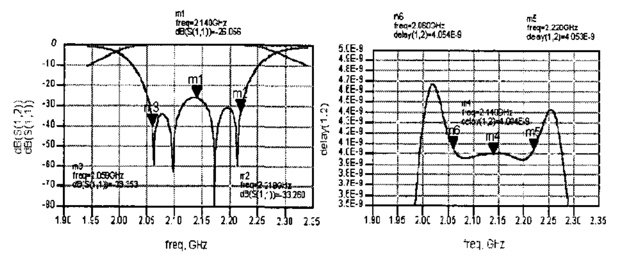

Fig. 5 Filter response by equivalent circuit with tapped inputs (using ADS™).

A systematic way to iterate a filter using an EM-simulator is to put all poles and zeros of the filter at the same positions so that the pole-zeros of the reference filter are located on the frequency axis.

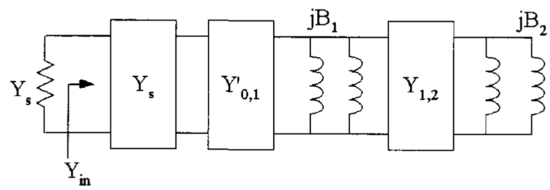

Fig. 6 Even or odd mode equivalent circuit for Fig. 3.

The equivalent circuit of Fig. 3 can be used as a reference filter while all the physical dimensions of the filter are being determined. Using the symmetry, we can divide it into two identical sections to calculate all parameters, namely even and odd modes as shown in Fig. 6. The example of the reference filter characteristics is shown in Fig. 7, and the pole-zeros in S_{11} from even and odd modes are shown in Fig. 8.

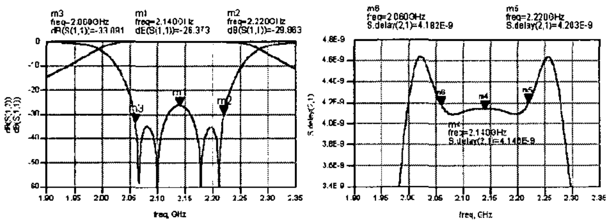

Fig. 7 Filter response by equivalent circuit (using ADS™).

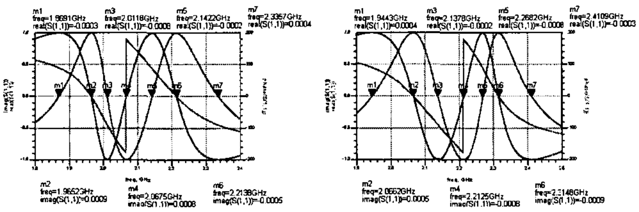

Fig. 8 Typical pole-zeros for s11 of even (left) and odd (right) mode circuit

The 7 pole-zeros appear around the center frequency for the 4-pole filter as demonstrated in Fig. 8. The relation of each pole and zero between the real and imaginary parts of S_{11} is summarized as below:

a) $Im(S_{11})=0$ and $Re(S_{11})= -1$ at f_4, or,

$B_2 = 0$ at f_4

b) $Im(S_{11})=0$ and $Re(S_{11})= 1$ at f_2, f_6, or

$B_1 - \frac{Y_{12}^2}{B_2} = 0$ at f_2, f_6

c) $Im(S_{11})=1$ and $Re(S_{11})= 0$ at f_1, f_5, or

$B_1 - \frac{Y_{12}^2}{B_2} = -\frac{Y'^2_{01}}{Y_s}$ at f_1, f_5

d) $Im(S_{11})=-1$ and $Re(S_{11})= 0$ at f_3, f_7, or

$B_1 - \frac{Y_{12}^2}{B_2} = \frac{Y'^2_{01}}{Y_s}$ at f_3, f_7

where,

$$B_1 = Y_{11} - Y'_1 \cot\theta_1,$$
$$B_2 = Y_{22} - Y_2 \cot\theta_2 \quad \text{for even mode} \tag{5}$$

and,

$$B_1 = -Y_{11} - Y'_1 \cot\theta_1$$
$$B_2 = -Y_{22} - Y_2 \cot\theta_2 \quad \text{for odd mode.} \tag{6}$$

The input admittance Y_{in} and S_{11} in Fig. 6 are given as (7) and (8).

$$Y_{in} = j\left(\frac{Y_s}{Y'_{01}}\right)^2 \frac{B_1 B_2 - Y_{12}^2}{B_2} = jB \tag{7}$$

$$S_{11} = \frac{Y_s - Y_{in}}{Y_s + Y_{in}} = \frac{Y_s^2 - B^2}{Y_s^2 + B^2} - j\frac{2Y_s B}{Y_s^2 + B^2} \tag{8}$$

From a)-d), the resonator frequency (or electrical length) and coupling coefficients are calculated as follows.

$$\ell_2 = \frac{1}{f_{4e} + f_{4o}} \frac{1}{2\sqrt{\mu\varepsilon}} \tag{9}$$

$$\frac{\cot\theta_{21e}\cot\theta_{61e} - \cot\theta_{31e}\cot\theta_{71e}}{(\cot\theta_{21e} + \cot\theta_{61e}) - (\cot\theta_{31e} + \cot\theta_{71e})} = \cot\theta_{42e} \tag{10}$$

$$k_{22} = \frac{4}{\pi}\cot\theta_{42e} \tag{11}$$

$$k_{12} = \frac{4}{\pi}\sqrt{(\cot\theta_{42e} - \cot\theta_{21e})(\cot\theta_{61e} - \cot\theta_{42e})} \tag{12}$$

$$k_{11} = \frac{4}{\pi}\left[\cot\theta_{21e} + \left(\frac{\pi}{4}k_{12}\right)^2 \frac{1}{\cot\theta_{42e} - \cot\theta_{21e}}\right] \tag{13}$$

$$k_{01} = \frac{2}{\sqrt{\pi}}\sqrt{\frac{\pi}{4}k_{11} - \cot\theta_{31e} - \left(\frac{\pi}{4}k_{12}\right)^2 \frac{1}{\cot\theta_{42e} - \cot\theta_{31e}}} \tag{14}$$

where, θ_{ije} and θ_{ije} are the electrical lengths of the j-th resonator at i-th frequency for even mode and odd mode circuits, respectively.

The definitions of coupling coefficients for the circuit in Fig. 3 are simply given as (15)-(18).

$$k_{01} = \frac{J_{01}}{\sqrt{b_1 Y_s}} = 2\sqrt{\frac{Y'^2_{01}}{\pi Y'_1 Y_s}} \tag{15}$$

$$k_{12} = \frac{J_{12}}{\sqrt{b_1 b_2}} = \frac{4}{\pi}\frac{Y_{12}}{\sqrt{Y'_1 Y_2}} \tag{16}$$

$$k_{11} = \frac{J_{11}}{b_1} = \frac{4}{\pi}\frac{Y_{11}}{Y'_1} \tag{17}$$

$$k_{22} = \frac{J_{22}}{b_2} = \frac{4}{\pi}\frac{Y_{22}}{Y_2} \tag{18}$$

A cross sectional of the physical structure and dimensions of the filter are represented in Fig. 9. The general stripline parameters and fringe capacitances for coupled striplines are available in [8, 9].

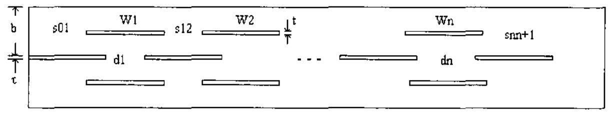

Fig. 9 A cross section of physical structure

In the top view of the filter, Fig. 10, L is λ/4. The input line for tapped input is 50ohm line.

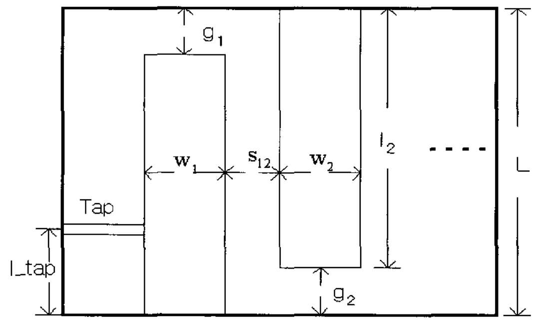

Fig. 10 Top view of the filter.

All resonators must be tuned at the filter's center frequency, so we take (19).

$$\omega_0 (C_{g1} - C_{tap}) = Y_{o1} \cot \frac{\pi l_1}{2\lambda}$$

$$\omega_0 C_{gk} = Y_{ok} \cot \frac{\pi l_k}{2\lambda} \qquad (19)$$

where C_{gk} and Y_{ok} are the k-th gap fringing capacitance and characteristic impedance of the resonator. Each C_{gk} can be calculated by (29) and the more accurate equations available in [10].

$$C_{gk} = \omega_0 \varepsilon w_k (2c_{fo}(g_k)/\varepsilon), \; g_k = L - l_k \qquad (20)$$

Table 1 Spec. of the linear phase filter

N=2n=4, fo=2.140GHz, BW=160MHz, ripple=0.01dB.
b=1.270mm, t=0.00mm, tau=0.00mm, er=25.0.
Group delay= 0.1ns variation within the passband.

To test the derived design equations, we take specifications for a linear phase filter as given in Table 1. The filter needs to have a center frequency of 2.14GHz, BW of 160MHz, 0.01dB ripple and 0.1ns variation of group delay within the passband. The relative dielectric constant is 25 and the height of the filter is 2.54mm. First, initial physical dimensions from initial design with the flow chart in Fig. 11 were obtained. This is a well known process [9] that is greatly inaccurate. The initial dimensions are fed to an EM simulator, Momentum™ as even and odd mode structures, whose equivalent circuits are given in Fig. 6. The resulting poles and zeros are fed to the proposed equations, (9)-(20), which is implemented in C++ code. The subsequent process is the optimizing loop using the C++ code and EM simulator pole-zero to help situate the pole and zero at the proper positions. For the characteristic impedance of striplines, Z_l, and for the width of the filter, L, 10Ω and λ/4(7.005mm) are used, respectively. After optimizing three times, a good linear delay filter was revealed as shown in Fig. 12. An improved result was obtained as provided in Fig. 13, which was followed by additional optimizing by EM simulator to reduce the delay variation.

3. Conclusion

Design equations for a multi-layered planar interdigital stripline linear group delay bandpass filter with tap input port were presented. As a design example, a four-pole group delay filter with center frequency of 2.14GHz, bandwidth of 160MHz, and group delay variation of ±0.1nS for LTCC technology was designed. In the design process, it was not necessary to simulate the entire design structure, and a fine result was achieved after optimizing three times with the proposed design equations. This design method could be useful for controlling the error correction in the manufacturing process of the filter as well as in the design stage.

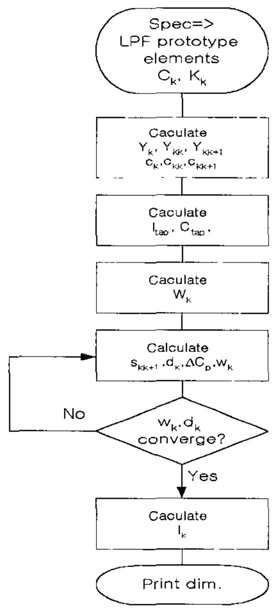

Fig. 11 Design flow chart for initial design

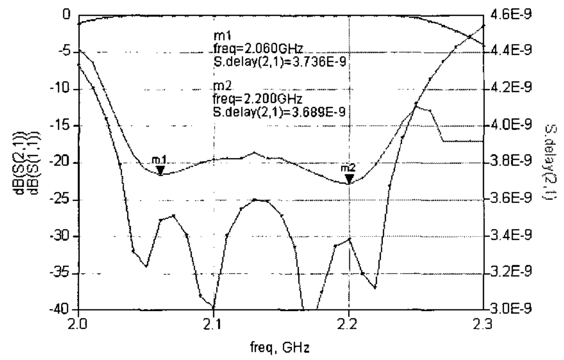

Fig. 12 The EM simulated (by Sonnet™) response of optimized LTCC linear delay in Fig. 10

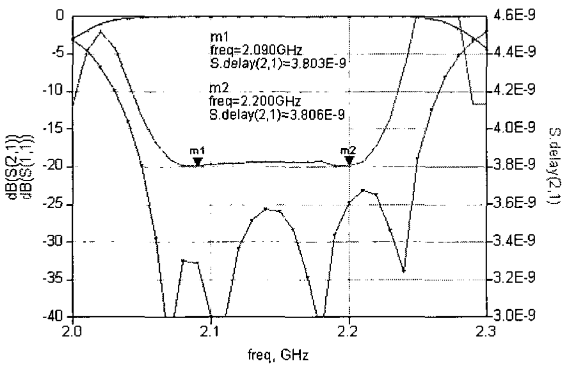

Fig. 13 Further flat group delay response after additional iteration with EM-simulator (Sonnet™)

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References

[1] David Chambers and Yafei Huang, "Synthesis of Delay Filters", IEEE MTT-s International Microwave Symposium Digest, pp1327-1330, 1998.

[2] L. Accatino, A. Angelucci, "A DIELECTRIC RESONATOR FILTER AS LOW LOSS DELAY ELEMENT FOR 14 GHz ON-BOARD 4Φ- DCPSK DEMODULATION", IEEE MTT-s International Microwave Symposium Digest, pp, 1981.

[3] John David Rhodes, "The Generalized Interdigital Linear Phase Filter" IEEE Transaction on Microwave Theory and Techniques, Vol. MTT-18, No.6, June 1970, pp301-307.

[4] A. E. Atia and A. E. Williams, "Nonminimum-Phase optimum-amplitude band waveguide filters", IEEE Transaction on Microwave Theory and Techniques, Vol. MTT-22, pp425-431, April 1974.

[5] John David Rhodes, "The Generalized Direct-Coupled Cavity Linear Phase Filter" IEEE Transaction on Microwave Theory and Techniques, Vol. MTT-18, No.6, June 1970, pp308-313.

[6] John David Rhodes, "A Low-pass Prototype Network for Microwave Linear Phase Filters" IEEE Transaction on Microwave Theory and Techniques, Vol. MTT-18, No.6, June 1970, pp290-301.

[7] J.H. Cloete, "Tables for Nonminimum-Phase Even-Degree Low-Pass Prototype Networks for the Design of Microwave Linear-Phase Filters" IEEE Transaction on Microwave Theory and Techniques, Vol. MTT-27, No.2, Feb. 1979, pp123-128.

[8] Shimizu, J.K. and E.M.T.Jones, "Coupled-Transmition-Line Directional Couplers", IRE Trans. MTT, Vol. MTT-6, pp.403-410, Oct. 1958

[9] J.A.G.Malherbe, Microwave Transmition Line Filters, Artech house, Inc. 1979.

[10] D. D. Khandelwal, "The Resonant Frequency of Interdigital Filter Elements", IEEE Transaction on Microwave Theory and Techniques, May 1967, pp322-324.

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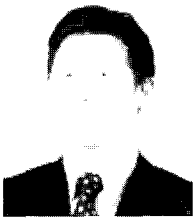

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