

A 5-GHz Band CCNF VCO Having Phase Noise of -87 dBc/Hz at 10 kHz Offset

Ja-Yol Lee¹ · Sang-Heung Lee¹ · Jin-Young Kang¹ · Bo-Woo Kim¹ · Seung-Hyeub Oh²

Abstract

In this paper, we present a new current-current negative feedback(CCNF) differential voltage-controlled oscillator (VCO) with $1/f$ induced low-frequency noise suppressed. By means of the CCNF, the $1/f$ induced low-frequency noise is removed from the proposed CCNF VCO. Also, high-frequency noise is stopped from being down-converted into phase noise by means of the increased output impedance through the CCNF and the feedback capacitor C_f . The proposed CCNF VCO represents 11-dB reduction in phase noise at 10 kHz offset, compared with the conventional differential VCO. The phase noise of the proposed CCNF VCO is measured as -87 dBc/Hz at 10 kHz offset frequency from 5.5-GHz carrier. The proposed CCNF VCO consumes 14.0 mA at 2.0 V supply voltage, and shows single-ended output power of -12 dBm.

Key words : VCO, Phase Noise, $1/f$ Noise, CCNF, SiGe.

I. Introduction

Recently, as high-quality local signal is necessary at mobile wireless phone such as CDMA and GSM, a lot of low phase noise VCO circuit design techniques have been developed to diminish the phase noise of VCO^{[1]~[4]}.

In VCO having LC-tank resonator, different noise sources are generated from both active devices and resonator, and then closely converted around the carrier frequency by the nonlinear operation of the switching active devices. The dc-blocking capacitors of the cross-coupling path are used to obtain balanced signal and to diminish the low-frequency noise due to all even harmonics. However, the capacitors increase low-frequency voltage due to the high output impedance at the output node, causing worse phase noise. Accordingly, the output impedance was reduced by low-frequency feedback^[1].

In reference [2], a cascode current source with capacitor filter was utilized to suppress the low-frequency noise in $1/f^3$ region. The common-mode node is not nearly changed because its output impedance is very high.

In order to suppress the low-frequency noise down-converted from thermal noise around all even harmonics, the LC low-pass filter is connected from the

collector node of the tail current transistor to ground^[3].

Additionally, the degeneration inductor is connected from the source of the tail current transistor to ground in order to diminish the tail current noise^[4].

In oscillator using FET device, it is reported that the low-frequency feedback method has suppressed the induced input noise voltage from the flicker noise of FET device, reducing the interaction between FET and flicker noise generator^[5]. Therefore, we can reduce the phase noise of VCO at low-offset frequency through the low-frequency feedback network that consists of resistor and transistor^{[6]~[8]}.

Rohde first presented the low-frequency feedback oscillator circuit and showed significant phase noise improvement^{[6],[11]}. But the oscillator circuit includes resistor and inductor in the feedback path. The resistor causes thermal noise, which degrades phase noise in oscillator. The inductor is voluminous to integrate in silicon RFIC oscillator. Also, Rohde's oscillator is susceptible to common-mode noise such as power supply noise because of its single-ended type. Therefore, Rohde's oscillator needs to be improved for silicon RFIC oscillator.

In this paper, we present not only an improved differential current-current negative feedback oscillator that has suitable structure for RFIC oscillator, but also

Manuscript received June 12, 2004 ; revised August 17, 2004. (ID No. 20040612-021J)

¹SiGe Device Team, ETRI, Daejeon, Korea.

²Dept. of Electronics Engineering, Chungnam National University, Daejeon, Korea.

describe the CCNF oscillator in detail. Through this paper, we suppress the low-frequency noise using the CCNF oscillator whose output impedance is increased by loop gain. The CCNF has an important role to sample the low-frequency noise and cancel the noise source at the base input port of Q_1 . We achieved 11-dB improvement in the phase noise of the proposed VCO using CCNF. The phase noise of the proposed CCNF VCO is measured as -87 dBc/Hz at 10 kHz offset frequency from 5.5-GHz carrier. The CCNF VCO consumes 14.0 mA at 2.0 V, and represents single-ended output power of -12 dBm.

II. Design of CCNF VCO

2-1 Intuitive Description about CCNF VCO

In this section, the qualitative description is given about the low-frequency noise suppression technique in the CCNF oscillator of Fig. 1. Since positive feedback is generated by the base-emitter capacitance of Q_1 and C_f at high frequency, the CCNF oscillator is Colpitts-type oscillator. The CCNF oscillator of the left-side circuit in Fig. 1 is composed of emitter follower Q_1 , low-frequency feedback resistor R_f , high-frequency feedback capacitor C_f , and feedback amplifier Q_3 . The same right-sided CCNF oscillator is symmetrically connected through the LC-tank resonator to form balanced oscillator. In the proposed CCNF oscillator, the emitter current of Q_1 is sampled by R_f , and injected into the base resistor of Q_1 at low frequency. So, the proposed VCO is called CCNF VCO. By means of CCNF, therefore, the $1/f$ induced low-frequency noise is sampled by feedback resistor R_f and is feedback to the base of Q_1 through Q_3 . The feedback low-frequency noise cancels the low-frequency noise source induced at the base input of Q_1 such as flicker noise, shot noise and thermal noise^{[6],[7]}. The low-frequency noise from the tail current source is also suppressed by means of R_f and the increased output impedance by the CCNF.

While the feedback capacitor C_f shorts both high-frequency noise around even harmonics and high order harmonics to ground, it generates positive feedback at fundamental frequency. Here, the feedback-boosting transistor Q_3 has an important role not only to boost high-frequency power gain, but also to suppress the whole low-frequency noise of the CCNF VCO through the feedback operation of CCNF.

2-2 Noise Suppression using Current-Current Feedback Network

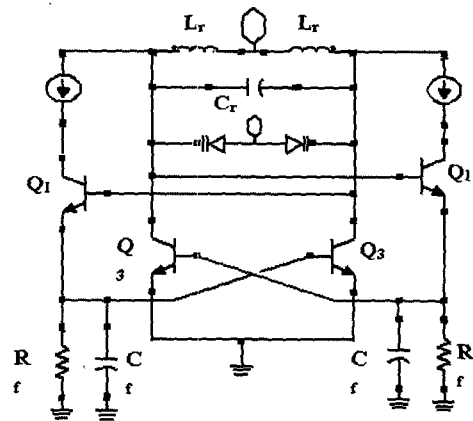


Fig. 1. Proposed CCNF differential VCO circuit diagram.

In the Fig. 2, there shows up the low-frequency equivalent circuit model of the proposed CCNF oscillator. The small-signal equivalent circuit of Q_3 is simply drawn in the dotted line of Fig. 2. Here, r_b represents both base spreading resistance and contact resistance, and r_i is the incremental resistance of forward biased base-emitter diode of Q_3 . As shown in the Fig. 2, the base input noise voltage v_{nb} is induced by flicker noise source v_{nf} . The induced input noise is converted to the carrier by the nonlinear mixing operation of the amplifier Q_1 , and has significant effect on the phase noise of VCO. According to [5], however, the base input noise v_{nb} can be diminished by negative feedback which is locally caused by the emitter resistance R_f of Q_1 . This is approximately expressed by Eqs. (1).

$$v_{nb} = \frac{v_{nf}}{1 + A_{v1}} \quad (1)$$

Additionally, if considering negative feedback by CCNF with Q_3 , the base input noise is more suppressed as given by Eqs. (2).

$$v_{nb} = \frac{v_{nf}}{1 + A_{v1} + \frac{A_{v1} A_{v3} r_i}{r_b + r_i}} \quad (2)$$

where A_{v1} and A_{v3} is the voltage gain of Q_1 and Q_3 , respectively. As given by equations (1) and (2), the base input noise voltage could be more reduced with the increasing voltage gain of Q_1 and Q_3 , respectively. As explained in the previous section, the sampled low-frequency noise v_{ne} injects into the base of Q_3 and is amplified to cancel v_{nf} as shown in Fig. 2.

Also, due to the loading effect of CCNF, the output

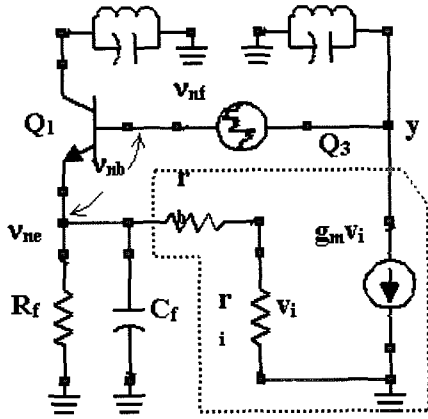


Fig. 2. Low frequency equivalent circuit model.

impedance is enhanced and the input impedance is reduced by loop gain^{[8],[9]}. Since the increased output impedance of CCNF takes a similar role with the inductor on the current source in [3], [4], the tail current noise is stopped from being converted into the phase noise of the carrier.

2-3 One-Port Analysis

In the Fig. 3, the approximate high-frequency small-signal equivalent circuit model is presented. The small-signal equivalent circuit represents only the active part to generate negative resistance except the LC-tank resonator of Fig. 2. Resistors of Fig. 2 are ignored at high frequency. Here, it is assumed that the miller capacitances of Q_1 and Q_3 are considered only at the input port of each transistor, but neglected at the output port because miller effect is usually small at the output port. Now the input impedance of Fig. 3 is derived using test signal V_y . Then it is demonstrated that the input impedance has negative real part at high frequency. If the test signal voltage V_y is applied to node y of Fig. 2 and then the input current I_y is measured, it is capable of calculating the input impedance through from Eqs. (3) to (5).

$$V_y = V_1 + V_3, \quad V_3 = \frac{g_{m1}}{sC_1} V_1 \quad (3)$$

$$I_y = sC_1 V_1 + g_{m3} V_3 = \left(sC_1 + \frac{g_{m1}g_{m3}}{sC_3} \right) V_1 \quad (4)$$

Here, it is assumed that the emitter current of Q_1 is approximately equal to the collector current of Q_1 . That is, the base current of Q_1 is ignored in order to simplify Z_{in} . Substituting Eqs. (4) into Eqs. (3), the input impe-

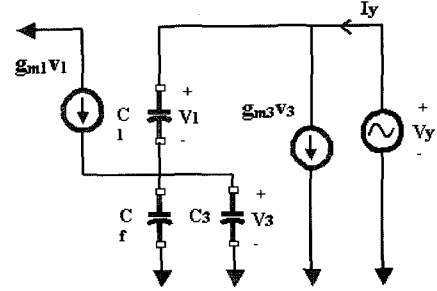


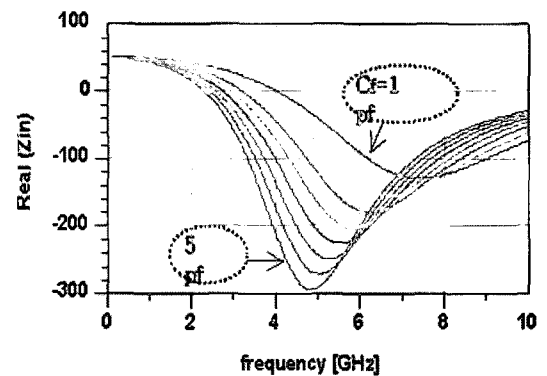
Fig. 3. High frequency equivalent circuit model.

dance Z_{in} is approximately calculated as Eqs. (5).

$$Z_{in} = \frac{V_y}{I_y} = \frac{g_{m1} + j\omega C_t}{g_{m1}g_{m2} - \omega^2 C_1 C_t} \approx -\frac{g_{m1}}{\omega^2 C_1 C_t} - j\frac{1}{\omega C_t} \quad (5)$$

where C_t is the parallel combination of C_f and C_3 . C_1 and C_3 is base-emitter junction capacitance including miller capacitance of Q_1 and Q_3 , respectively. Also, since $g_{m1}g_{m2} \ll \omega^2 C_1 C_t$ at high frequency, the denominator is approximately equal to $\omega^2 C_1 C_t$. Since the feedback resistor C_f is included in the negative real part of Eqs. (5), the magnitude of negative resistance is controlled by the adjustment of C_f .

The simulated input impedance is presented in the Fig. 4. As operating frequency grows up, it shows larger negative resistance. Through the maximum point of the negative real part, the magnitude of the negative resistance starts to be decreased as operating frequency increases. Also, the magnitude of the negative resistance rises up with C_f increasing, which does not consist with the real part of Z_{in} . This simulation results from the approximation of Z_{in} that does not consider resistances and additional capacitances.


 Fig. 4. Simulation result of real part of Z_{in} .

III. Measurements and Discussions

In order to demonstrate the phase noise improvement of the proposed CCNF VCO, we manufactured another conventional 5.5-GHz VCO using 0.8 μm SiGe HBT process technology. The complete schematic diagram of the conventional VCO is given in Fig. 5. In Fig. 6, the chip photographs of the two VCOs are shown, and their sizes are 1.0 mm \times 0.8 mm (a) and 0.7 mm \times 0.7 mm (b), respectively.

Fig. 7 represents the 5.54-GHz signal output power spectrum of the proposed CCNF VCO whose output power is about -12.0 dBm considering cable loss and connector loss. The measured phase noises of the conventional VCO and the proposed CCNF VCO are compared in Fig. 8. The phase noise difference between the conventional VCO and the proposed CCNF VCO is about 11 dB at 300 kHz offset frequency from 5.5-GHz carrier.

Therefore, it is demonstrated that the phase noise of the proposed CCNF VCO is improved by means of the current-current negative feedback network. Since the phase noise of the CCNF VCO is more reduced at low-offset frequency, the proposed CCNF has a significant effect in suppressing low-frequency noise such as flicker noise and shot noise.

For the purpose of comparing the performance of the conventional differential VCO and the proposed CCNF VCO, Figure of Merit (FOM) is calculated as given by Eqs. (6)^[7].

$$FOM = 10 \log f_{osc}^2 - 10 \log (f_m^2 P) - dB[L(f_m)] \quad (6)$$

where f_{osc} is oscillation frequency, f_m is offset fre-

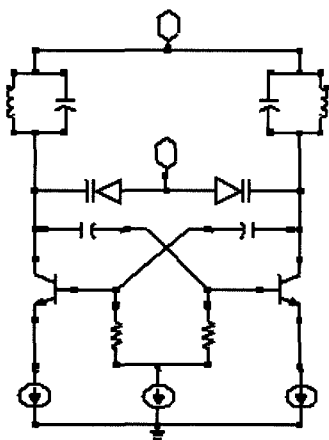
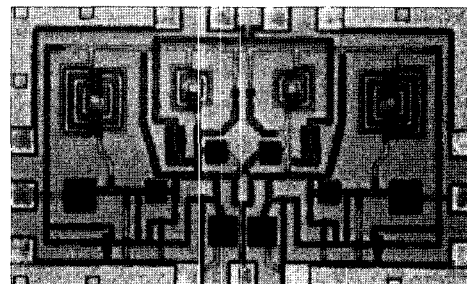
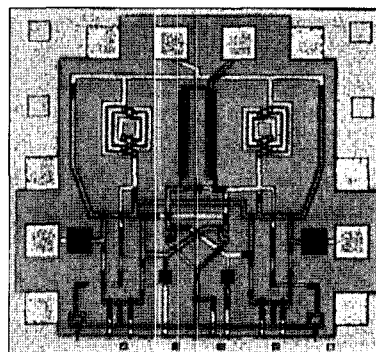


Fig. 5. Conventional differential VCO.



(a) The conventional VCO



(b) The CCNF VCO

Fig. 6. Chip photographs.

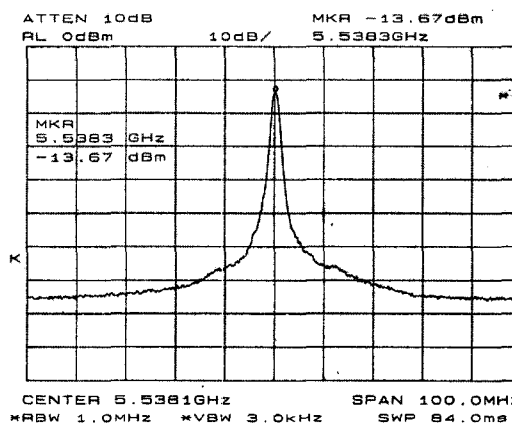


Fig. 7. Measured output power of the CCNF VCO.

quency, P is dissipated power, an $L(f_m)$ is phase noise measured at f_m .

The performance results of the conventional VCO and the CCNF VCO are summarized in Table 1. The FOM of the CCNF VCO is larger by 12 dB than the conventional VCO. Additional, high-order harmonics are more suppressed as -27 dBc through the feedback capacitor C_f .

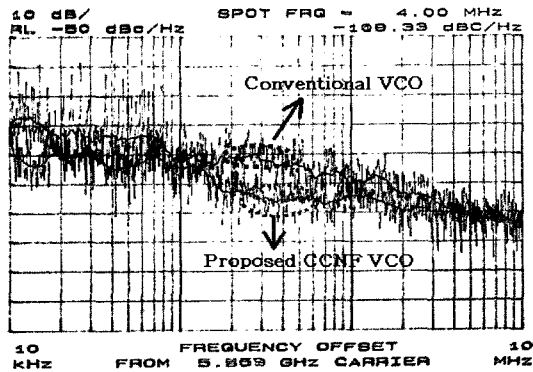


Fig. 8. Measured phase noise of the conventional VCO and the CCNF VCO.

Table 1. Summary of performance parameters about the conventional VCO and the proposed CCNF VCO.

VCO type	Conventional VCO	Proposed colpitts VCO
Parameters		
V_{cc} [V]	2.5	2.0
I_{total} [mA]	13.5	14
P_{out} [dBm]	-10.6	-12
Tuning range [MHz]	5,380~5,520	5,410~5,540
Harmonics [dBc]	< -23	< -27
Phase noise [dBc/Hz]	-77@ 10 kHz	-87@ 10 kHz
Phase noise [dBc/Hz]	-89@ 100 kHz	-98@ 100 kHz
Phase noise [dBc/Hz]	-94@ 300 kHz	-105@ 300 kHz
Phase noise [dBc/Hz]	-102@ 1 MHz	-108@ 1 MHz
Phase noise [dBc/Hz]	-109@ 4 MHz	-110@ 4 MHz
Figure of merit [dB]	174	186

IV. Conclusion

The proposed CCNF VCO is presented for the purpose of improving phase noise in the conventional differential VCO. By the measured results, the phase noise of the proposed CCNF VCO is improved as much as 11-dB at 300 kHz offset from 5.5 GHz carrier compared to the conventional differential VCO. Therefore, we have achieved the effect that the phase noise of VCO is reduced by means of the low-frequency current-current negative feedback (CCNF). Also, the proposed CCNF VCO results in more suppressed harmonics by the feedback capacitor C_f . The conventional VCO and the proposed CCNF VCO was designed and fabricated using 0.8 μm SiGe HBT process tech-

nology.

This work was supported by the Ministry of Information and Communication, Republic of Korea.

References

- [1] M. Borremans, B. De Muer and M. Steyart., "Phase noise up-conversion reduction for integrated CMOS VCOs", *Electronics Letters*, vol. 36, no. 10, pp. 857-858, May 2000.
- [2] Bram De Muer, M. Borremans, M. Steyaert and G. Li Puma, "A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization", *IEEE JSSC*, vol. 35, no. 7, pp. 1034-1038, Jul. 2000.
- [3] Emad Hegazi, et al., "A filtering technique to lower LC oscillator phase noise", *IEEE JSSC*, vol. 36, no. 12, pp. 1921-1930, Dec. 2001.
- [4] Pietro Andreani et al., "Tail current noise suppression in RF CMOS VCOs", *IEEE JSSC*, vol. 37, no. 3, pp. 342-348, Mar. 2002.
- [5] M. Prigent, J. Obregon, "Phase noise reduction in FET oscillators by low-frequency loading and feedback circuitry optimization", *IEEE Trans. MTT*, vol. 35, no. 3, pp. 349-352, Mar. 1987.
- [6] Ulrich L. Rohde, "Requirements for high performance RF/UHF ICs and possible solutions", *IEEE RFIC*, vol. 35, pp. 13-17, 2002.
- [7] Yi Lin, K. H. TO, J. S. Hamel and W. M. Huang, "Fully integrated 5 GHz CMOS VCOs with on chip low frequency feedback circuit for 1/f induced phase noise suppression", *ESSCIRC*, pp. 551-554, 2002.
- [8] Ja-Yol Lee, et al., "An 1.8 voltage-controlled oscillator using current-current negative feedback network", *6th EcWT*, pp. 113-116, Sep. 2003.
- [9] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd edition., McGraw-Hill, Inc.
- [10] J. Rogers, J. Macedo and C. Plett, "The effect of varactor nonlinearity on phase noise of completely integrated VCOs", *IEEE JSSC*, vol. 35, pp. 1360-1365, Sep. 2001.
- [11] Ulrich L. Rohde, "Oscillator basics and low-noise techniques for microwave oscillators and VCOs", *EuMC*, Oct. 1999.

Ja-Yol Lee



received the B.E. degree from Konkuk university, Seoul, Korea, in 1998 and the M.E. degree from Chungnam National University, Daejeon, in 2000, all in electronics engineering. Since 2001, he has been with ETRI, where he has been working as RF & Analog Circuit Designer. His research interests are RFIC and OEIC design, semiconductor device modeling, and SPICE parameter extraction and optimization. He is a member of KICS and KEES.

Sang-Heung Lee



was born in Daejeon, Korea, in 1966. He received the B.E., M.S., and Ph.D. degrees in department of electronics engineering from Chungnam National University, Korea, in 1988, 1992, and 1998, respectively. From 1998 to 1999, he held a position as a post-doctorial researcher at Electronics and Telecommunications Research Institute(ETRI) in Daejeon, Korea. Since 1999, he has been working as a circuit design engineer at Electronics and Telecommunications Research Institute (ETRI). His current interests are RFIC and OEIC design, semiconductor device modeling, and SPICE parameter extraction and optimization.

Jin-Young Kang



received the M.E. and Ph.D. degrees in Physics from Korea Advanced Institute of Science and Technology, in 1979 and 1991, respectively. He joined the Electronics and Telecommunications Research Institute(ETRI) at Daejeon in 1979. He has been working on the development of SiGe Devices and Processes. At present, he is a director of SiGe Device Team at ETRI-Basic Research Laboratory.

Bo-Woo Kim



He received the B.S. and M.S. degrees in physics from Busan National University, in 1975 and 1978, respectively. From 1978 to 1981, he served as a Research Engineer at Samsung Semiconductor Inc., Korea, where he worked on process integration and characterization of MOS devices. Since 1981, he has been with the Electronics and Telecommunications Research Institute (ETRI), Korea. He worked on the development of high-density MOS technology, high-speed bipolar technology, and BiCMOS technology. Also, he has been responsible for developing the unit and modular process to improve small-geometry devices, and played a leading role in the development of advanced process and equipment for VLSI devices. His research interests are thin-film characterization and hot-carrier effect phenomena. From July 1989 to 1987, he researched an evaluation method of electron and hole traps in dielectric film at Tokyo University, Japan, as a foreign researcher. At present, he is a director of High-Speed SoC Research Department at ETRI-Basic Research Laboratory.

Seung-Hyeub Oh



received the B.E., the M.S., and the Ph. D. degrees in Yonsei University, Seoul, Korea, in 1971, 1973 and 1982, respectively, all in electrical engineering. He worked for Tohoku University, Japan, from 1980 to 1981, as a guest researcher and Pennsylvania State University, USA, from 1985 to 1986, as a guest researcher. Since 1984 he has been with Chungnam National University, Daejeon, Korea, where he is a professor in the Department of Electronics Engineering. His research interests include antenna engineering and digital communication RF sub-system design. He is a member of KICS and KEES and IEEE.