

The Phase Transition with Electric Field in Ternary Chalcogenide Thin Films

Sung-Jun Yang, Jae-Min Lee, Kyung Shin, and Hong-Bay Chung^a
Department of Electronic Materials Engineering, Kwangwoon University,
Wolgye 1-dong, Nowon-gu, Seoul 139-701, Korea

^aE-mail : hbchung@daisy.gwu.ac.kr

(Received July 12 2004, Accepted September 1 2004)

Phase transitions from the amorphous to crystalline states, and vice versa, of GST(GeSbTe) and AST(AsSbTe) thin films by applying electrical pulses have been studied. These materials can be used as nonvolatile memory devices. The thickness of ternary chalcogenide thin films is approximately 100 nm. Upper and lower electrodes were made of Al. I-V characteristics after impressing the variable pulses to GST and AST films. T_c (crystallization temperature) of AST system is lower than that of the GST system, so that the current pulse width of crystallization process can be decreased.

Keywords : AsSbTe, GeSbTe, Phase-change, Nonvolatile memory, Chalcogenide

1. INTRODUCTION

A phase-change memory array based on chalcogenide (C-RAM) materials originally was reported by R.G. Neal, D. L. Nelson and G. E. Moore in 1970[1]. Electrical characteristics[2] of amorphous chalcogenide semiconductor thin film, and the on-off switch characteristics[3] have been studied. Improvements in phase-change materials technology subsequently paved the way for the development of rewritable CD and DVD optical memory disks[4]. These advances, coupled with significant technology scaling and better understanding of the fundamental electrical device operation, have motivated the development of chalcogenide based memory technology at the present day technology node[5,6]. C-RAMs nonvolatile devices which used a small volume of chalcogenide alloy material converted between low-resistance poly-crystalline and high resistance amorphous structural phases by resistive heating with programming current pulses[7]. Key advantages of C-RAM nonvolatile technology are: write/read performance, endurance, low programming energy, process simplicity, cost, and CMOS embeddability. The write/read performance is comparable to DRAM[8]. The GeSbTe (GST) system, which is one of the chalcogenide materials, has been studied for phase-change random access memory (P-RAM or C-RAM), because of its fast crystallization and good data storage lifetime characteristics[9]. One of the most important problems is the high current pulse required or the amorphization process. Because the

sample must be heated to its melting point (T_m) in this process(amorphization). T_m of the AsSbTe (AST) system, which is also one of the chalcogenide materials, is lower than that of the GeSbTe (GST) system. However, the crystallization speed of the AST system is slow. In order to get the materials of fast convert to polycrystalline in this study, phase-change of $Ge_2Sb_2Te_5$ and $As_2Sb_2Te_5$ for temperature and electric field is examined in chalcogenide thin films.

2. EXPERIMENTS

$Ge_2Sb_2Te_5$, and $As_2Sb_2Te_5$ bulk were prepared with the same contributed reference[10,11]. The constituent elements weighed in the appropriate ratio were sealed in evacuated quartz ampoules, which were then placed in a furnace and heated at 500, 700, and 1000 °C for 2, 2, and 24 hours, respectively. Then the ampoules were constantly stirred for 1 hour to achieve the complete homo-genization of the constituents in the melt state and quenched successively in air after water dipping. Films of amorphous $Ge_2Sb_2Te_5$, and $As_2Sb_2Te_5$ were prepared by thermal evaporation of the bulk at a deposition rate of about 0.5 nm/s on glass of evaporated Al kept in vacuum at 1×10^{-5} Torr. The composition of the evaporation source is used for the composition of the evaporated films, although there might be slightly differences in the composition between the evaporated films and the starting bulk materials.

The sample structure is shown schematically in Fig. 1. The 100 nm thin film on Al-substrate was fabricated with thermal vacuum evaporator. Al was used as both of lower electrode and upper electrode[12]. T_c was confirmed by measuring the resistance with the varying temperature on the hotplate. I-V characteristics were measured with Hewlett Packard 4155 B semiconductor parameter analyzer. It was experiment that impresses the pulse before 0~1.2 V sweep with step 50 mV. The current pulse has variable duration. The I-V characteristics with sweep were obtained.

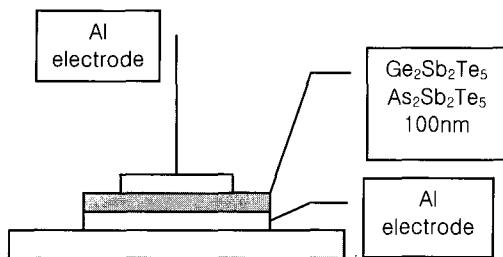


Fig. 1. Schematic illustration of fabricated the sample.

3. RESULTS AND DISCUSSION

When a liquid is cooled, one of two events may occur. Either crystallization may take place at the melting point T_m , or else the liquid will become 'supercooled' for temperatures below T_m , becoming more viscous with decreasing temperature, ultimately to form a glass.

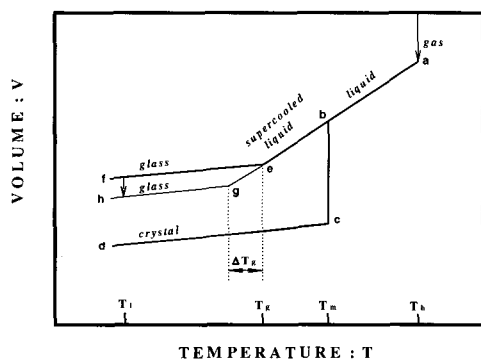


Fig. 2. Schematic illustration of the change in volume with temperature.

The crystallization is processed by an abrupt change in volume at T_m , whereas glass structure was formed by a gradual break in slope. The region over which the change of slope occurs is termed the 'glass-transition temperature' T_g [13].

Once the chalcogenide material is heated over the T_m ,

it is melted into a liquid. Subsequently rapid cooling of the material to below its T_g causes the chalcogenide to be amorphous phase. We have experiment with electric method to convert thermal energy to electric field[14]. It is possible to obtain vitreous/polycrystalline transition resistance ratio which is greater than 100.

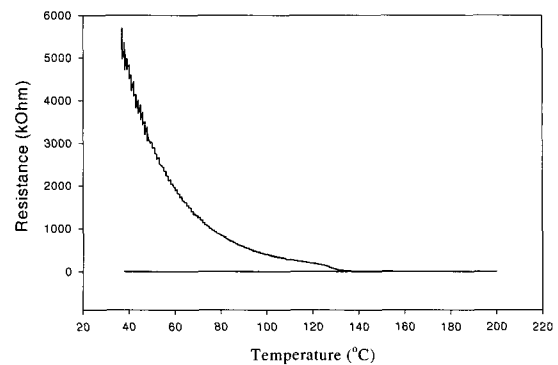


Fig. 3. Resistance change curve with temperature ($Ge_2Sb_2Te_5$).

Figure 3 shows the resistance change with temperature ($Ge_2Sb_2Te_5$), which is changed from room-temperature to 200 °C and gradual cooling to the room-temperature after the sample was kept for 1 hour at 200 °C.

Figure 3 shows considerable transition of resistance after heating. The sample has 5.6 MΩ before heating, and 219 Ω after heating process. Large resistance reduction is owing to crystallization of the sample. Also, Fig. 4 shows the similar result to the Fig. 3. Temperature is changed from room-temperature to 133 °C and gradual cooling to room-temperature. The sample has 12 MΩ before heating, and 2 KΩ after heating process. In results Figs. 3 and 4 shows the phase-change from amorphous state to crystalline state.

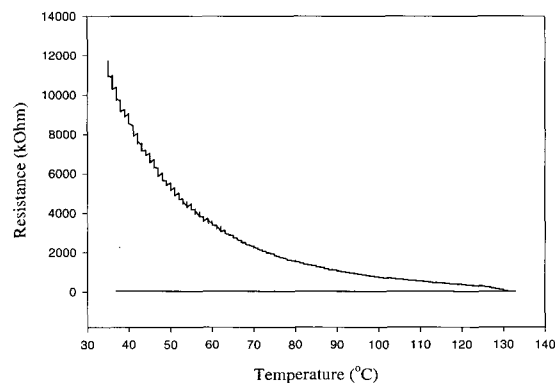


Fig. 4. Resistance change curve with temperature ($Ge_2Sb_2Te_5$).

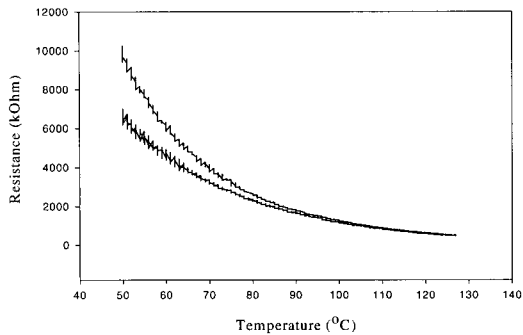


Fig. 5. Resistance change curve with temperature ($\text{Ge}_2\text{Sb}_2\text{Te}_5$).

On the other hand, Fig. 5 shows reversible change of the resistance with temperature, which is changed from room-temperature to 127 °C and gradually cooling to the room-temperature. When temperature was cooled gradually down, resistance increased with temperature. High resistance state (amorphous state) remained after temperature down to room-temperature. Result of reversible change shows that heating temperature of the sample did not approach to T_c (crystallization temperature).

Figure 4 and Fig. 5 show the T_c is placed as approximately from 127 °C to 133 °C.

Figure 6 shows the reversible change of the resistance with temperature ($\text{As}_2\text{Sb}_2\text{Te}_5$), which is changed from room-temperature to 78 °C and gradually cooling to the room-temperature.

Figures 7 and 8 show $\log \sigma$ (conductivity) vs $1/T$ plot of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ and $\text{As}_2\text{Sb}_2\text{Te}_5$ films, where the heating rate was 2.5 K/min. T_c was easily determined as the temperature at which the conductance suddenly increased. GST and AST films have T_c of 404 and 351 K, respectively.

Figures 9 and 10 show I-V characteristics curve 0~1.2 V after impressing pulses which have variable duration and 5 V height.

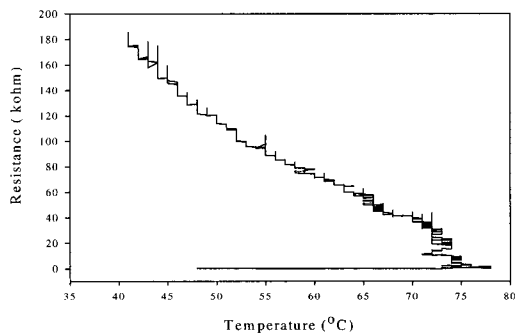


Fig. 6. Resistance change curve with temperature ($\text{As}_2\text{Sb}_2\text{Te}_5$).

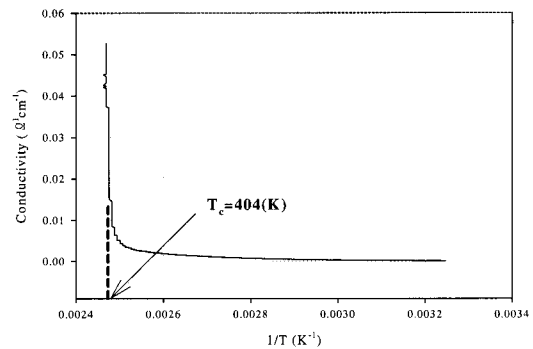


Fig. 7. Temperature dependence of conductivity of the ($\text{Ge}_2\text{Sb}_2\text{Te}_5$).

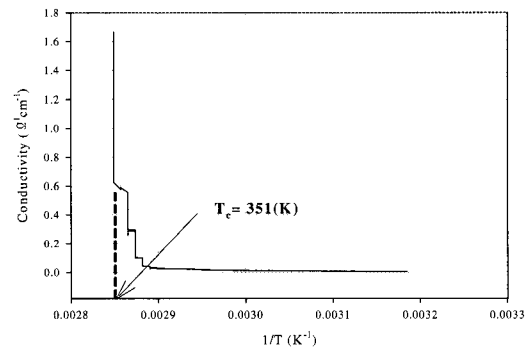


Fig. 8. Temperature dependence of conductivity of the ($\text{As}_2\text{Sb}_2\text{Te}_5$).

When impressed the pulse to resistance change from amorphous to polycrystalline GST and AST are 50 mA, 500 us and 500 uA, 1 ms, respectively. The range of V_{th} (threshold voltage) was typically 0.6 V~1 V (V_{th} GST ; 0.92 V, AST ; 0.68 V)

T_c of AST system is lower than that of the GST system so that the current pulse width of crystallization process can be decreased.

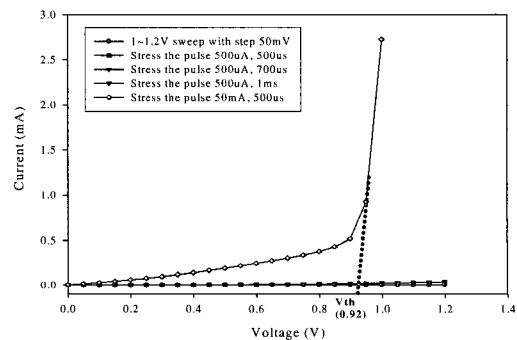


Fig. 9. I-V characteristic curve ($\text{Ge}_2\text{Sb}_2\text{Te}_5$).

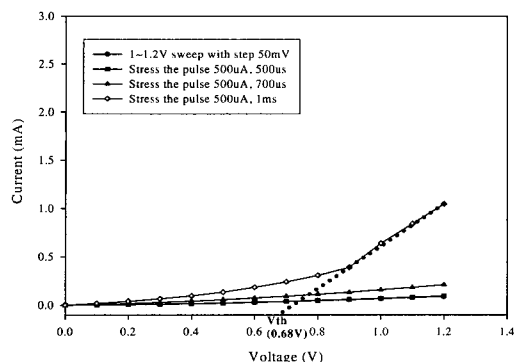


Fig. 10. I-V characteristic curve ($\text{As}_2\text{Sb}_2\text{Te}_5$).

4. CONCLUSIONS

One of the most important problems for C-RAM is that a large current is required for write/erase operation. Particularly, the current for the reset operation is large, because the memory cell must be heated to a temperature higher than T_m in this operation. The use of chalcogenide glass with low T_m is the answer to the above problem.

In this paper, we have investigated the phase change of amorphous chalcogenide thin film with temperature and voltage. T_c is confirmed by using a hotplate for heating the sample, and transition resistance by impressing the current pulse with variable height and duration. V_{th} was typically 0.6 V~1 V (V_{th} GST ; 0.92 V, AST ; 0.68 V)

T_c of AST system is lower than that of the GST system, so that the current pulse width of crystallization process can be decreased.

After this, we should study to find the factor of reversible convert vitreous and crystalline, and find the pulse characteristics for transition resistance.

ACKNOWLEDGMENTS

This work was supported by Korea Research Foundation Grant (KRF-2003-041-D20231).

REFERENCES

- [1] R. Neale, D. Nelson, and Gordon Moore, "Nonvolatile and reprogrammable, the read-mostly memory is here", *Electronics*, p. 56, 1970.
- [2] Hong-Bay Chung and Chang-Yub Park, "Electrical characteristics of the thin film interface of amorphous chalcogenide semiconductor", *J. of KIEE*. Vol. 29, p. 111, 1979.

- [3] Hong-Bay Chung, "Transition characteristics of ON-off state of amorphous chalcogenide semiconductor", *J. of KIT.*, Vol. 9, p. 59, 1980.
- [4] N. Yamada, E. Ohno, K. Nishiuchi, N. Akahira, and M. Takao, "Rapid-phase transitions of $\text{GeTe-Sb}_2\text{Te}_3$ pseudo-binary amorphous thin films for an optical disk memory", *J. App. Phys.*, Vol. 69, No. 5, p. 2849, 1991.
- [5] G. Wicker, "Nonvolatile, high density, high performance phase change memory", *SPIE*, Vol. 3891, p. 2, 1999.
- [6] G. Wicker, "A comprehensive model of submicron chalcogenide switching devices", Ph.D. Dissertation, Wayne State University, Detroit, MI 1996.
- [7] Scott Tyson, Steve Hudgens, Boil Pashmakov, and Wally Czubytyj, "Total dose radiation response and high temperature imprint characteristics of chalcogenide based RAM resistor elements", *IEEE Transactions on nuclear science*, Vol. 47, No. 6, p. 2528, 2000.
- [8] Stefan Lai and Tyler Lowrey, "OUM - A 180 nm Non-volatile Memory Cell Element Technology For Stand Alone and Embedded Applications", Intel Corporation, RN3-01.
- [9] M. Gill, T. Lowrey and J. Park: *IEEE ISSCC 2002 Dig. Tech. Pap.*, p. 202, 2002.
- [10] Jong-Hwa Park, Jung-II Park, Eun-Su Kim, and Hong-Bay Chung, "Holographic grating formation by wet etching of amorphous $\text{As}_{40}\text{Ge}_{10}\text{Se}_{15}\text{S}_{35}$ thin film", *Jpn. J. Appl. Phys.*, Vol. 41, p. 4271, 2002.
- [11] Hong-Bay Chung, Sook Im, and Young-Jong Lee, "The optical properties of Te-Ge-Sb thin films with crystallization", *Proc. 1996 Autumn Conf. KIEEME*, p. 144, 1996.
- [12] Sung-Jun Yang, Kyung Shin, Jung-II Park, Ki-Nam Lee, and Hong-Bay Chung, "The Study of Phase-Change According to Temperature and Voltage in Chalcogenide Thin Film", *Proc. 2003 Summer Conf. KIEEME*, p. 417, 2003.
- [13] S. R. Elliott "Physics of Amorphous Materials", Long-man Scientific & Technical, p. 30, 1990.
- [14] Byeong-Seok Yi, Hyun-Yong Lee, and Hong-Bay Chung, "Electrical and memory switching characteristics of amorphous $\text{As}_{10}\text{Ge}_{15}\text{Te}_{75}$ thin films", *1996 Autumn Conf.*, p. 235, 1996.