A Study on the Electrical Characteristics of Ultra Thin Gate Oxide

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Deep sub-micron device required to get the superior ultra thin gate oxide characteristics. In this research, I will recommend a novel shallow trench isolation structure(STI) for thin gate oxide and a N_2O gate oxide 30 Å by NO ambient process. The local oxidation of silicon(LOCOS) isolation has been replaced by the shallow trench isolation which has less encroachment into the active device area. Also for N_2O gate oxide 30 Å, ultra thin gate oxide 30 Å was formed by using the N_2O gate oxide formation method on STI structure and LOCOS structure. For the metal electrode and junction, $TiSi_2$ process was performed by RTP annealing at 850 ℃ for 29 sec. In the viewpoints of the physical characteristics of MOS capacitor, STI structure was confirmed by SEM. STI structure was expected to minimize the oxide loss at the channel edge. Also, STI structure is considered to decrease the threshold voltage, result in a lower Ti/TiN resistance(Ω /cont.) and higher capacitance-gate voltage(C-V) that made the STI structure more effective. In terms of the TDDB(sec) characteristics, the STI structure showed the stable value of 25 % ~ 90 % more than 55 sec. In brief, analysis of the ultra thin gate oxide 30 Å proved that STI isolation structure and salicidation process presented in this study. I could achieve improved electrical characteristics and reliability for deep submicron devices with 30 Å N_2O gate oxide.

Keywords : N_2O gate oxide, Thin film, $TiSi_2$, Reliability, STI

1. INTRODUCTION

As the deep sub-micron device are recently integrated high package density, novel process method for the 0.1 um devices is required to get the superior thin gate oxide characteristics[1] and reliability. However few have reported on the electrical quality and reliability of the ultra thin gate oxide[2]. In this paper I will recommend a novel shallow trench isolation structure for thin gate oxide and a N_2O gate oxide 30 Å by NO ambient process.

Different from using normal local oxidation of silicon(LOCOS) technology, novel shallow trench isolation(STI)[3] have a unique "inverse narrow channel effects" when the channel width of the devices is scaled down shallow trench isolation has less encroachment into the active device area. Also for STI, the abrupt transient portion from the isolation region to the active one has a significant influence on the electrical characteristics of MOSFET's[4]. In this research, ultra thin gate oxide 30 Å[5,6] was formed by using the N_2O gate oxide formation method on STI structure and LOCOS structure. For the metal electrode and junction, $TiSi_2$ process[7,8] was performed by RTP annealing at 850 ℃ for 29 sec.

In the viewpoints of the physical characteristics of MOS capacitor, STI structure was confirmed the growth of perfect topology by SEM. STI structure achieved in this research is expected to minimize the oxide recess at the channel edge and to contribute to ULSI device integration by giving a big process margin. In the viewpoints of the electrical characteristics of PMOS capacitor for STI structure, the capacitance-gate voltage(C-V) of 0.96, the threshold voltage(V_t[V]) of 0.382 V, the constant current stress test(CCST[sec]) of 25 % ~ 90 % more than 55 sec[9,10].

2. EXPERIMENT

The MOS capacitors were fabricated on p(100) si

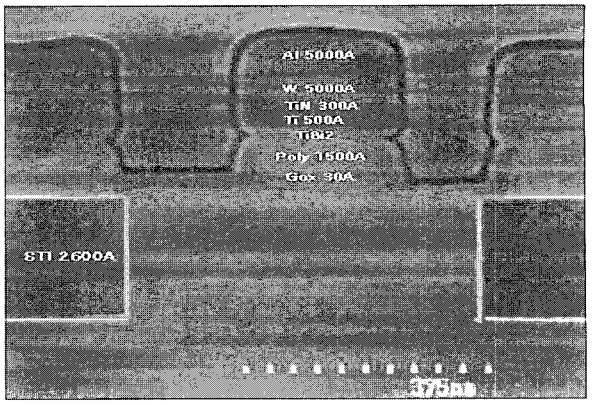
wafers with resistivity of 8~10 Ω.m(prime) using the N_2O gate process. For the isolation technology, the STI structure was fabricated by the following STI process. The STI process sequence starts with the growth of a thermal pad oxide 100 Å followed by the deposition of a HDP-CVD 6000 Å layer. The trenches are achieved by chemical mechanical polishing(CMP) process. The LOCOS structure is fabricated by the following process. The LOCOS process sequence starts with the growth of thermal pad oxide 50 Å followed by the deposition nitride 900 Å. Dry etching for nitride is then done for defining the active area of devices. Gate oxides of 30 Å were formed by using N_2O oxidation at the 900 ℃[11] and 1500 Å polysilicon deposition. A TiSi layer was formed using the conventional self-aligned silicide (SALICIDE) process by rapid thermal annealing(RTA) at 800 ℃ fod 20 sec in N_2 ambient. A metal electrode layer, Ti(500 Å)/TiN(300 Å) were deposited by the conventional sputtering method. TiN/Ti/n^+-Si were annealed at 650 ℃ for 10 sec in N_2 ambient. Lastly, W(5000 Å)/Al(5000 Å) was deposited on the nitrided $TiSi_2$ surface.

As an evaluation of the physical characteristics of the formed device, the phenomena of the STI and the LOCOS field oxide structure due to $TiSi_2$ formation were observed successfully by using a SEM. Gate oxide thickness(T_{ox}) and metal contact resistance were measured. The electrical characteristics analyzed were the capacitance-gate voltage(C-V), the threshold voltage(V_t) of the Si/SiO_2 interface and the time-dependent dielectric-breakdown(TDDB) characteristics under substrate side injection.

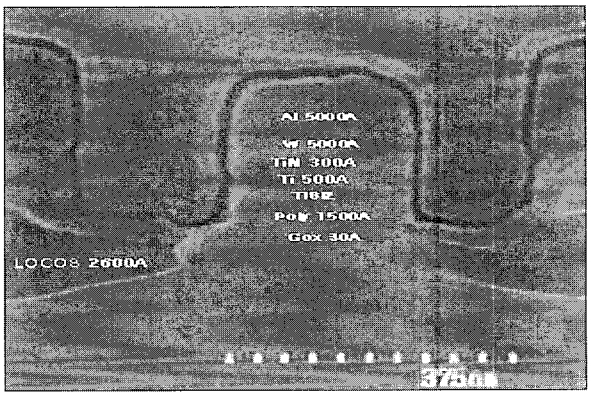
3. RESULTS AND DISCUSSION

Figure 1 displays SEM images for the STI structure formed by using the new method and the LOCOS structure. The figure shows the Al, W, Ti/TiN, $TiSi_2$, polysilicon layers and gate oxide. The cross-section view of the isolation structure confirms the perfect growth of $TiSi_2$ layers, and "kink effect" was not observed near the corner edge of the active area. I think that this phenomenon in the STI structure will enhance not only device integration by taking advantage of the large active area but also the electrical characteristics in terms of channel width.

Figure 2 displays contact resistance of the Ti/TiN layer for the isolation structure. Resistance was 13.2, 13.5, 13.64 Ω/cont. at $TiSi_2$ annealing time 20, 40 and 60 sec on STI. These mean that the STI structure was superior characteristics to LOCOS structure.



(a) STI structure



(b) LOCOS structure

Fig. 1. SEM images of the MOS structure.

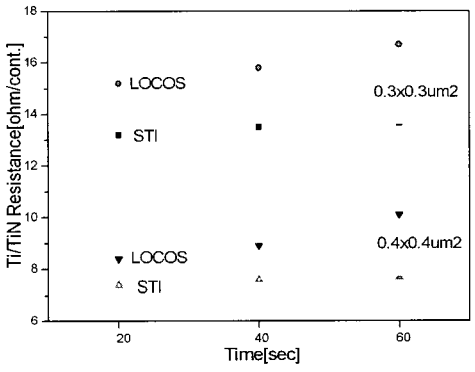
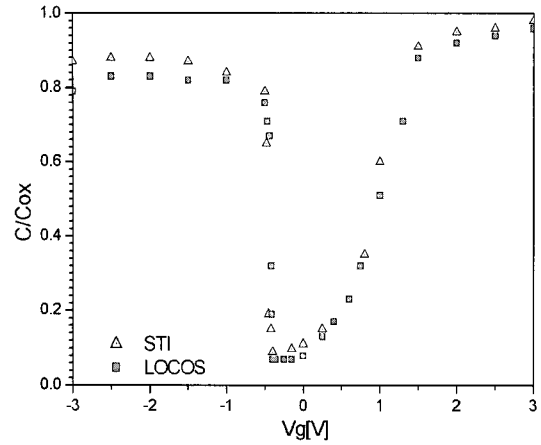
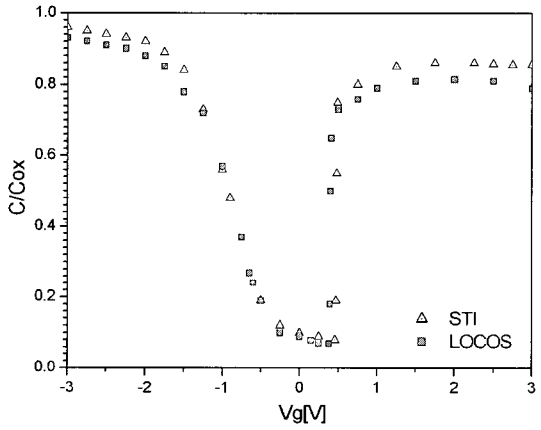


Fig. 2. Contact resistance of the Ti/TiN layer.

Figure 3 displays C-V characteristics of the MOS capacitor. C-V value was 0.87 of STI, 0.79 of LOCOS at reverse gate voltage –3 V on NMOS and 0.96 of STI, 0.93 of LOCOS at reverse gate voltage –3 V on PMOS. In the case of STI C_V value was layer than LOCOS. These means that the major carrier concentration of the STI structure larger than the LOCOS and Ions of the STI structure smaller than the LOCOS at the Si/SiO_2 interface.

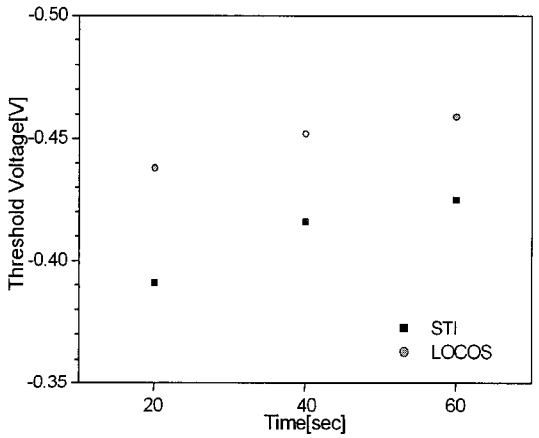


(a) NMOS

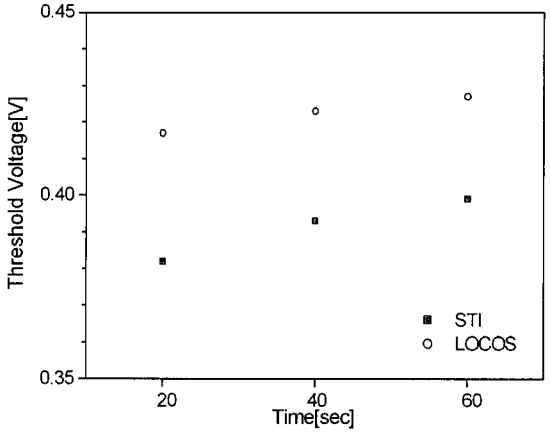


(b) PMOS

Fig. 3. C–V Characteristics of the MOS capacitor.



(a) NMOS



(b) PMOS

Fig. 4. Threshold voltage characteristics of the MOS capacitor.

Figure 4 displays threshold voltage(V_t) characteristics of the MOS capacitor. V_t value was -0.391 V, -0.416 V, -0.42 V of STI, -0.438 V, -0.452 V, -0.459 V of LOCOS at $TiSi_2$ annealing time 20 sec, 40 sec, 60 sec on PMOS. On the whole, STI's was smaller than the LOCOS's. These means that the diffusion coefficient of B^{11} was big and phosphorus(P) concentration was decreased by the phos-phorus retribution on $TiSi_2$ formation.

4. CONCLUSION

Recently, as the sizes of MOSFET devices have been aggressively scaled down into the deep sub-micron region, superior device electrical characteristics and reliability are required for sub-0.1 ㎛ MOSFET devices

Thus, I investigated the electrical quality and reliability of thin gate oxide formed by using a N_2O gate oxide 30 Å with salicide($TiSi_2$) process and STI isolation structure. By using the SEM, I could confirm the successful fabrication of the STI structure which had less encroachment into the active device area and decreased the leakage current as well as trapped charge density at the Si/SiO_2 interface.

In the case of STI structure, oxide loss could be minimized channel edge. Also, STI structure is considered to decrease the threshold voltage, result in a lower Ti/TiN resistance(Ω/cont.) and higher capacitance-gate voltage(C-V) that made the STI structure more effective. In terms of the TDDB(sec) characteristics, the STI structure showed the stable value of 25 % ~ 90 % more than 55 sec.

In brief, analysis of the ultra thin gate oxide 30 Å proved that STI isolation structure and salicidation

process presented in this study. I could achieve improved electrical characteristics and reliability for deep submicron devices with 30 Å N_2O gate oxide.

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