Nature of Surface and Bulk Defects Induced by Epitaxial Growth in Epitaxial Layer Transfer Wafers

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Surface defects and bulk defects on SOI wafers are studied. Two new metrologies have been proposed to characterize surface and bulk defects in epitaxial layer transfer (ELTRAN) wafers. They included the following: i) laser scattering particle counter and coordinated atomic force microscopy (AFM) and Cu-decoration for defect isolation and ii) cross-sectional transmission electron microscope (TEM) foil preparation using focused ion beam (FIB) and TEM investigation for defect morphology observation. The size of defect is 7.29 um by AFM analysis, the density of defect is 0.36 /cm^2 at as-direct surface oxide defect (DSOD), 2.52 /cm^2 at ox-DSOD. A hole was formed locally without either the silicon or the buried oxide layer (Square Defect) in surface defect. Most of surface defects in ELTRAN wafers originate from particle on the porous silicon.

Keywords : ELTRAN, AFM, TEM, FIB, Square defect.

1. INTRODUCTION

Silicon on insulator (SOI) devices are proposed to achieve better device characteristics by having fine-tuned device operation speed, lower power consumption and latch-up immunity reduction [1-3]. SOI wafers have vertical structure made up of buried oxide film grown on a silicon substrate covered with a top layer of silicon. The application of ultra-thin SOI wafers with top silicon thickness of less than 200nm has recently become a standard tool used in the engineering of device architecture for high speed microprocessors. There are several types of SOI wafers that include bonded SOI [4,5], epitaxial layer transfer (ELTRAN)[6,7], and SIMOX[8,9]. The Process flow of ELTRAN fabrication follows. Epitaxial layers on porous Si are transferred by bonding and etching back porous Si, as shown in Fig. 1 [10,11]. The key processes are epitaxial growth on porous Si and selective removal of porous Si. Splitting takes place along around the interface between the 1st and the 2nd porous Si layers at the entire 8-inch bonded pairs with several techniques. The porous Si around the interface is strained due to the difference of the porosity. This localized stress would be responsible for the splitting mechanism. The active layer has no crystalline originated pit (COP) and gives several hundreds microsecond for its minority carrier lifetime. Defects on ELTRAN wafer can be classified as four types: i) Micro void (the interface defect between top Si and buried oxide layer (Box)), ii) Lifted top Si & Hole, iii) Pit (empty top Si layer), iv) Pit (empty top Si & Box). Especially, square defects with missing of top Si and Box is the most important. In this study, a new characterization method will be introduced to observe the morphology and distribution of defects in ELTRAN wafers. We used a light scattering particle counter and coordinated atomic force microscopy (AFM), Cu-decoration with focused ion beam (FIB) and transmission electron microscopy (TEM). In addition, the mechanism by which defects in ELTRAN wafers are produced will be explained with detailed morphology observation. We also investigated the dependency of electric field on Cu-decorated defects for as- and oxidation wafers.

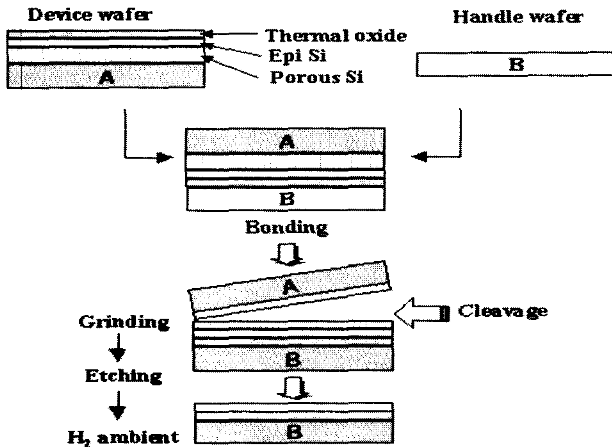

Fig. 1. Process flow of ELTRAN fabrication.

2. EXPERIMENTAL

The samples used in this experiment were p-type, 10Ω-cm, 8 inch diameter ELTRAN wafers. The ELTRAN wafers produced by epitaxial growth on porous silicon at the process of anodization, the annealing, and oxidation. The thickness of top silicon layer and buried oxide layer of these wafers were 180 and 150 nm, respectively. The laser scattering particle counter was used to counter remaining surface defects with a detection sensitivity of greater than 0.20um in size for as-ELTRAN wafers. AFM was coordinated to work with the laser scattering particle counter to observe details of defect morphology. In addition, Cu-decoration was utilized for isolating surface and bulk defects in as-ELTRAN wafers (see, Fig. 2).

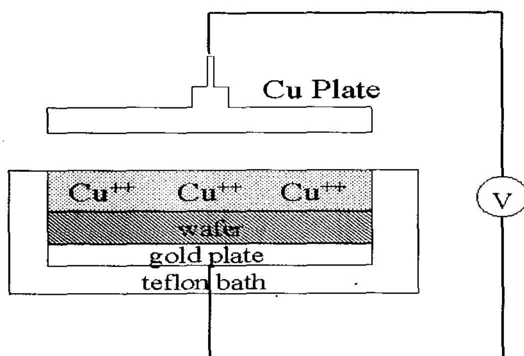

Fig. 2. Schematic drawing of Cu-decorator.

A Cu electrode dipped into a bowl contained methanol was oxidized by the application of a 70V on the cathode, thus creating double charged Cu ions in methanol. Then, as-ELTRAN wafers were dipped into methanol containing Cu ions, which were applied by changing the electric field from 10 to 90V to induce a localized leakage path. Note that the Cu electrode is positively biased while the wafer backside is negatively biased. The defect site produces a negative surface charge as localized leakage occurs, causing a coulomb reaction of Cu^{2+} ions. As a result, Cu^{2+} ions are deposited at the defect site. The defect site deposited with Cu ions is marked by FIB. A wafer containing the defect site is cut with $1\times1cm^2$ area, and then the wafer surface is evaporated by an aluminum layer of a few thousands angstroms to protect the original defect morphology during TEM foil fabrication. A cross-sectional TEM foil at the defect site is fabricated via disc-cutting, grinding, Pt-deposition, and FIB etching. Finally, the cross-section image of the defect site was also observed via TEM. In addition, a thermal oxide film of 100 nm was grown on as-ELTRAN wafers to accelerate a leakage path at the defect site. Finally, the oxidized wafers were examined by Cu decoration method mentioned above.

3. RESULTS AND DISCUSSION

3.1 Morphology of surface defects on ELTRAN wafers via laser scattering particle counter and AFM

It is difficult to recognize the presence of surface defects with a conventional laser particle counter due to a high ratio of signal to noise caused by interference signals from the Box. In our experiment, various polystyrene latex (PSL) on as-ELTRAN wafers were calibrated with a corresponding laser scattering intensity. After calibration, the detection sensitivity of surface defect was greater than 0.20 um in size. Fig. 3(a) exhibits an AFM image of surface defects in ELTRAN wafers. The detailed morphology of the type of surface defects represented in Fig. 3(a) is observed using FIB and TEM.

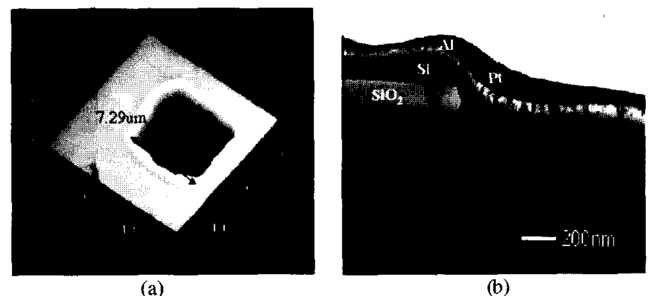

Fig. 3. AFM, TEM images of square defect on the ELTRAN wafer.

The center of the hole shows that the top silicon and buried oxide layer is not exist. Surface defect is square defect. Fig. 3(b) represents TEM image of a square defect like AFM image of Fig. 3(a) in which the size is

0.25 um as measured by the laser scattering particle counter. The true defect size measured by AFM (7.29 um) is approximately 29 times bigger than that measured by the laser scattering particle counter (0.25 um). The true size of the shallow surface defects measured by AFM is much larger than the defect size measured by the laser scattering particle counter as PSL-equivalent. Since the defect size measured via the laser scattering particle counter is determined by the total of the scattered intensity inside the detector, shallow surface pits most likely create a small scattering intensity even though the true defect size is very large. These large discrepancies cause concern as to whether or not the laser scattering particle counter is capable of recognizing surface defects of below sub-um size. This certainly proves that a new metrology to recognize and measure sub-um surface defect is necessary.

3.2 Morphology of surface defects on ELTRAN wafers via Cu-decoration and FIB/TEM

We found the surface defects and bulk defects using the Cu-decoration method. This method conveys positive voltage and negative voltage in the electric power on the surface of wafer and backside. We observed the surface defect of the wafer in detail. Cu ions are deposited on the isolated defect site as soon as the leakage current approaches the critical leakage current (I_{defect}) which is several tens of nano-amperes. From ohm's law

$$I_{defect} = C_1 = \frac{V_{ap}}{R} \tag{1}$$

Where C_1 is the constant that is several tens of nano-amperes, Vap is the applied voltage bias necessary to decorate Cu ions at the isolation defect site, and R is the resistance at the isolation defect site. In addition,

$$R = \rho \frac{l}{A} \tag{2}$$

Where ρ is the resistivity of the wafer, l is the wafer thickness, and A is the area of defect. Assuming that the defect shape is square or circular as shown in Fig. 3, A can be written by $C_2 \bullet R^2_{defect}$. C_2 is the proportional constant for correcting the isolation defect area and R_{defect} is the radius of isolation defect. Equation (1) is rewritten as follows:

$$V_{ap} = \frac{C_1 \cdot \rho \cdot l}{C_2 \cdot R^2_{defect}} \tag{3}$$

Thus, the radius of the isolation defect decreases by increasing the applied bias voltage (Vap). Fig. 4 appears the defect point on the surface of ELTRAN wafer by Cu-decoration method. The edge part of wafer appears the defect on the as- and oxidized ELTRAN wafers.

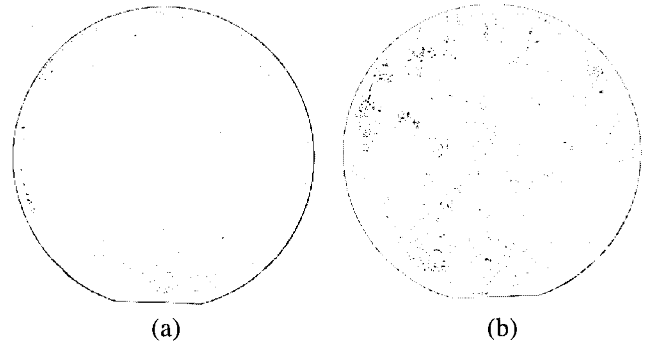

Fig. 4. Distribution of Cu-decorated defects in ELTRAN wafer. (a) Eltran as wafer. (b) Eltran ox wafer.

It is shown that as the electric voltage increases, the defect density also increases in Fig. 5. Especially, in the case of growth of the oxide film on SOI wafer, dsod defects density increases abruptly. When applied voltage is equal to 100V for as-SOI wafer, dsod density is 0.36 / cm^2.

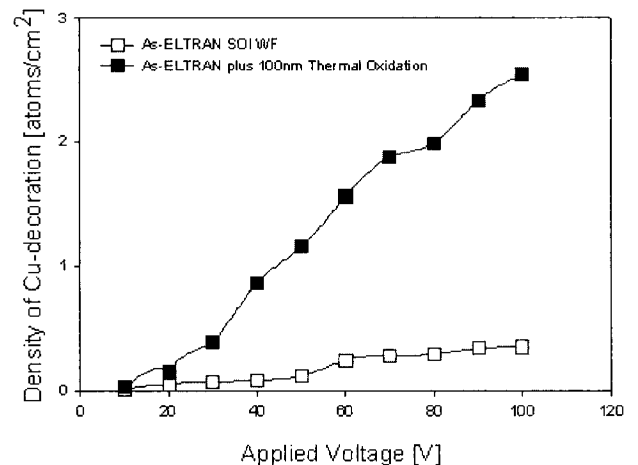

Fig. 5. Effect of applied bias voltage on the density Cu-decorated defect in ELTRAN wafers as a function of the presence of additional 100nm thermal oxide growth.

After growth of 100nm oxidation film on the ELTRAN wafer, dsod density is 2.52 /cm^2. Using Cu-decoration method, ELTRAN wafer on 100 nm thickness oxide layer is found to have a seven times more defect density than the wafer without oxide film. This is due to the size of the defect increase after oxidation. Therefore, it occurs the breakdown at lower electric field. Figure 6 is TEM image for Cu-ion deposition of ELTRAN wafer on the function of applied voltage.

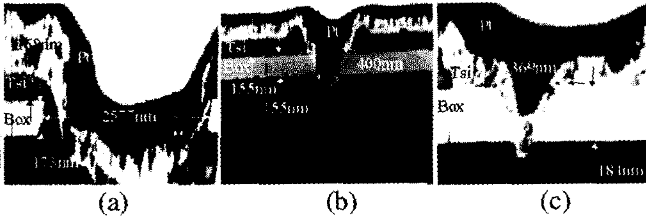

Fig. 6. Cross-sectional TEM images of Cu-decorated defects for as-ELTRAN wafers as a function of the applied bias voltage. (a) 30 V, (b) 50 V, and (c) 80 V.

The typical type of defects is square defect without top silicon layer. There is not epitaxial silicon growth because of a particle on the surface of ELTRAN wafers. Therefore, leakage path form between Cu ion and the interval of silicon substrate on the square defect during applied voltage and Cu ion deposit the position of the defect on the surface of ELTRAN wafers. The size of defect decreases with increase of applied voltage. In Fig. 6(a), the size of the defect is 2577 nm at 30 V, the thickness of buried oxide is 173 nm. The thickness of top silicon layer is 168 nm. After the applied voltage increase, the size of the defect is 400 nm at 50 V in Fig. 6(b). The thickness of top silicon and buried oxide layer is equal to 155 nm. In Fig. 6(c), the size of defect is 369 nm at 80V, the thickness of buried oxide layer is 184 nm. Figure 7 is TEM image of ELTRAN wafer after the growth of 100nm oxide layer through applied voltage. ELTRAN wafer with 100 nm oxide film has increasing defect density with applied voltage and have larger defects than ELTRAN wafer without oxide film. This is due to the square defect during epitaxial growth. The growth of oxide layer consume the silicon layer of 44 percent below and grow 56 percent upper. In Fig. 7, top silicon layer reduces and the size of square defect can not be known with the image of TEM because it is too large.

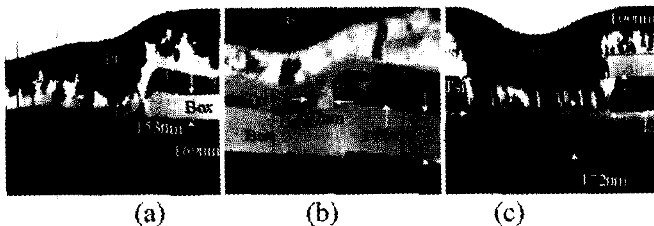

Fig. 7. Cross-sectional TEM images of Cu-decorated defects for ELTRAN wafers grown with additional 100 nm of thermal oxide film as a function of applied bias voltage. (a) 30 V, (b) 50 V, and (c) 80 V.

It is known that the size of defect through SEM image is about 4~6um and top silicon layer and buried oxide layer don't grow. In Fig. 7(a), the thickness of top silicon layer is 153 nm, buried oxide is 169 nm at 30 V. The size of the defect contacts the buried oxide layer because of thin top silicon layer. Top silicon layer is 169 nm and buried oxide layer is 184 nm at 60 V in Fig. 7(b). The crack is shown at buried oxide layer. Cu ion deposits at the surface of ELTRAN wafer because leakage current path occur to the Cu ion and silicon substrate during applied voltage. Figure 7(c) shows the accurate image of the square defect at 80 V. The size of the defect is 1036 nm and don't grow the top silicon layer. Top silicon layer is 118 nm, buried oxide layer is 172 nm. The oxide layer has a 100 nm oxide layer on the top silicon layer.

3.3 Morphology of surface formation on ELTRAN wafers

Figure 8 shows the square defect formation mechanism of ELTRAN wafers. Porous Si is formed due to anodization on the device wafer, and then epitaxial silicon is grown. Anodization is the electrical method. The etching particles of silicon exist with high concentration in anodization bath during porous Si formation. We have to remove the particles with continuous cleaning process. If they are not removed, the particle adheres to the surface of wafer. Especially, the particles of Si grow the Si_xO_y particles for porous Si during oxide layer growth. Once the particle adheres to the surface of wafer, epitaxial silicon layer doesn't grow at the part of particle. The particle on the surface should be remained during bonding through cleaning, etching process. We define the square defect to this position of the defect. The square defects partially don't have epitaxial silicon layer in Fig. 8, and are easily observed during HF defect and Secco defect experiment because of large defect size after buried oxide etching.

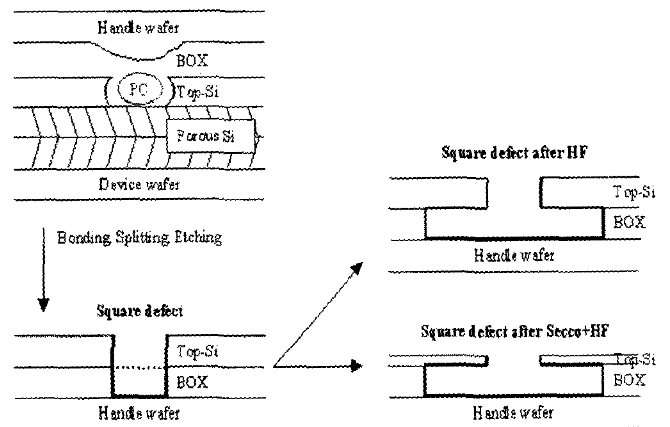

Fig. 8. Square defect formation mechanism on ELTRAN wafer.

4. CONCLUSION

We analysis for defects on ELTRAN wafers and know that the size of defect is 7.29 um by AFM analysis, the density of defect is 0.36 /cm^2 at as-dsod, 2.52 /cm^2 at ox-dsod. The as-dsod wafer has not the oxidation on ELTRAN wafer, but the ox-dsod wafer have the oxidation on ELTRAN wafer. The chiefly defect of ELTRAN wafer is the square defect. The particle of Si type is the source of square defect at anodization during ELTRAN process. In other words, it is caused by particles in case of oxidation of pore wall after porous Si growing. It is able to improve with cleaning using DI water. DI water is avoids the porous Si from chemical reaction. Also, during porous Si formation, it reduces the occurrence of the particle due to difference of porosity density. And for the fabrication of ELTRAN wafer under 100nm of top silicon layer, we have to change with the method of low epi layer film at 650 °C but now the method of high epi layer film at 1135 °C.

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