# Design of 60 GHz Millimeter-Wave Frequency Doubler using Distributed Structure

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## Abstract

A millimeter-wave distributed frequency doubler has been designed with distributed block and frequency tunable output reflectors. The simulated conversion loss of 9.5 dB to 7.7 dB from 54.6 GHz to 62.4 GHz output frequencies is achieved with fundamental and third harmonic signal rejections of more than 10 dBc. The fabricated chip has the size of 1.2 mm×1.0 mm. Some measured results of frequency and bias dependent characteristics are presented for the fabricated PHEMT MMIC frequency doubler. The designed doubler has two transistors, and if one of the transistors fails the doubler unit still operates with reduced gain. The failure effect of the PHEMT has been simulated, and compared to the measured data of which one PHEMT is not operating properly.

***Key words*** : Frequency Multiplication, Monolithic Microwave Integrated Circuit, Distributed Doubler.

## Ⅰ. Introduction

With the growth of wireless communication and increasing data rate, wideband, low noise and stable sources are required in millimeter-wave(MMW). So, the importance of frequency multiplier is increasing. Most of the reported frequency multipliers are based on the narrow band single ended designs implemented by using diodes or FETs[1]~[3]. Active frequency multipliers have the advantage of good conversion gain over the diode-based types. Single ended topology has the advantage of allowing a compact size. In order to have the wideband operation at higher frequency, a balanced distributed monolithic microwave integrated circuit (MMIC) multiplier was proposed using common-source/common-gate FETs to achieve the 180° out-of phase characteristics at the input[4]. For the MMW frequency, a balanced V-band doubler that employed a balun and two single ended doublers with common source HEMTs were reported[5].

The balanced topology can easily achieve the good fundamental and odd harmonic rejections with in-phase and out-of-phase combinations[6]. However, this topology has the conventional drawbacks which require large area and more numbers of transistors.

This paper presents the MMIC design of a pseudomorphic high electron mobility(PHEMT) distributed frequency doubler which is operating at V-band. Based on a 0.1 um GaAs PHEMT process and coplanar waveguide(CPW) technology, the doubler is designed by using the broadband distributed block and the reflector block of a LC notch filter and a transmission line stub at the output to reject the fundamental and the third harmonic instead of using the balanced topology. The designed frequency doubler uses two PHEMTs, and the effect of transistor failure has been simulated and compared to some measured data.

## Ⅱ. Device Characteristics and MMIC Fabrication

The MMIC distributed doublers have been fabricated using the GaAs based PHEMT process developed by MINT, Seoul, Korea. The active device is a 0.1 um gate-length PHEMT with a unit current gain frequency ($f_T$) and a maximum oscillation frequency(fmax) of 106 GHz and 160 GHz. The passive components include thin film resistor, metal-insulator-meta(MIM) capacitor which has the measured characteristics of 30.2 ~33.4 ohm/□ and 0.458~0.538 fF/um$^2$. This library also includes the CPW transmission lines of various characteristic impedances(35, 50, and 70 ohm)[7].

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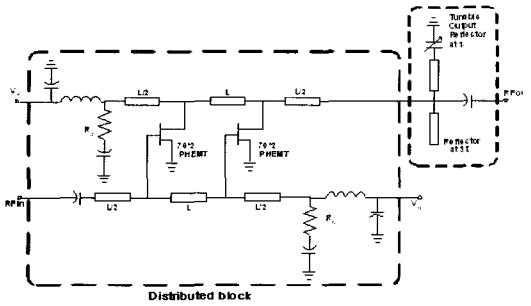


Fig. 1. Designed frequency doubler consisting of distributed block and tunable output reflector.

## Ⅲ. Circuit Design

Fig. 1 is the circuit schematic of the 60 GHz distributed frequency doubler. The input signal travels down to the transmission line, goes through the active devices, and finally is absorbed by the gate termination resistor Rg. The second harmonic signal that is generated by the nonlinear active devices travels down to the output port. Some of the reflected wave of the second harmonic signal will be absorbed by the drain termination resistor.

The doubler consists of the distributed block and the output reflectors. The distributed block is designed by using transmission lines and two identical PHEMTs, each with two-finger gate and total gate-width of 140 um. In order to reduce the dc power consumption and generate the large second harmonic signal, the transistors are biased near the pinch-off region, where the nonlinearity of trans-conductance versus gate-to-source voltage is used for frequency doubling.

Coplanar lines are used to form the artificial gate and drain transmission line low pass filters with the Cgs and Cds. In order to pass the fundamental signal in the gate line, the cutoff frequency of the gate line filter is set as 33.9 GHz. The cutoff frequency of the drain line filter needs to be doubled for that of gate line filter. The gate and drain line length are determined by the design equation in [8] as

$$Z_0 = \sqrt{\frac{L}{C}}$$
$$f_c = \frac{1}{\pi\sqrt{LC}}$$
$$\beta l = \frac{LR_0}{Z_h} \quad (1)$$

where $\beta l$ is the electrical length of the inductor section, C is the capacitance $C_{gs}$ or $C_{ds}$, and $Z_h$ is the impedance of the transmission line.

The input gate filter from 25 to 30 GHz operation and output drain filter from 50 to 60 GHz are designed to provide the broad-band operation. In order to reduce the chip size, the transistor biasing circuits are integrated with the input and output matching networks.

The fundamental and 3rd harmonic reflector circuits of the drain line are used to reflect the undesired signals from the output. Modifying or tuning these reflector circuits can change the operating frequency with the same distributed circuit block, so the frequency doubler can be used to have frequency selectivity. For this doubler design, the third harmonic suppression is much better than the fundamental suppression, so changing the resonance frequency of the fundamental frequency reflector by changing the capacitance can improve the doubler characteristics of the harmonic suppression and the operating bandwidth.

Fig. 2 shows the output power with changing the fundamental reflector frequency. Fig. 3 shows the fundamental and third harmonic suppression by using the tunable reflector. Unconditionally stable operation is achieved by an additional RC parallel network in the drain and gate bias network, which also serves for RF bypassing to desensitize the external biasing circuit.

MMIC design requires some tolerances for the fabrication processes. The distributed structure will still work even if one of the two transistors fails to operate properly. The failure simulation has been done for the worst case when a transistor terminal is open or short. Fig. 4 shows the output power when one of the two PHEMTs is short or open. The multiplication gain degrades by 2.5 dB to 5.5 dB for the operating frequency band, but multiplier is still operating.

The doubler performance is simulated by the har-

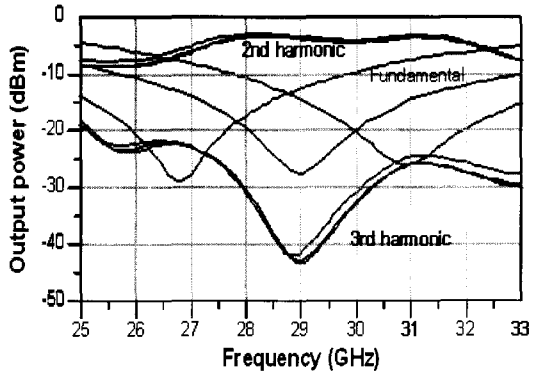


Fig. 2. Output power with changing the resonance frequency of $f_0$ reflector.

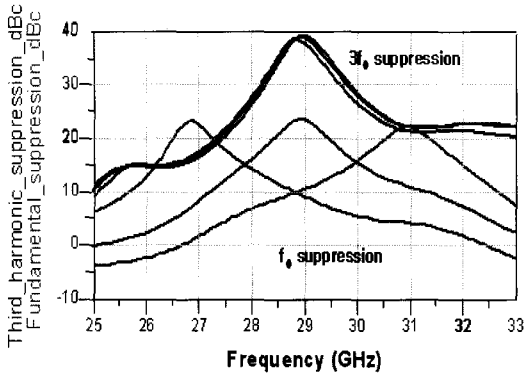


Fig. 3. Fundamental and third harmonic suppression with changing the resonance frequency of $f_0$ reflector.

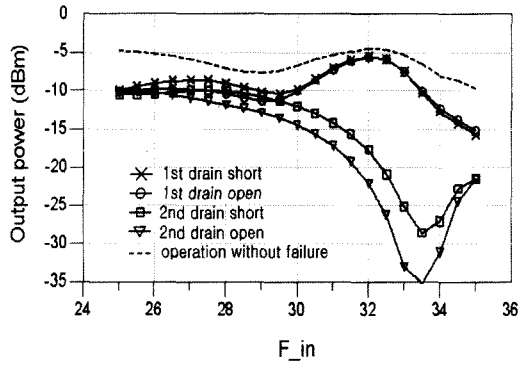


Fig. 4. Output power simulations for the case of one transistor failing(short or open).

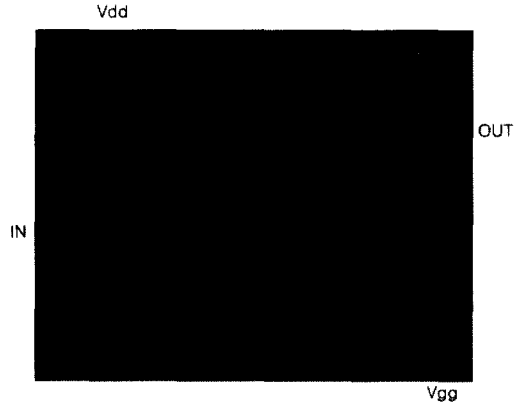


Fig. 5. Top-view photograph of the fabricated MMIC frequency doubler(1.2 mm × 1.0 mm).

monic-balance technique implemented in the commercial computer-aided design(CAD) software(ADS from Agilent). The nonlinear HEMT model used in the simulation is 70 × 2 um PHEMT large signal model developed by MINT. Fig. 5 shows top-view photograph of the fabricated V-band distributed frequency doubler. The chip size is 1.2 mm × 1.0 mm.

## Ⅳ. Measurement Results

The fabricated MMICs were measured using the on-wafer probing system. For the measurements, RF input signal at 20~35 GHz was generated by an Agilent E8244A signal generator. The output signal was measured by Agilent E4407B spectrum analyzer and 83557A MMW source module. In the measurement of the complete doubler, the transistors are all biased near the pinch-off region in the dc-IV curves. This bias is about $V_{gs}$ = −1.5 V and $V_{ds}$ = 2.0 V. It is observed that the conversion performance becomes saturated at input signal level of 8 dBm. The measured output power

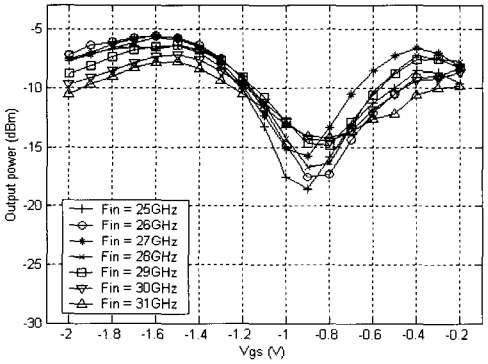


Fig. 6. Measured output power for the gate-sourc bias at RF input signal level of 8 dBm and $V_{ds}$ = 2.0 V.

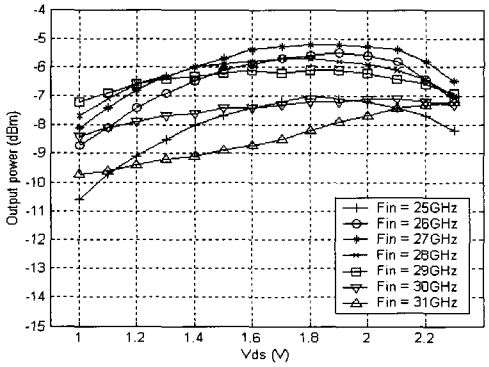


Fig. 7. Measured output power for the drain-source bias at RF input signal level of 8 dBm and $V_{gs}$ = - 1.5 V.

signal levels for changing the gate-source and drain-source bias at RF input frequency from 25 GHz to 31 GHz are plotted in Fig. 6 and Fig. 7.

Fig. 8 shows the measured conversion loss and rejections with the input frequency(20 GHz × 35 GHz) at the input power of 8 dBm. For some frequencies, the conversion loss and the fundamental signal rejection reach to 13.4 dB and 15.5 dB. The measured conversion loss is between 13.4~15.4 dB across 20~31 GHz input frequencies. In the measurement, the fundamental and third harmonic rejections reach to 15.5 and 20.2 dB. The output power for changing input power levels from −10 to 8 dBm is measured at the 25, 27, and 29 GHz, respectively. It is observed that the conversion loss is good at the 25 GHz frequency.

Fig. 9 shows the measured output power for a non-proper working chip. The chip has a half of the saturated current(Idss) compared to the proper working chips. The 2nd PHEMT of the chip seems to fail in the

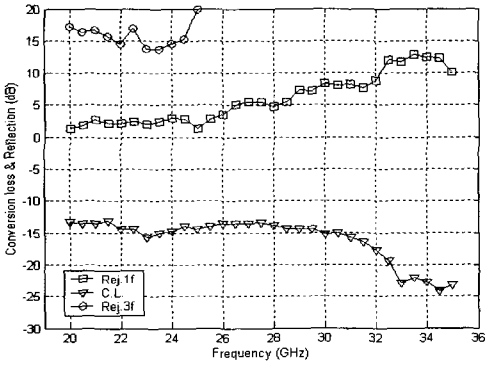


Fig. 8. Measured conversion loss and rejection of the fundamental and third harmonic at the input power level of 8 dBm.

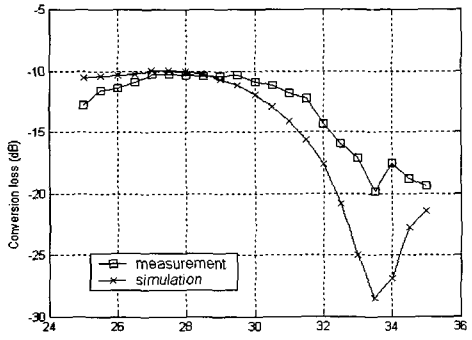


Fig. 9. Output power measured and simulated for the 2nd FET drain short.

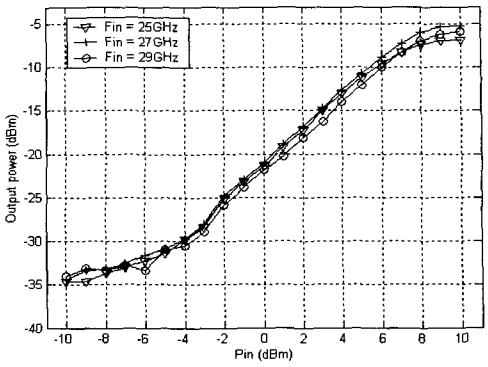


Fig. 10. Measured output power with changing input power.

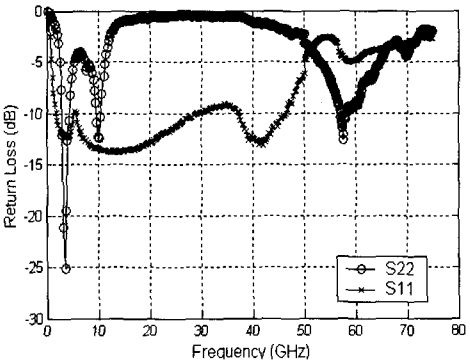


Fig. 11. Measured input loss and output return loss of the broad-band distributed doubler.

fabrication process. The conversion loss is about 18 dB which is about 4 dB worse than the other proper working chips. The measured data is similar to the simulated data of second FET drain short.

Fig. 10 shows the output power with changing input power at 25 GHz, 27 GHz and 29 GHz. This graph has linear increasement characteristics at the input with −4 to 8 dBm.

Fig. 11 shows the measured small signal parameters of the return loss at the input and the output port. The S11 shows wideband characteristics from about 20 to 40 GHz and the S22 has a good matching characteristics around 58 GHz.

## V. Conclusions

A compact and wide-band MMIC distributed doubler using LC notch filter and $3f_0$ /4 open stub for reflecting fundamental signal and the third harmonic instead of using the balanced topology has been described in this

paper. The frequency doubler can be designed to have the different operating frequency by modifying the reflector circuits with the same distributed circuit block. This circuit has the unconditional stability by using RC parallel network and also operates at broad-bandwidth with the input matching from 20 to 40 GHz. The measured conversion loss is 13.4~15.4 dB and the fundamental and third harmonic rejections reach to 13.4 and 20.2 dB, respectively. The designed distributed doubler will still operate with reduced conversion gain, if one of the two transistors fails. The chip size is 1.2 mm × 1.0 mm. So, this work will be useful for multi-band applications which requires frequency changing over broadband MMW spectrum.

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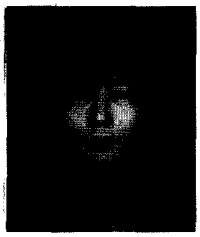

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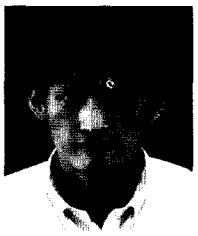

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