Multi-Gbit/s Digital I/O Interface Based on RF-Modulation and Capacitive Coupling

Hyunchol Shin

Abstract

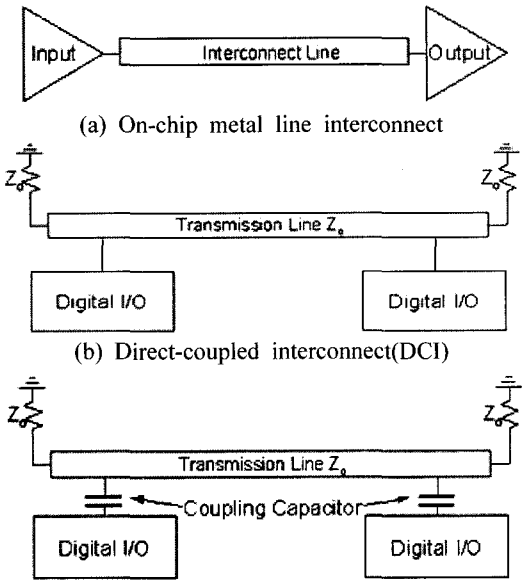
We present a multi-Gbit/s digital I/O interface based on RF-modulation and capacitive-coupling over an impedance matched transmission line. The RF-interconnect(RFI) can greatly reduce the digital switching noise and eliminate the dc power dissipation over the channel. It also enables reduced signal amplitude(as low as 200 mV) with enhanced data rate and affordable circuit overhead. This paper addresses the system advantages and implementation issues of RFI. A prototype on-chip RFI transceiver is implemented in 0.18-μm CMOS. It demonstrates a maximum data rate of 2.2 Gbit/s via 10.5-GHz RF-modulation. The RFI can be very instrumental for future high-speed inter- and intra-ULSI data links.

Key words : RF Interconnect, CMOS RF Integrated Circuit, High-Speed Digital Interface.

I. Introduction

On-chip, chip-to-chip, package-to-package or board-to-board interconnect has become the speed bottleneck as the interconnect transmission latency exceeds the active device delays. It is now generally recognized that conventional interconnect will soon encounter fundamental limits in meeting the future ULSI interconnection needs[1]. On-chip interconnect, as shown in Fig. 1(a), is limited by the $R \times C$ time delay, $I \times R$ voltage drop and crosstalk. Chip-to-chip interconnects are often limited by the dispersive transmission medium characteristics and poor noise immunity. The most popular direct-coupled interconnects(DCI) over a matched transmission line between chips is shown in Fig. 1(b). Both of the Gunning Transceiver Logic(GTL)[2] and Rambus Signaling Logic(RSL)[3] fall into this category. DCI typically uses large signaling level to maintain sufficient noise margin from the switching noise and consumes significant dc power through the interconnect.

The capacitive-coupled interconnect(CCI), as shown in Fig. 1(c), has advantages of dc-blocking between the I/O's and eliminating low-frequency disturbance coupling into the transmission medium. The CCI has been used in long-distance transcontinental interconnects or short-distance high-speed back planes. However, due to its low frequency blocking nature, CCI often requires additional signal processing techniques



(a) On-chip metal line interconnect

(b) Direct-coupled interconnect(DCI)

(c) Capacitive-coupled interconnect(CCI)

Fig. 1. Conventional on-chip and off-chip high speed digital interconnect schemes.

such as quantized feedback or encoding/decoding to recover the low frequency components of data[4]. CCI also incorporates off-chip coupling capacitors that are often too bulky to be integrated on a chip.

In order to solve the problems imposed by the conventional DCI and CCI, we proposed a novel RF-

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High-Speed Integrated Circuit and System Lab., Department of Radio Science and Engineering, Kwangwoon University, Seoul, Korea.

interconnect(RFI) system concept for transmitting data by using RF-modulation and capacitive coupling over an impedance-matched microwave transmission line[5]~[7]. However, the previous works did not address specific system advantages of the RFI and practical implementation issues for digital I/O interface applications. This paper further elaborates the RFI system concept with specific transceiver architecture and modulation scheme to perform the I/O interface function. The improved noise immunity capability of the RFI system is also investigated along with the measured characteristics of a multi-I/O RFI channel. Finally, a prototype on-chip RFI is successfully implemented with 0.18 μm CMOS in demonstrating a 2.2 Gbit/s data transmission by using 10.5-GHz RF- modulation.

Ⅱ. RFI System Architecture

2-1 RFI System Architecture

RFI is based on RF-modulation and capacitive-coupling over an impedance-matched transmission line. Fig. 2 illustrates the intended RFI system architecture for chip-to-chip interconnection. It comprises a transmission line with both-ends terminated by its characteristic impedance(Z_o), coupling capacitors(C_c), and RF-transmitter/receiver(or RF-modulator/demodulator). The transmitter(Tx) modulates(up-converts) the baseband data with the RF-carrier(f_{RF}) then sends it to the channel through the capacitor C_c. The receiver(Rx), on the opposite end, demodulates(down-converts) the signal with the coherent f_{RF} to recover the data. The RF-modulation is used to enhance the coupling efficiency of the baseband data through the coupling capacitors. Since the data is upconverted to f_{RF}, the transmission channel must be designed to be low loss and low dispersion in the frequency range of interest, that is, (f_{RF}+data bandwidth). C_c is required to be large enough to minimize the coupling loss. A simple analysis of an equivalent circuit model of RFI channel yields a criterion of $Cc >> 10/(\omega_{RF} Z_o)$[6]. The RFI can be also implemented in the form of multi-drop I/O's as shown in Fig. 3, where each I/O includes its own RFI-transceiver.

2-2 RFI-Transceiver Architecture and Modulation Scheme

RFI-transceiver must be fully integrated on a chip.

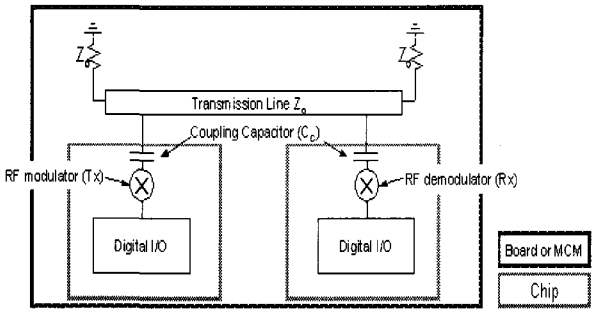


Fig. 2. RF-Interconnect system architecture for high-speed digital interconnects.

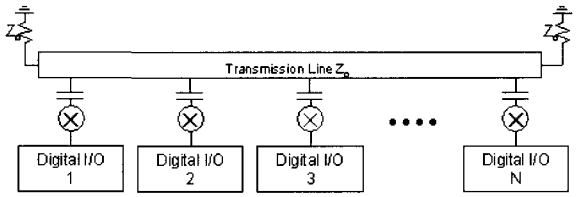


Fig. 3. Multi-I/O RFI configuration.

Thus, direct conversion transceiver architecture is the most suitable choice considering its minimized circuit complexity and reduced power consumption. Fig. 4 gives the RFI-transceiver architecture. The transmitter consists of a low-pass filter, an up-conversion mixer, and an output driver, and the receiver consists of a pre-amplifier, down-conversion mixer, and baseband amplifier, and a low-pass filter. Tx filter limits the transmitted signal bandwidth in order to minimize the inter-symbol interference, and Rx filter removes out-of-channel signal and noise components at the baseband. RF-carrier generation circuitry is required for LO signals in the transceiver. A global clock is

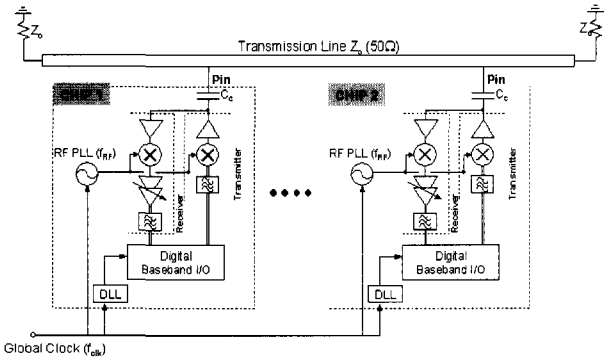


Fig. 4. RFI direct conversion transceiver architecture.

assumed to be available to provide the reference frequency for each I/O.

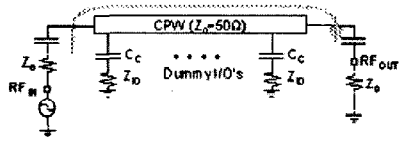
BPSK(binary phase shift keying) has been adopted as the modulation scheme in our RFI design because it suppresses the carrier frequency and minimizes the undesired dc-offset in the direct conversion receiver. The BPSK signal can also be coherently demodulated through the Costas loop that automatically synchronizes LO with an incoming signal[9].

Ⅲ. RFI System Advantages

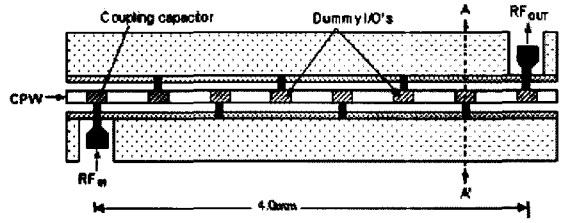
3-1 Signal-to-Noise Ratio Improvement

Switching noise is one of the major noise sources in a digital system. In this section, the RFI channel is analyzed to show its superiority in suppressing the switching noise.

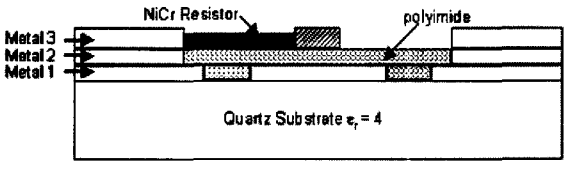
A prototype multi-I/O RFI channel is implemented with two active I/O ports(RF_{IN} and RF_{OUT}) at both ends and several inactive dummy I/O's along the channel, as shown in Fig. 5(a). The active ports are 4-mm apart with 50Ω-matched input impedance(Z_O) while the inactive ports are evenly distributed with higher input impedance(Z_{IO}). The transmission line is realized as a coplanar waveguide on a quartz substrate with a thickness of 625 μm and a dielectric constant (ε_r) of 4. Fig. 5(b) and (c) show the layout and cross-section of the test pattern, respectively. The input resistors(Z_{IO}) of dummy I/O's are formed by NiCr deposition and the coupling capacitors of 250 fF are realized with two metal layers(Metal-1 and Metal-3) separated by 1-μm thick polyimide.



(a) Circuit schematic of the channel with RF_{IN} and RF_{OUT} ports at both ends and dummy I/O's in between



(b) Layout of the test pattern

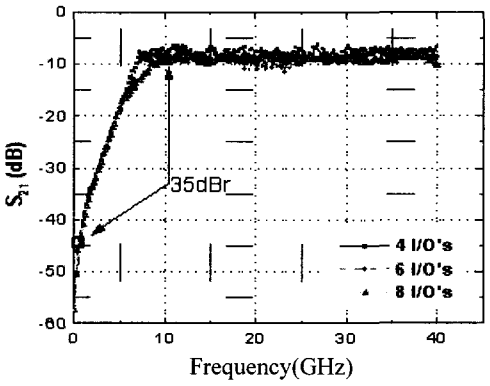


(c) Cross section(A-A') of the fabricated structure

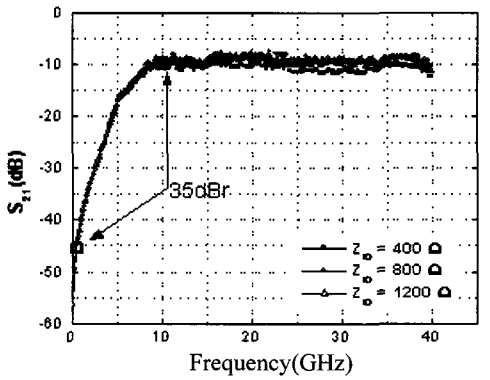
Fig. 5. Test pattern for characterization of a prototype RFI channel.

The transmission characteristics from RF_{IN} to RF_{OUT} are measured from 1 GHz~40 GHz by using a network analyzer. Fig. 6 shows the measured power transmission in dB with (a) varying the number of dummy I/O's(4, 6, 8) when Z_{IO} is 1.2 kΩ and (b) varying Z_{IO}(400, 800, 1200 Ω) with six dummy I/O's. It clearly shows that the high-pass characteristics with a low cut-off frequency around 9-GHz are measured for the entire range of Z_{IO} and the dummy I/O count in the experiment.

These high-pass characteristics can reduce the swi-



(a) With varying the number of dummy I/O's(4, 6, 8) when the input impedance(Z_{IO}) of dummy I/O is 1.2 kΩ.



(b) With varying Z_{IO}(400, 800, 1200 Ω) with six dummy I/O's.

Fig. 6. Measured transmission characteristics of the RFI channel.

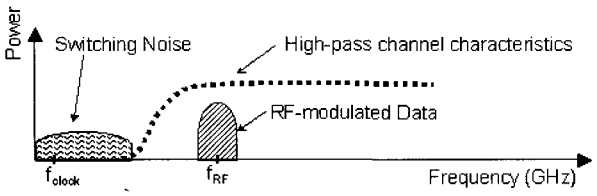


Fig. 7. Suppression of switching noise in RFI.

tching noise coupling from the on-chip digital circuitry into the channel and consequently improve the SNR. Fig. 7 illustrates that RF-modulation actually separates the data and the noise in the frequency domain and the noise is removed by the channel characteristics while the modulated data around f_{RF} passes through the channel.

The improvement of SNR can be estimated by examining the rejection ratio of the RFI high pass characteristics between f_{RF} and f_{clock}. Assuming the RF-carrier frequency(f_{RF}) is 10 GHz and digital clock frequency(f_{clk}) is 1 GHz, the rejection ratio is about 35 dBr under all measurement conditions given in Fig. 6. For more accurate estimation, we must integrate the switching noise suppression over the frequency bands. Nevertheless, 35 dBr is sufficient as a first order approximation. When taking into account the noise figure of RFI-transceiver(15 dB) and the signal coupling loss through the C_c(10 dB), the aggregate SNR improvement becomes 10 dB. This would correspond to an improved BER(bit error rate) by a factor of $>10^{-23}$ for BPSK signal with Gaussian white noise[1].

3-2 Low Signaling Level

Signaling level of interconnects should be determined with the simultaneous considerations on the power dissipation, noise margin, and data rate. Generally, it is desirable to lower the signaling level to reduce the power dissipation and increase the data rate, but the minimum swing is limited by SNR and BER requirements. For instance, differential signaling scheme was proposed to enhance the SNR by rejecting the common mode noise, and consequently lower the signaling level with increased speed[10].

RFI can lower the signaling level without such a differential signaling thanks to the improved noise immunity described in the previous section. Based on the extensive simulations including the circuit and channel non-idealities, we decide to use a 200-mV signaling level in RFI. However, a more analytical and experimental study is needed to choose an optimum signaling level in future. Low signaling level is also advantageous for low supply voltage applications in a scaled CMOS technology.

3-3 Wide Bandwidth and Easy Upgradability of RFI-Transceiver

As the carrier frequency becomes higher, the relative bandwidth(~Data Bandwidth/f_{RF}) occupied by the modulated data gets smaller than that without RF-modulation. It implies that RFI provides potentially larger effective bandwidth than a non-modulated system, just like the optical communication provides enormous bandwidth resource for data transmit. Thus, once RFI transceiver is implemented, it should be relatively easy to increase the data rate without much modification on the existing RFI transceiver, for instance, from 1-Gb/s to 3-Gb/s, because the relative bandwidths with respect to the carrier frequency are not much different for both cases.

3-4 Elimination of DC-Current Dissipation on the Channel

Usually DCI terminates the transmission line with a regulated dc voltage(for example, GTL uses 0.8 V for the termination voltage[2]). Thus, dc currents inevitably flow in either logic "1" or "0" states, which cause unwanted current dissipation due to the parasitic IR-drop in the transmission line. In contrast, RFI completely eliminates dc current dissipation in the channel due to the capacitive coupling and dc-free modulation of the baseband data.

3-5 Power and Circuit Overhead of RFI Transceiver

The circuit overheads of RFI system include RFI-transceiver and RF-synthesizer. In a 0.18-μm CMOS technology, typical power consumptions based on

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1. The BER of BPSK signal is given by $BER = Q\left(\sqrt{2\left(\frac{E_b}{N_o}\right)}\right)$, and a relatively simple closed-form upper bound for Q-function is given by $Q(z) < \frac{1}{\sqrt{2\pi}z} e^{-z^2/2}$. The BER improvement is calculated with z=10 dB, which gives a reasonable approximation.

preliminary designs are estimated to be 14 mW for RF-synthesizer, 20 mW for RFI-transceiver, and 16 mW for output driver, therefore 50 mW in total. The current consumption of RFI output driver is calculated to be 8 mA by assuming 200 mV-signaling over the 50-Ω doubly matched transmission line[11]. The power consumption of the baseband circuitry increases linearly proportional to the data rate as predicted by $p=f_{Clock} \cdot C_{Load} \cdot V_{DD}^2$, but the RFI power dissipation should keep almost constant regardless of the data rate. It is because RFI has larger effective bandwidth than conventional non-modulation interconnect schemes due to its use of high frequency RF-carrier. So, the power overhead becomes more affordable as the data rate gets higher.

Ⅳ. RFI Prototype Demonstration

4-1 Design and Implementation

To demonstrate the feasibility of RFI concept, we implemented a prototype RFI on a chip. Although it is not a chip-to-chip interconnect, it proves the concept of RFI for high speed operation. The designed chip architecture is given in Fig. 8. Since the transmission line is relatively short, the output driver and the pre-amplifier are not included in this implementation.

A balanced passive switching mixer is designed for the up-conversion in Tx, whose conversion gain is −6 dB. The LO carrier suppression is simulated to be less than −28 dBc. The output signal is linked to the transmission line through a coupling capacitor of 100 fF. On the receiver, a Gilbert-cell down-conversion mixer is designed whose circuit schematic is shown in Fig. 9. The down-conversion mixer accepts single-ended signal from the coupling capacitor and converts it to a differential form. A variable gain amplifier

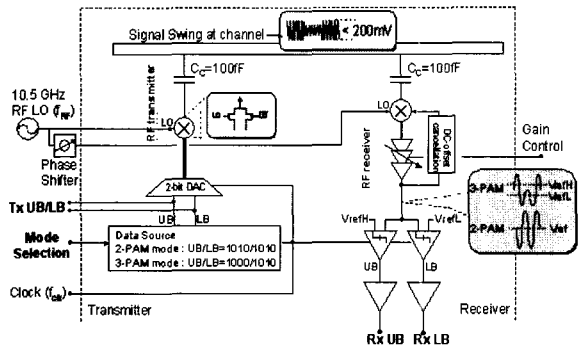

Fig. 8. Prototype chip architecture for on-chip RFI demonstration.

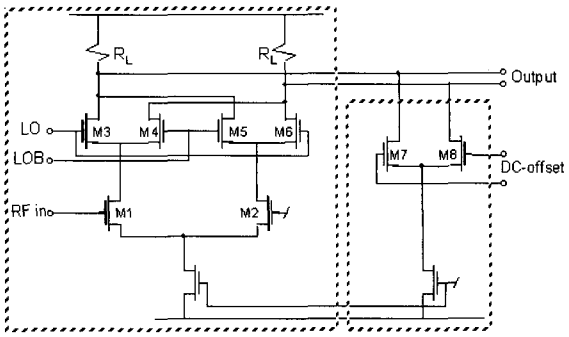

Fig. 9. Circuit schematic of down-conversion mixer with dc-offset cancellation circuit.

(VGA) is included to compensate for unexpected loss and keep the signal swing constant thereafter. The gain variation of 14 dB~24 dB is achieved by changing the effective width of the differential pairs. An advantage of the width scaling method is that it ensures high input linearity and low gain for large input and low input linearity and high gain for small input, as is usually required by Rx VGA[12]. No inductors are used as loads in the receiver in order to support high baseband data rate up to 2 GHz. Even though the LO signal is suppressed in the transmitted spectrum, the dc-offset is still a critical problem in a direct conversion receiver. Thus, an offset cancellation feedback circuit is included, which operates either in closed-loop or open loop. It senses the dc-offset voltage from the baseband amplifier outputs and feed the cancellation signal back to the amplifier input. The RF-modulated signal amplitude is designed to be ±0.1 V on the channel due to the great improvement of noise immunity.

Besides the RFI-transceiver, we have designed digital baseband circuitry to permit functional testing of RFI as also shown in Fig. 8. The data source in the transmitter can generate either binary(2-PAM) or 3-level(3-PAM) data depending on the mode selection. The 3-PAM signaling is intended for demonstrating the RFI's potential capability for multi-level signal transmission. The two-bit(UB/LB) fixed patterns from the data source correspond to 1010/1010 for 2-PAM and 1000/1010 for 3-PAM. A current-switch type DAC adds the UB/LB to yield the 2-PAM or 3-PAM data, thus generates levels "2"/ "0" for 2-PAM and levels "2"/ "1"/ "0" for 3-PAM. In the receiver, the baseband signal is recovered by two dynamic comparators with reference voltages of V_{refH} and V_{refL} in 3-PAM mode or a common V_{ref} in 2-PAM mode, as shown in the inset of Fig. 8. The potential dc-offset issue that is inherent in

any zero-IF receiver is resolved by a dc-offset cancellation technique as shown in Fig. 9. It shows the circuit schematic of the feedback dc-offset cancellation in the down-conversion mixer.

A prototype transceiver is fabricated in a 0.18-μm 1-poly 6-metal CMOS technology. A chip micrograph is shown in Fig. 10. The metal-insulator-metal(MIM) coupling capacitors of 220 fF are realized with an area of 220 μm^2. The length of the interconnect line between the transmitter and receiver is about 0.5 mm. The total transmitter and the receiver consume chip areas of 220×150 μm^2 and 330×170 μm^2, respectively, while the RF-transceiver takes only 300×140 μm^2.

4-2 Measurement Results

The chip is tested on-wafer using a high frequency probe card. The Transmit and Receive signal(Tx and Rx UB/LB) are measured and compared to see the functionality of the chip[8]. The 10.5-GHz 0.3 V_p LO is supplied externally and a phase shifter is used to adjust the phase difference. The RF-transceiver consumes 9.5 mA from a 2.0 V supply.

Fig. 11 shows the measurement results for 2-PAM mode transmission with 2-GHz clock, where the transmitted(Tx UB) and received(Rx UB) data are shown together. Rx UB is measured with the RF LO turned on and off. It clearly illustrates that no signal is detected without RF LO. Thus, RFI is operational with the RF-modulation and the capacitive coupling.

The operation modes are switched between 3-PAM and 2-PAM with a periodic signal applied to the mode selection. Fig. 12 shows measurement results for the received data(Rx UB/LB) along with the simulated waveforms for the mode selection(Mode), the transmitted data(Tx UB/LB), the modulated signal on the channel(Channel), and the received data(Rx UB/LB). It shows that the data is successfully transmitted without error. With a 1.1-GHz clock, the aggregate data rate of 2.2 Gbit/s is achieved for both channels(UB/LB). It should be noted that the effective signaling level in 3-PAM mode is only 100 mV, which is only half of 2-PAM mode. It implies that this RFI can be extended to handle 4-PAM signal once it is fully implemented with 2-bit DAC and ADC.

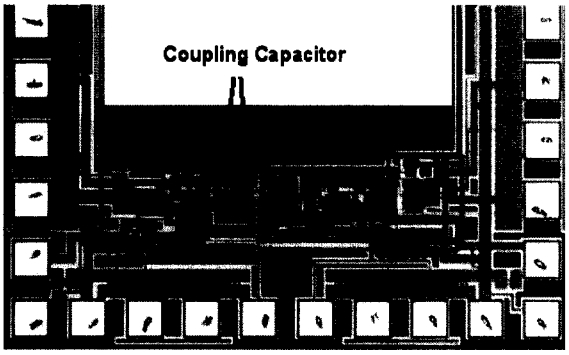

Fig. 10. Chip micrograph.

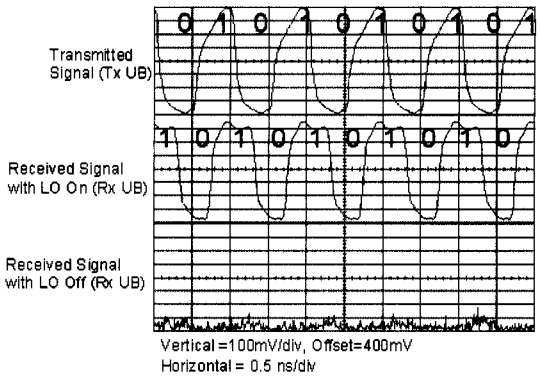

Fig. 11. Measurement results for data transmission with clock frequency of 2 GHz and RF-carrier of 10.5 GHz.

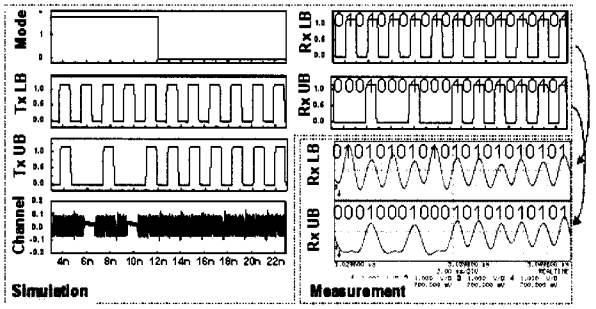

Fig. 12. Simulation and measurement results for 2.2 Gbit/s data transmission with clock frequency of 1.1 GHz and RF-carrier of 10.5 GHz exhibiting mode change from 3-PAM to 2-PAM.

V. Conclusions

We present a multi-Gbit/s digital I/O interface based on RF-modulation and capacitive-coupling over an impedance matched transmission line. The RF-interconnect(RFI) can greatly reduce the digital switching noise(>35 dB) and improve the system SNR by at least 10 dB. As a result, the RFI enables reduced signal amplitude(as low as 200 mV) in transmission with

enhanced data rate and affordable circuit overhead. With the high pass nature of the capacitive coupling, the RFI also eliminates the dc power dissipation over the channel. The prototype on-chip RFI demonstrates a maximum data rate of 2.2 Gbit/s via 10.5-GHz RF-modulation in a 0.18 μm CMOS technology. We believe that the RFI is an excellent candidate for use in future high-speed intra- and inter-chip interfaces.

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Hyunchol Shin

received the B.S., M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejon, Korea, in 1991, 1993 and 1998, respectively.

His graduate research was focused on the high frequency III-V devices and MMIC design. During 1997, he was on leave at Daimler Benz Research Center, Ulm, Germany as a doctoral research student where he worked on InP/InGaAs HBT's. In 1998, he joined Samsung Electronics as a Senior Engineer, where he was involved in the RF/IF chipset development for CDMA mobile handsets. From 2000 to 2002, he was with the Electrical Engineering Department of the University of California, Los Angeles as a Research Associate and a Lecturer, where he had been working on the RF circuit design in CMOS and SiGe BiCMOS technology. From 2002 to 2003, he worked for RF/Analog IC Design Group, Qualcomm Inc., San Diego, CA. where he had been involved in the advanced RF Transceiver Design. In September 2003, he joined Kwangwoon University as an Assistant Professor. His current research interests are RF/Analog circuits and System Design and Microwave Integrated Circuit Design by using CMOS, SiGe BiCMOS, and III-V technology.