Application of the EKV model to the DTMOS SOI transistor

Jean-Pierre Colinge and Jong-Tae Park

Abstract— **The EKV model, a continuous model for the MOS transistor, has been adapted to both partially depleted SOI MOSFETs with grounded body (GBSOI) and dynamic threshold MOS (DTMOS) transistors. Adaptation is straightforward and helps to understand the physics of the DTMOS. Excellent agreement is found between the model and the measured characteristics of GBSOI and DTMOS devices**

Index Terms— **Silicon-on-Insulator technology, MOS devices, Insulated gate FETs**

I. INTRODUCTION

The Enz-Krummenacher-Vittoz (EKV) model is a continuous model developed for MOS transistors. Because its equations are valid in all regimes of operation, above or below threshold, as well as in saturation, the EKV model is highly suitable for the simulation of analog and low-voltage circuits.[1,2] The EKV model has successfully been adapted to inversion-mode and accumulation-mode fully depleted SOI transistors. [3,4] The DTMOS SOI transistor is a partially depleted device where contact is made between the gate and the floating body. The device is sometimes referred to as VCBM (Voltage-Controlled Bipolar CMOS) [5], MTCMOS (Multiple-Threshold CMOS) [6], hybrid bipolar-MOS transistor [7,8], or DTMOS [9] and is mainly used for low-voltage (e.g. 0.5V) CMOS applications.[10] Several models have been proposed for the DTMOS.[11,12] In this Letter we propose to adapt the EKV model to the device, which is most appropriate, since both the model and the device are optimized for low-voltage, low-power applications.

II. MODEL

The EKV model for the EKV MOSFET is described in detail in [2]. The drain current is a continuous function of the terminal voltages and is given by the following expression:

$$\mathrm{I_D} = 2\mathrm{n}\,\mu_\mathrm{n}\,\mathrm{C_{ox}}\,\frac{W}{L}\left(\frac{kT}{q}\right)^2 \times \left[\left\{\ln\left[1+\exp\left(\frac{V_P-V_S}{2kT/q}\right)\right]\right\}^2 - \left\{\ln\left[1+\exp\left(\frac{V_P-V_D}{2kT/q}\right)\right]\right\}^2\right] \tag{1}$$

where $$V_P = \frac{(V_G - V_{TH})}{n} \tag{2}$$

is the saturation drain voltage above threshold that should be applied to the channel to cancel the effect of the gate voltage and V_G, V_S and V_D are the gate, source and drain voltages, respectively.. The body effect coefficient is given by

$$n = \frac{1}{1 - \dfrac{\gamma}{2\sqrt{V_G - V_{THo} + (\frac{\gamma}{2} + \sqrt{2\Phi_F})^2}}} \tag{3}$$

where $\gamma = \dfrac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$ and $V_{THo} = \Phi_{MS} + 2\Phi_F + \dfrac{\sqrt{4q\varepsilon_{si}N_A\Phi_F}}{C_{ox}}$.

The value for the threshold voltage used in (1) is given

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Jean-Pierre Colinge is with Dept. of Electrical Engineering, University of California, Davis, CA 95616, USA

Jong-Tae Park is with Dept. of Electronics Engineering, University of Incheon, #177 Dohwa-dong, Nam-ku, Incheon 402-749, Korea

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$$V_{TH} = V_{THo} - \gamma\sqrt{2\Phi_F} + \gamma\sqrt{2\Phi_F - V_B} + 3\frac{kT}{q} \qquad (4)$$

In these expressions, V_B is the potential of the device body. All other symbols have their usual meaning. These equations, developed for a bulk MOSFET, were applied to grounded-body partially-depleted SOI transistors and DTMOS devices by setting V_B equal to V_S or to V_G, respectively. No other modification to the model was required. As far as the DTMOS device is concerned the model can only be used for gate voltages lower than $2\Phi_F$ in order for Equation (4) to admit real solutions. Since DTMOS devices are mostly used for very low-voltage operation [10], we will limit the scope of our study to values of gate voltage ranging from 0 to 0.5 V. Under these bias conditions the current NPN bipolar transistor present in the DTMOS is negligible compared to the MOS channel current.

III. EXPERIMENTAL

The devices used in this experiment are long-channel, partially depleted n-channel MOSFETs with body either tied to source (grounded-body MOSFET, or GBSOI) or tied to gate (DTMOS). The processing parameters are t_{ox} = 8 nm, N_A = 1.65x10^{17}cm^{-3}, W=10 μm, L = 2 μm. The gate material is N^+ polysilicon.

Figure 1 presents the threshold voltage in the GBSOI and the DTMOS device as a function of gate voltage. V_{TH} in the DTMOS decreases with increased gate voltage because of bulk-like substrate effect, as predicted by Equation 4. Figure 2 shows the current in both GBSOI and the DTMOS device as a function of gate voltage, for a drain voltage value of V_D=100 mV. The value for the electron surface mobility used in the model is 300 cm^2/Vs. The same set of equations (Equations (1) to (4)) and parameters is used for both devices. The only difference resides in setting V_B equal to V_S = 0V in the GBSOI and or to V_B = V_G in the DTMOS device. Figure 3 shows the transconductance dI_D/dV_G at V_D=100 mV

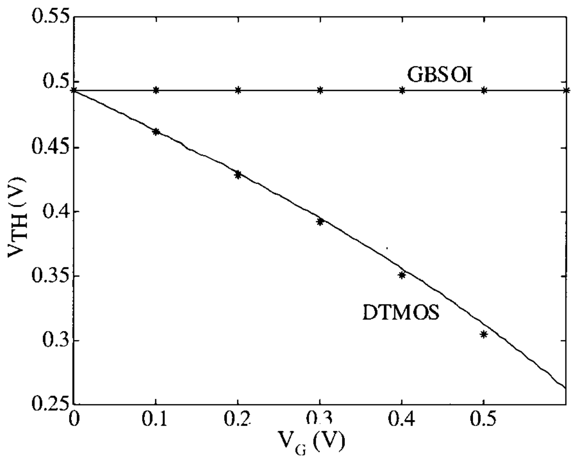

Fig. 1. Threshold voltage vs. gate voltage in grounded-body SOI (GBSOI) and DTMOS devices. Solid lies represent the EKV model and the (*) symbols represent the measured data.

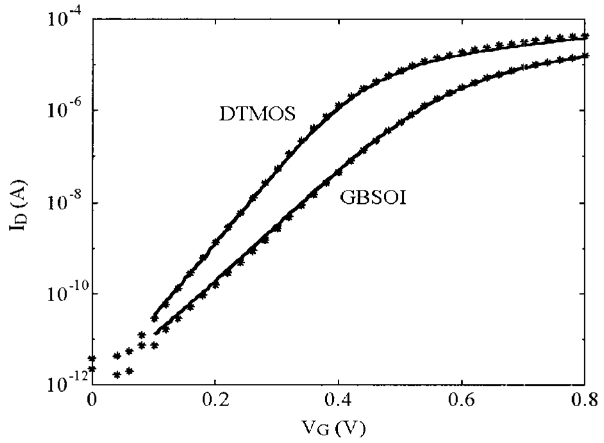

Fig. 2. Drain current vs. gate voltage in grounded-body SOI (GBSOI) and DTMOS devices. Solid lies represent the EKV model and the (*) symbols represent the measured data. V_D = 100 mV.

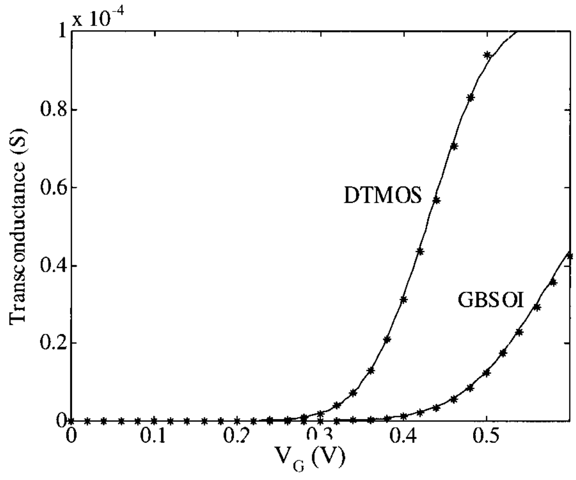

Fig. 3. Transconductance dI_D/dV_G vs. gate voltage in grounded-body SOI (GBSOI) and DTMOS devices. Solid lies represent the EKV model and the (*) symbols represent the measured data. V_D = 100 mV.

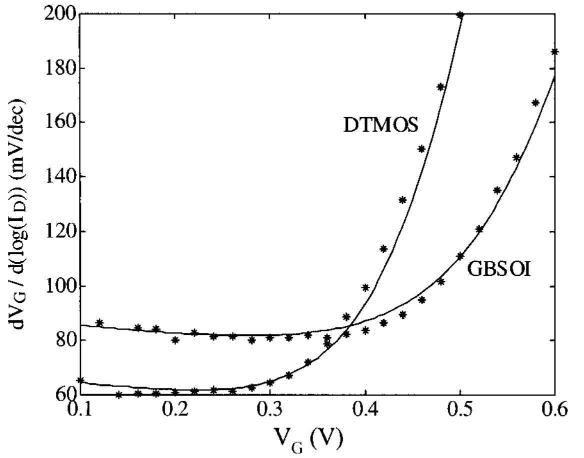

Fig. 4. $dV_G/d(\log(I_D))$ (subthreshold swing) vs. gate voltage in grounded-body SOI (GBSOI) and DTMOS devices. Solid lies represent the EKV model and the (*) symbols represent the measured data. V_D = 100 mV.

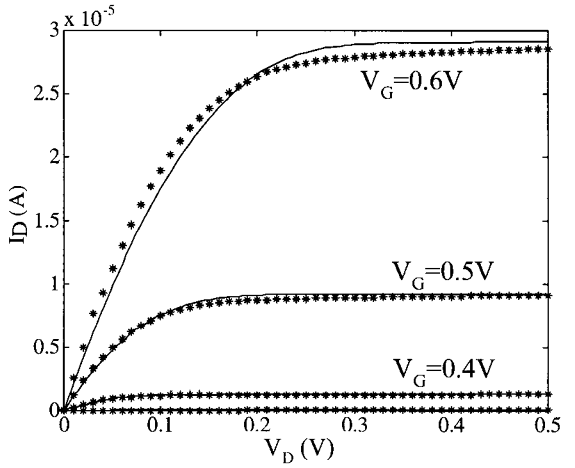

Fig. 5. Output characteristics of the DTMOS device. Solid lines represent the EKV model and the (*) symbols represent the measured data.

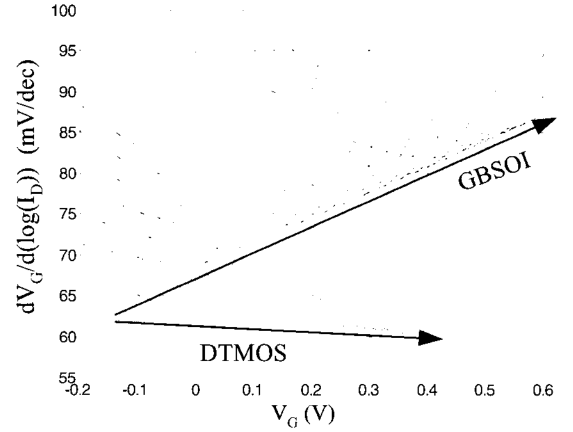

Fig. 6. $dV_G/d(\log(I_D))$ in GBSOI and DTMOS devices with t_{ox} = 3 nm; N_A ranges from 10^{16} to $2x10^{18}$ cm^{-3}.

for both devices. Figure 4 shows $dV_G/d(\log(I_D))$ for V_D=100 mV. Note that $dV_G/d(\log(I_D))$ is equal to the local subthreshold swing in the subthreshold regime. The model correctly predicts the subthreshold swing value close to the 60 mV per decade observed in the measured data. The reduction of subthreshold swing from 80 mV/decade in the GBSOI device to 60 mV/decade in the DTMOS is due to the reduction of threshold voltage with increased gate bias. Figure 5 shows the simulated and measured output characteristics of the device. Figure 6 shows $dV_G/d(\log(I_D))$ (subthreshold swing) vs. gate voltage in GBSOI and DTMOS devices. The minimum subthreshold swing value increases with doping concentration in the GBSOI device but stays relatively constant and close to 60 mV/decade in the DTMOS.

IV. CONCLUSION

The EKV model has successfully been employed to simulate DTMOS devices. This is done by using the classical model for a bulk MOSFET and imposing the substrate voltage to be equal to the gate voltage. The reduction of threshold voltage brought about by the increase of gate bias explains the increase of transconductance and the reduction of subthreshold swing observed in the DTMOS, compared to the grounded-body SOI MOSFET.. Excellent agreement is found between the model and experimental data for $I_D(V_G)$, transconductance and subthreshold swing characteristics.

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Jong-Tae Park received the B.S. degree in electronics engineering from Kyungpook National University, Korea, in 1981, and the M.S. and Ph.D. degrees from Yonsei University, Korea, in 1983 and 1987, respectively, where he performed the device characterization and modeling of SOI CMOS.

From 1983 to 1985, he was a Researcher at Gold-Star Semiconductor, Inc., Korea, where he worked on the development of SRAM. He joined the Department of Electronics Engineering, University of Incheon, Incheon, Korea, in 1987, where he is a Professor. As a visiting scientist at Massachusetts Institute of Technology, Cambridge, in 1991, he conducted research in hot carrier reliability of CMOS. As a visiting scholar at University of California , Davis, in 2001, he conducted research on the device structure of Nano-scale SOI CMOS. His recent interests are device structure and reliability of Nano-scale CMOS devices, flash memory, and RF-CMOS.

Jean-Pierre Colinge received the B.S. degree in philosophy, the Elect. Eng. Degree, and the Ph.D. degree in applied sciences, all from the University Catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, and 1984, respectively.

From 1981 to 1985, he was with the Centre National d'Etuers des Telecommunications(CENT), Meylan, France, where he developed new silicon-on-insulator(SOI) and 3-D integration technologies using laser recrystallization. From 1985 to 1988, he was with the Hewlett-Packard Laboratories, Palo Alto, CA, where he was involved in thin-film SOI CMOS and bulk bipolar technologies for high-speed digital applications. From 1988 to 1991, he was with IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. From 1991 to 1997, he was Professor at the University Catholique de Louvain, leading a research team in the field of SOI technology for low-power, radiation-hard, high-temperature and RF applications as well as reduced-dimension devices (thin double-gate and quantum-wire MOSFETs). He is now Professor at the University of California at Davis. He has published over 240 scientific papers and three books on the field of SOI as well as a book on the semiconductor device physics.

Dr. Colinge has been on the committee of several conferences, including IEDM and SSDM, and has been General Chairman of the IEEE SOS/SOI Technology Conference in 1998.