Process Optimization for High Frequency Performance of InP-Based Heterojunction Bipolar Transistors

Yongjoo Song, Yongsik Jeong, and Kyounghoon Yang

Abstract—**In this work, process optimization techniques for high frequency performance of HBTs are presented. The techniques are focused on reducing parasitic base resistance and base-collector capacitance, which are key elements determining the high frequency characteristics of HBTs. Several fabrication techniques, which can significantly reduce the parasitic elements of the HBTs for improved high frequency performance, are proposed and verified by the measured data of the fabricated devices.**

Index Terms—**InP HBT, CDC technology, self-alignment, base-collector capacitance, base-pad isolation**

I. Introduction

InP-based heterojunction bipolar transistors (HBTs) are one of the best candidates for ultra high frequency analog, digital and mixed signal integrated circuits due to their inherent material properties [1-5]. These merits result from excellent electron transport characteristics of their material systems, such as the high electron mobility and the high peak electron drift velocity. Also, the small surface recombination velocities both in InP and InGaAs are advantageous for fabricating sub-micron emitter devices for high-speed/high-density ICs without a serious degradation in the current gain [6]. In addition, InP-based HBTs provide low-voltage operation owing to the small band-gap energy of InGaAs. Moreover, InP-based HBTs are very attractive for optoelectronic integrated circuits (OEICs) due to their capability for the monolithic integration with long-wavelength optical devices [4].

It is well-known that the base resistance (R_b) and the base-collector capacitance (C_{bc}) are key elements determining the maximum oscillation cut-off frequency (f_{max}) of HBTs by $f_{max} \approx [f_T/(8\pi R_b C_{bc})]^{1/2}$. For this reason, many attempts to minimize R_b and C_{bc} have been made [5-13]. According to the above relation, a small base resistance is desired for high oscillation cut-off frequency. Because the base sheet resistance is relatively larger than the base contact resistance, minimum contact spacing between the emitter-base junction and the base metal is essential to realize small base resistance in the HBT. A self-aligned emitter-base contact technique is generally used to maintain the minimum contact spacing to minimize the base series resistance. The high frequency performance of HBTs is also greatly enhanced by reducing the parasitic base-collector capacitance (C_{bc}). The parasitic base-collector capacitance consists of intrinsic device capacitance and extrinsic base-pad capacitance.

In this work, a novel self-alignment technique is proposed and investigated to minimize the base resistance in InP HBTs. Its device structure as well as the proposed fabrication method are described in section II. For C_{bc} reduction, a new base pad isolation technique and a novel lateral reverse-etching technique have been developed and the details are discussed in section III. At first, a method to isolate the base-pad from the intrinsic device structure, which has been proposed to reduce the extrinsic base-pad capacitance, is discussed. Another C_{bc} reduction method is also discussed, which is very

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effective in InP-based double HBTs (DHBTs) for minimizing the intrinsic device capacitance using a new lateral reverse-etching technique.

II. CDC Emitter-Base Self-Alignment Technology

Various self-alignment technologies have been reported to reduce the base resistance of HBTs using processing techniques, such as wet chemical etching using an emitter electrode mask in the conventional HBT process, a thick SiO_2 sidewall formation around the emitter electrode [6], overhang caused by the undercut of the sidewall [7], and T-shaped emitter electrode [8]. However, previously reported processing methods rely on inconsistent wet etching or reactive ion etching, resulting in problems such as excessive etching at the emitter mesa or plasma damage of the etched surface.

A novel self-alignment technique, namely crystallo-graphically defined emitter contact technology (CDC technology), has been proposed by the authors to minimize the base resistance [14]. The technique is based on the anisotropic wet etching characteristics of InP, which provide consistent crystallo-graphically etched facet. The angle of etched facet with respect to the (100) wafer plane was found to be an angle of 35° along the $[0\,1\,\bar{1}]$ crystal orientation, when the InP is etched with an HCl : H_3PO_4 wet solution. To utilize the above property, a dummy emitter on the top of the conventional InP-based HBT structure is used and the epitaxial layer structure is described in Table I.

Fig. 1 illustrates the brief fabrication sequence of the new self-alignment technique. The new self-aligned process begins with evaporation of Ti metal as an etching mask. After evaporation of Ti metal, photolithography is performed to define the emitter pattern of HBTs. The emitter finger should be aligned to the parallel direction of the primary flat to obtain the crystallo-graphically defined emitter electrode in the proposed self-aligned structure. After the emitter patterning, Ti metal is etched and then the InP dummy layer is etched with HCl : H_3PO_4. The planes with the smooth angle of about 35° along the $[0\,1\,\bar{1}]$ crystal orientation are formed due to the crystallo-graphic

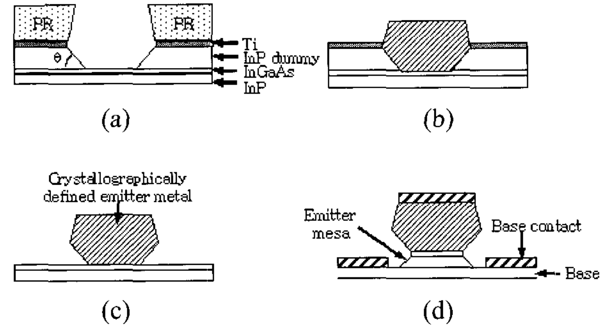


Fig. 1 A brief fabrication sequence of the proposed self-aligned contact process; (a) wet-etching of dummy emitter, (b) emitter metallization, (c) wet-etching of remained dummy emitter, and (d) emitter mesa etching & base metallization.

Table I Epitaxial layer structure for CDC Emitter-Base Self-alignment technology.

Layer	Material	Doping (cm^{-3})	Thickness (nm)
Dummy	**InP**	**Undoped**	**250**
Emitter cap	InGaAs	$n^+ = 2 \times 10^{19}$	100
Emitter cap	InP	$n^+ = 2 \times 10^{19}$	50
Emitter	InP	$n = 3 \times 10^{17}$	50
Spacer	InGaAs	Undoped	5
Base	InGaAs	$p^+ = 4 \times 10^{19}$	40

etching characteristics of the InP dummy layer [Fig. 1(a)]. Emitter metals of Ti/Pt/Au are then deposited on the InGaAs emitter cap layer. As show in Fig. 1(b), the emitter electrode is formed according to the crystallo-graphically etched side-wall shapes in the InP dummy emitter layer. In this step, the crystallo-graphically defined emitter electrode provides reliable contact spacing for the self-alignment, which can be adjusted by careful design of InP dummy thickness. The remained dummy emitter layer is removed by an HCl : H_3PO_4 mixture with a high etch-rate [Fig. 1(c)]. Then, emitter mesa etching for InGaAs and InP layers is carried out successively using H_3PO_4 : H_2O_2 : H_2O and HCl : H_3PO_4 without over-etching [Fig. 1(d)]. Fig. 2 shows SEM photograph of the fabricated crystallo-graphically defined emitter electrode. The contact spacing is designed to be 2800Å.

The new self-alignment technology provides a reliable self-alignment between the emitter and the base electrode without any over-etching of emitter mesa or damage-inducing dry etching techniques due to the

consistent crystallo-graphically defined shape of emitter electrode. In addition, the CDC technology is expected to be useful for fabricating sub-micron size emitter HBTs with conventional optical lithography by controlling the foot dimension of the emitter electrode through only adjusting the thickness of the InP dummy emitter layer.

III. C_{bc} Reduction Techniques For High Frequency Characteristics

A. *Base pad isolation technique*

Reduction of base-collector capacitance by minimizing the parasitic base pad-capacitance is found to be very effective especially for small size devices, since the portion of base pad does not usually scale down with the emitter size [9]. Several methods have been reported to minimize base pad-capacitance portion using techniques such as a plated micro air-bridge interconnect [10], double polyimide planarization process [11]. However, the first method is not suitable for small size devices since it should utilize the electro-plating process and the second technique can cause plasma damage by the reactive ion etching of the base pad region.

In this work, a method to isolate the base pad from the intrinsic device structure for reducing the extrinsic base-collector capacitance of InP/InGaAs Single HBTs (SHBTs) is reported, which uses a new base pad layout. The new layout allows more effective and easier base pad isolation for InP-based HBTs, which have the emitter aligned to $[0\,1\,1]$ or $[0\,1\,\bar{1}]$ directions, without excessive lateral or additional etching. The epitaxial layer of the InP/InGaAs SHBT used in this work was grown by MBE and the layer structure is summarized in Table II. The dopants were Si for n-type and C for p-type. The devices were fabricated using a conventional wet etching mesa process [5]. The emitter was aligned to $[0\,1\,1]$ direction. Ti/Pt/Au was evaporated for the emitter and collector metal. Pt/Ti/Pt/Au was used for self-aligned base metal. For passivation of the device, polyimide was used. The detailed fabrication sequence is described elsewhere [14].

The proposed method of base pad isolation is based on the different etch rates of InGaAs collector with the

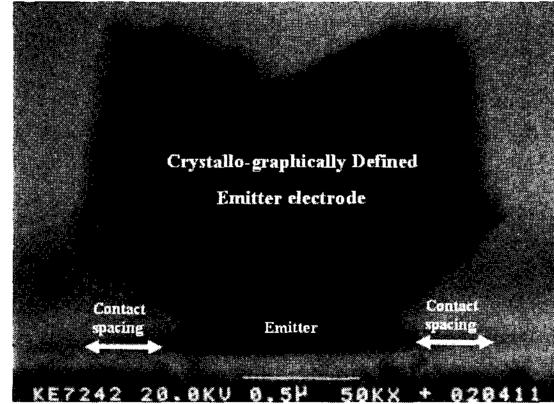


Fig. 2 SEM photograph of the fabricated crystallo-graphically defined emitter electrode. The contact spacing is designed to be 2800Å.

Table 2 Epitaxial layer structure of the SHBT.

Layer	Material	Doping(cm^{-3})	Thickness(nm)
Emitter cap	InGaAs	$n^+ = 2 \times 10^{19}$	80
Emitter cap	InP	$n^+ = 2 \times 10^{19}$	40
Emitter	InP	$n = 4 \times 10^{17}$	150
Spacer	InGaAs	Undoped	5
Base	InGaAs	$p^+ = 4 \times 10^{19}$	55
Collector	InGaAs	$n^- = 2 \times 10^{16}$	600
Etch-stop	InP	$n^+ = 2 \times 10^{19}$	10
Subcollector	InGaAs	$n^+ = 2 \times 10^{19}$	400
Buffer	InP	Undoped	100
Substrate	InP	S.I.	

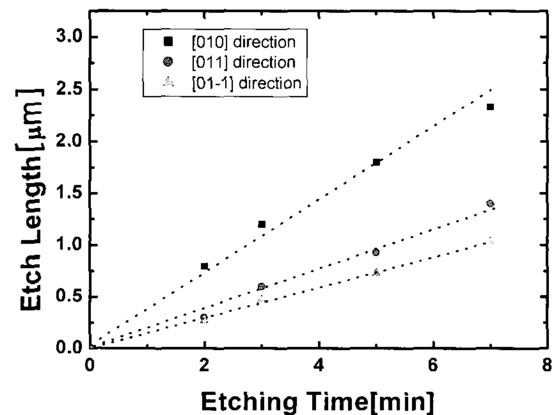


Fig. 3 Lateral etch length of the InGaAs base and collector depending on crystal orientations vs. etching time (Etchant = $H_3PO_4 : H_2O_2 : H_2O$).

crystal orientations. In order to investigate the etch rates depending on the crystal orientations, the lateral etching of the InGaAs base and collector layers was performed

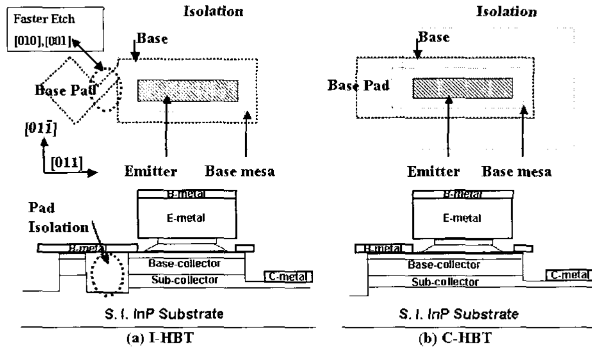


Fig. 4 Layout and schematic cross-section for (a) Proposed structure for C_{bc} reduction using the isolation technique (I-HBT) and (b) Conventional structure(C-HBT).

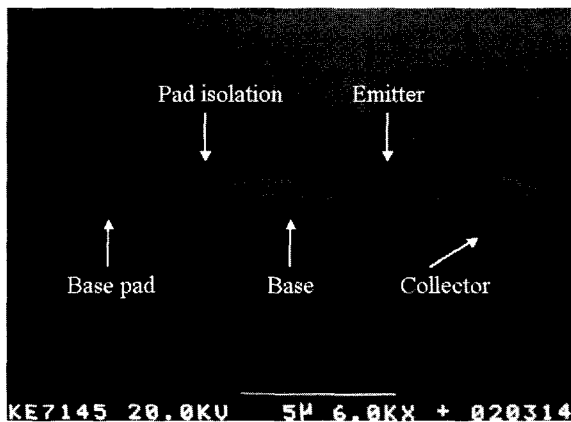


Fig 5 SEM picture of the fabricated I-HBT using the proposed isolation technique with a $2\times5\mu m^2$ emitter size before device passivation.

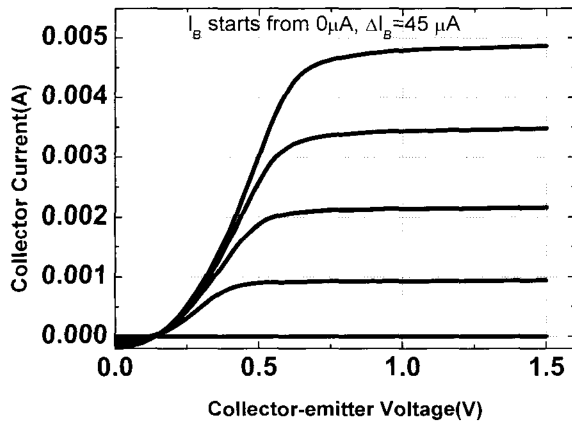


Fig 6 Common-emitter I-V characteristics of the fabricated I-HBT with a $2\times5\mu m^2$ emitter size.

with a wet etching solution. First, Ti metal was evaporated on the InGaAs base layer as an etch mask, which is aligned to [0 1 1] and [0 0 1] directions on the (100) wafer, respectively. Then the InGaAs collector layer was etched with an H_3PO_4:H_2O_2:H_2O (1:1:10) mixture. Fig. 3 shows lateral etch length of the InGaAs collector depending on the crystal orientations with etching time. It is observed that the etch rates of the InGaAs in the [0 1 0] and [0 0 1] directions are much higher than that in the [0 1 1] and [0 1 $\bar{1}$] directions. The etch rates were measured around 55.2Å/sec, 33.5 Å/sec and 24.6 Å/sec in the [0 1 0] , [0 1 1] and [0 1 $\bar{1}$] directions, respectively.

The proposed base pad layout and base pad isolation technique are illustrated in Fig. 4. The new base pad is designed to be connected to the base with a bridge-like narrow feeding [Fig. 4(a)] for the pad isolation, while the base pad of the conventional structure [Fig. 4(b)] is simply extended from the base of the intrinsic device region. In addition, the base feeding and the base pad are designed to be rotated by an angle of 45° with respect to the emitter finger, which is aligned to [0 1 1] or [0 1 $\bar{1}$] directions. The size of the base pad is set by the minimum size of the interconnect via hole. In order to avoid reliability problems related to the narrow width of the feeding, larger width of the feeding is desirable. However, for the pad isolation, the feeding width should be shorter than the twice of the lateral etch length during the mesa etching of the collector, otherwise excessive lateral or additional etching may be required. It means that the feeding, which is aligned to the crystal orientations with higher etch rates, provides more effective pad isolation even though the feeding with larger width is used. From above consideration, the base feeding and the base pad are designed to be rotated by 45°(aligned to the [0 1 0] or [0 0 1] direction). This new base pad design utilizes previously mentioned high etch rates of the InGaAs layer in the [0 1 0] or [0 0 1] direction. These results in not only efficient base pad isolation but also significant lateral etching of the base pad portion of the extrinsic InGaAs B-C junction during collector mesa etching without excessive lateral or additional etching. Fig. 5 shows the SEM picture of the isolated structure using the proposed technique before device mesa etching and polyimide passivation.

The devices were fabricated simultaneously on the same wafer using the proposed base pad isolation technique (I-HBT) and the conventional method (C-

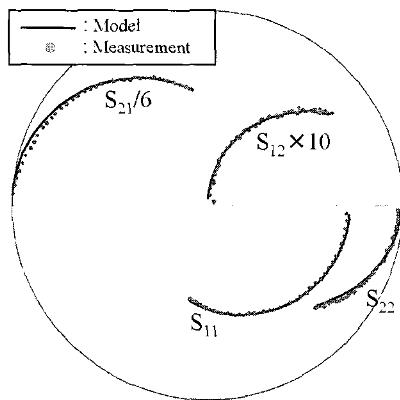


Fig 7 Modeled (-) and measured (•) S-parameters of the fabricated I-HBT.(V_{CE}=1.75V,I_C=9.85 mA).

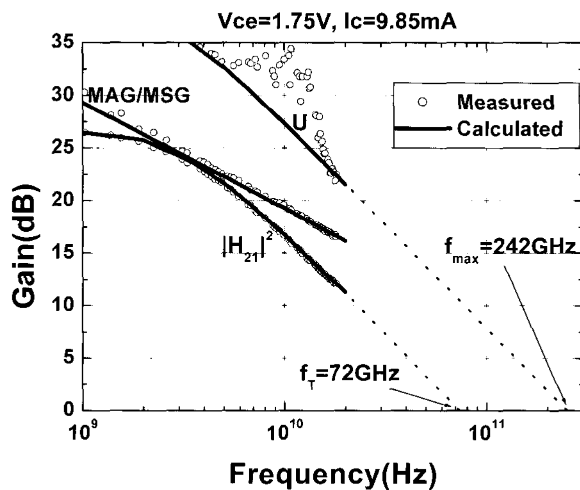


Fig 8 Measured and calculated gain characteristics of the fabricated I-HBT with a 2×10 μm² emitter size.

HBT). The two devices showed similar overall DC characteristics. The common-emitter characteristics of the I-HBT are shown in Fig. 6. The offset voltage $V_{CE,offset}$ was 0.15V and the collector-emitter breakdown voltage BV_{CEO} was 5.7V. The DC current gain h_{FE} of 19 was obtained with the ideality factors of n_C = 1.05 and n_B = 1.34. The frequency response of the I-HBT was measured on-wafer from 0.5GHz to 18GHz using a 8720C Network Analyzer. The S-parameter fitting and parameter extraction were performed to estimate the accurate frequency characteristics of the fabricated device at higher frequencies using a small signal model based on the measured data [15-16]. The results of the S-parameter fitting are shown in Fig. 7, which show excellent agreement between measured and calculated

Table 3 Extracted values of small signal parameters of the fabricated I-HBT with a 2× 10 μm² emitter size (V_{CE} = 1.75 V and I_C = 9.85 mA).

R_E (Ω)	R_b (Ω)	R_C (Ω)	R_{BE} (Ω)	R_{BC} (kΩ)	C_{BE} (fF)	C_{bc} (fF)	α_0	$\tau_B + \tau_C$ (ps)
10.2	6.9	7.92	3.23	550	220	7.2	0.959	1.2

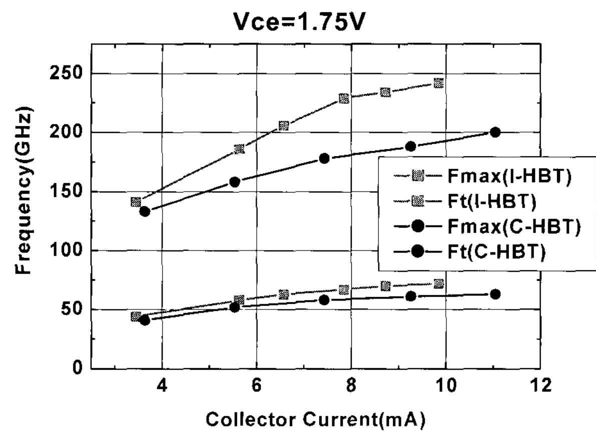


Fig 9 f_T, f_{max} vs. collector current of the fabricated SHBTs with a 2×10 μm² emitter size, biased at V_{CE}=1.75V; (■): Proposed structure HBT(I-HBT), (•): Conventional structure HBT(C-HBT).

data. Fig. 8 shows measured and calculated unilateral power gain (U), current gain (h_{21}) and maximum available gain (MSG/MAG) for the fabricated I-HBT with a 2x10 μm² emitter size. The peak f_T and f_{max}, estimated from -20dB/decade extrapolation, were found to be 72 and 242 GHz, respectively.

From the measured S-parameters of the I-HBT, the small-signal parameter values were extracted and optimized based on an HBT equivalent circuit model [15]. The extracted values of the key parameters are listed in Table III. The extracted values of the base resistance (R_b) and base-collector capacitance (C_{bc}) were found to be 6.9Ω and 7.2fF, respectively. The effective R_bC_{bc} time delay, calculated from the extracted values, agrees with the measured f_{max} of 242GHz. The high frequency characteristics of the fabricated I-HBT and C-HBT were compared to investigate the effects of the base pad isolation. Both devices have almost the same layout designs except for the shape of base pad as shown in Fig. 4. The measured f_T and f_{max} of the devices as a function of the collector current are shown and compared in Fig. 9. The I-HBT shows 20% improvement of the peak

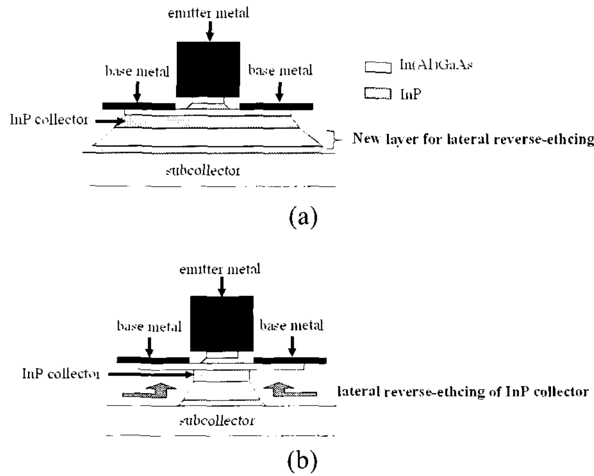


Fig 10 Schematic cross-section for (a) conventional DHBT structure (C-DHBT) and (b) optimized DHBT structure for C_{bc} reduction using the proposed lateral reverse-etching technique (R-DHBT).

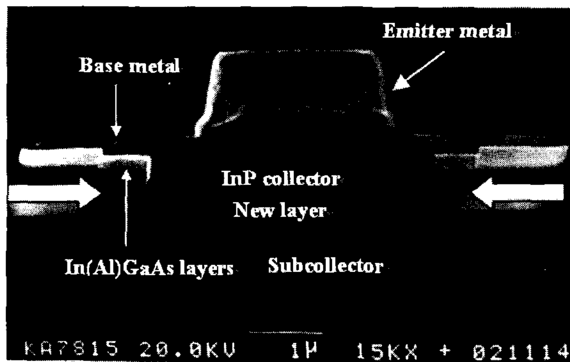


Fig 11 SEM photograph of the fabricated R-DHBT using the lateral reverse-etching technique with an emitter size of 2×10 μm^2.

f_{max}(198GHz→242GHz). The effective R_bC_{bc} products for the I-HBT and C-HBT, estimated from the relationship of $f_{max}=[f_T/(8\pi R_bC_{bc})]^{1/2}$, were found to be 49fs and 67fs, respectively. A 27% decrease in R_bC_{bc}(67fs→49fs) is directly attributed to the associated decrease in the parasitic C_{bc} component of the base pad region.

B. *Enhancement of cut-off frequency using lateral reverse-etching of BC-junction*

To reduce the intrinsic device capacitance, lateral etching of BC-junction was performed using an InP-based double HBT (DHBT) technology. The InP-based

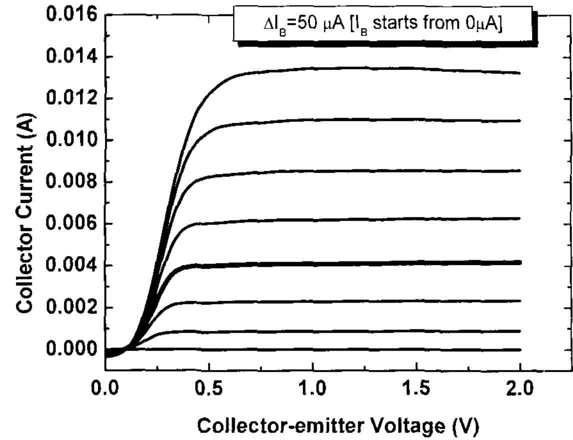
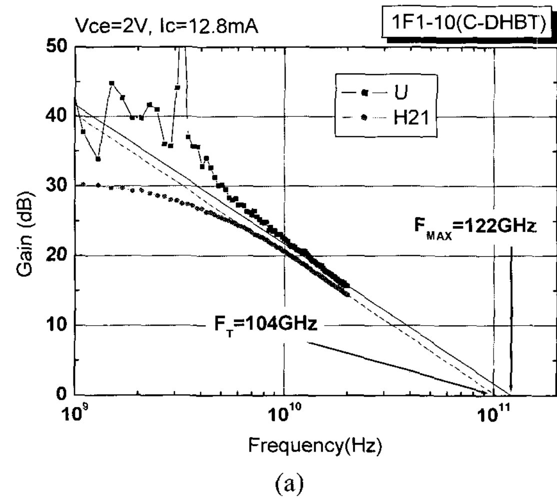


Fig 12 Common-emitter I-V characteristics of the fabricated R-HBT with an emitter size of 1×10μm^2.



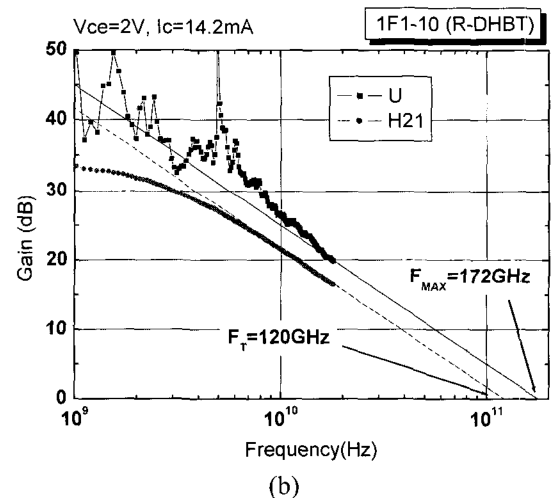


Fig 13 Measured gain-frequency characteristics of the fabricated devices with an emitter size of 1×10 μm^2 : (a) C-DHBT and (b) R-DHBT.

DHBT technology is very attractive for high-power applications even at high frequency range due to low impact ionization of the InP collector [2]. The effect of C_{bc} is considered more important in the DHBTs in achieving high cut-off frequencies than in the SHBTs, since a relatively short InP collector is generally employed in the DHBT technology to achieve high current gain cut-off frequency (f_T) while maintaining the same breakdown voltage [12]. Therefore, techniques of the C_{bc} reduction have been widely investigated in InP DHBTs. Among them, techniques relying on a laterally etched collector process to reduce C_{bc} have been widely used in InP DHBTs because of its easy lateral etching control due to the excellent selective wet etching property between the InP and the InGaAs materials [12-13].

In order to investigate the effects of C_{bc} reduction by lateral etching of the collector layer, two devices with the same emitter dimension were fabricated using the conventional method (C-DHBT) [Fig. 10(a)] and a proposed new lateral reverse-etching technique (R-DHBT) [Fig. 10(b)].

The layer structure of the DHBT is based on the conventional DHBT structure. Two new layers were added in the DHBT layer design between the 3000Å thick n^- InP collector and the n^+ InGaAs subcollector for the proposed lateral reverse-etching. The details of the layer structure and the new lateral reverse-etching technique are described in elsewhere [17]. The overall fabrication sequence of the DHBTs is similar to that of the SHBTs described in section III. Fig. 11 shows the SEM photograph of the fabricated HBT using the lateral reverse-etching technique. Both the C-HBT and R-HBT showed almost the same DC characteristics. The common-emitter DC characteristics of the fabricated R-HBT with an emitter size of $1\times10\mu m^2$ are shown in Fig. 12. The offset voltage $V_{CE,offset}$ and the collector-emitter breakdown voltage BV_{CEO} were 0.1V and 8.5V, respectively. The measured DC current gain is 48. The frequency response of the devices was measured on-wafer from 0.5GHz to 20GHz using a 8720C Network Analyzer. The microwave characteristics of the C-DHBT and R-DHBT with an emitter size of $1\times10\mu m^2$ are shown in Fig. 13. In the case of the C-DHBT, the peak f_T and f_{max}, estimated from -20dB/decade extrapolation, were found to be 104 GHz and 122 GHz, respectively

Table 4 Extracted values of small signal parameters from the fabricated C-DHBT and R-DHBT with an emitter size of $1\times 10\ \mu m^2$ (V_{CE} = 2.0 V).

	Peak f_{max} (GHz)	Peak f_T (GHz)	$C_{bc,i}$ (fF)	R_b (Ω)	R_E (Ω)	R_{BE} (Ω)	R_C (Ω)	C_{BE} (fF)
C-DHBT	122	104	**11.7**	18.5	5.3	2.1	1.5	80
R-DHBT	**172**	**120**	**4.43**	22.3	5.35	1.98	3.34	80

[Fig. 13(a)]. The R-DHBT showed slightly increased peak f_T of 120 GHz and greatly improved f_{max} of 172 GHz [Fig. 13(b)]. Small signal parameter extraction [15-16] from the measured S-parameter data was performed to verify the results. The extracted values of key parameters are summarized in Table IV. The C_{bc} values of the C-DHBT and R-DHBT were extracted to be 11.7fF and 4.43fF, respectively. The reduction of C_{bc} estimated from the extracted values agrees well with the physical structures of the device. From the above results, it is demonstrated that the proposed new lateral etching of the BC-junction results in an impressive improvement (43% increase) of f_{max} in the DHBT by significant reduction of C_{bc} reduction.

IV. CONCLUSIONS

In this work, process optimization techniques for high frequency performance of HBTs have been presented. Several techniques proposed for effective reduction of the base resistance and the base-collector capacitance have been investigated.

First, a new self-alignment technique (CDC technology) has been investigated, which was proposed to reduce the base resistance. Reproducible self-alignment of emitter-base electrodes was achieved without any over-etching or dry etching process of the emitter mesa, while maintaining minimum contact spacing between the emitter junction and the base electrode. The proposed self-alignment technique is also expected to be very promising for fabricating submicron size emitter HBTs using only the conventional optical lithography. Secondly, a new base pad isolation method for minimizing the extrinsic base pad-capacitance was proposed and demonstrated. The new method allows

more effective and easier base pad isolation for the InP-based SHBTs without excessive lateral or additional etching. This technique is also believed to be very effective for the base pad isolation in fabricating double HBTs with an InP collector. Finally, to reduce the intrinsic device capacitance, a new lateral reverse-etching technique was proposed, which can significantly enhance the f_{max} of InP-based DHBTs. The greatly improved f_{max} values obtained using the new technique verifies the validity of the proposed technique.

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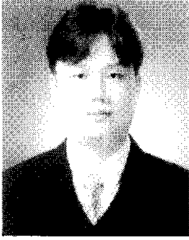

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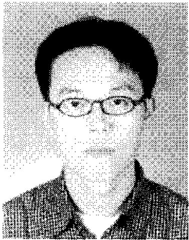

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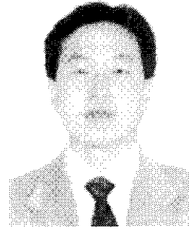

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