40nm InGaAs HEMT's with 65% Strained Channel Fabricated with Damage-Free SiO_2/SiN_x Side-wall Gate Process

Dae-Hyun Kim, Suk-Jin Kim, Young-Ho Kim, Sung-Wong Kim, and Kwang-Seok Seo

Abstract—**Highly reproducible side-wall process for the fabrication of the fine gate length as small as 40nm was developed. This process was utilized to fabricate 40nm InGaAs HEMTs with the 65% strained channel. With the usage of the dual SiO_2 and SiN_x dielectric layers and the proper selection of the etching gas, the final gate length (Lg) was insensitive to the process conditions such as the dielectric over-etching time. From the microwave measurement up to 40GHz, extrapolated fT and fmax as high as 371 and 345 GHz were obtained, respectively. We believe that the developed side-wall process would be directly applicable to finer gate fabrication, if the initial line length is lessened below the 100nm range.**

Index Terms—**InP, HEMT, InGaAs/InAlAs, nano-scale, side-wall, current-gain cutoff frequency (fT)**

I. Introduction

An InGaAs/InAlAs HEMT's on InP substrate has shown the excellent frequency characteristics due to the enhanced electron's mobility and the increased conduction band discontinuity (ΔE_c) [1][2][3]. Recently, the device microwave characteristics have been improved by reducing the gate length (L_g) to nano-meter scale and adapting the highly strained In_XGaAs channel (x>0.53) [4][5]. According to the Fusitzu group's work [6], f_T of 396GHz with L_g of 25nm and the strained $In_{0.7}GaAs$ channel was reported.

Conventional e-beam lithography machine with an acceleration voltage of 30 kV and a Tunsten (W) filament would offer to the range of about 100nm. To reduce the device gate length (L_g) to the sub-100nm scale, the state of the art e-beam lithography machines with high resolution will be needed. The side-wall process has been widely used to resolve these lithography limitations, especially in CMOS device fabrications [7]. The fine pattern is obtained through the formation of the side-wall spacer which results from the sequence of dielectric etch, dielectric re-deposition and dielectric etch-back. Among the various process parameters, a percentage of over-etch in the etch-back step affects mainly to the shape of the final side-wall spacer. Due to the step coverage problem in the dielectric re-deposition, the exact control of the over-etch time is really impossible, and thus the ambiguity of the shape of the final side-wall spacer would be problematic in this process.

In this paper, highly reproducible side-wall gate process was developed. The ambiguity of the shape for the final side-wall spacer was resolved through the use of SiN_x/SiO_2 dual dielectrics and the proper selection of etching gas. The 40nm side-wall gate InAlAs/InGaAs/InP HEMT's on InP substrate with the strained $In_{0.65}GaAs$ channel was fabricated and the device showed $G_{m,max}$, f_T, and f_{max} of 1.7 S/mm, 371 GHz and 345 GHz.

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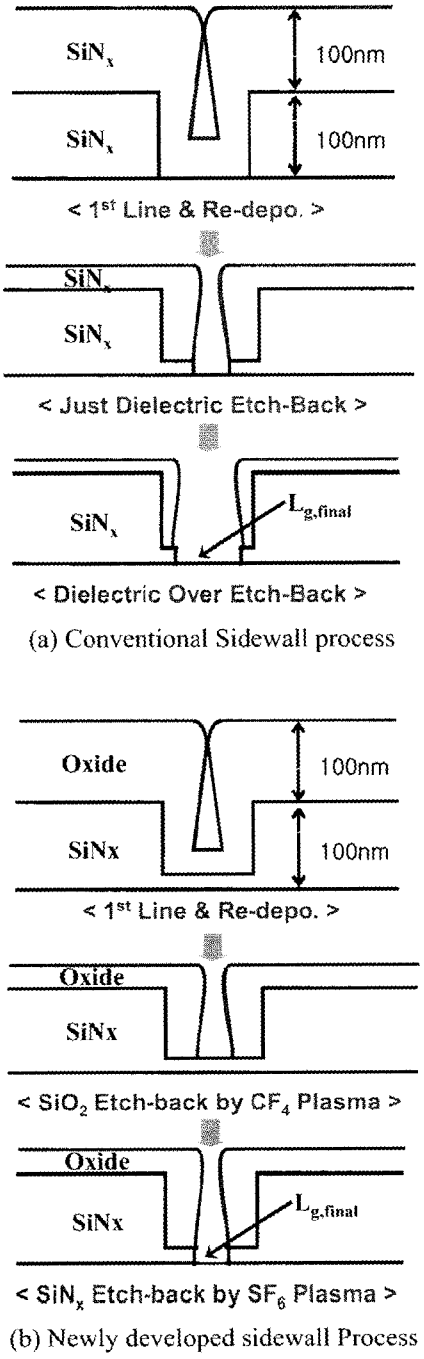


Fig1 Procedure of Sidewall process.

II. A Novel SiN_x/SiO_2 Side-Wall Gate Process

Figure 1-(a) shows the procedure of a conventional side-wall gate process which includes first line definition, dielectric re-deposition and dielectric etch-back. The final gate length (L_g) is lessened by the dimension of the two side-wall spacers. Because the shape of the final side-wall spacer is easily changed by a time of dielectric etch-back, the fine control of the final gate length (L_g) is very difficult.

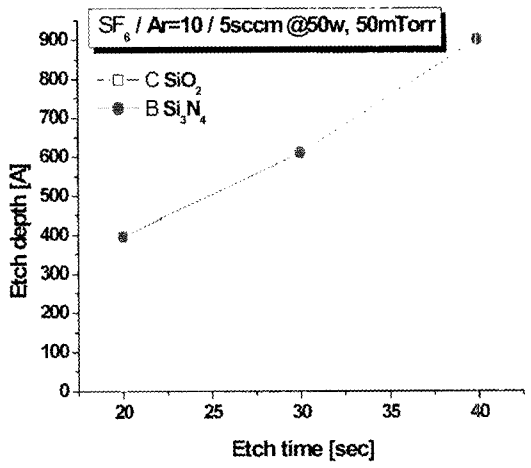
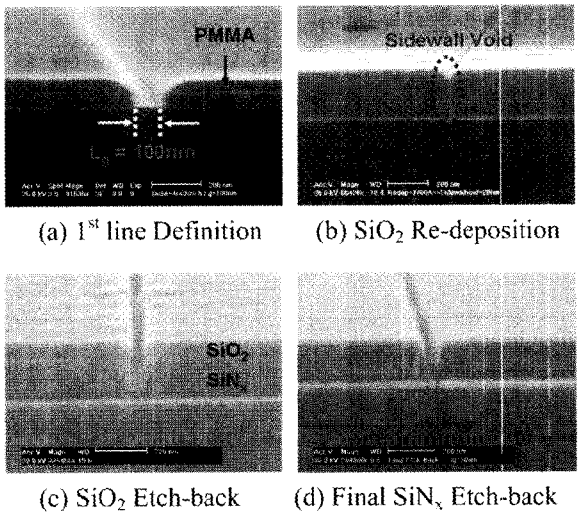


Fig 2 SiO_2 and SiN_x etch results by SF_6 based plasma.



(a) 1st line Definition (b) SiO_2 Re-deposition

(c) SiO_2 Etch-back (d) Final SiN_x Etch-back

Fig 3 The over-all SEM Photograph of Sidewall process

Figure 1-(b) represents the newly developed side-wall process, which utilizes two dielectric layers of SiN_x and SiO_2, and two plasma gas sources for the purpose of the dielectric dry etch. After the re-deposited SiO_2 was etched by the CF_4 based plasma, the residual SiN_x was etched by the SF_6 based plasma. Figure 2 shows typical etch characteristics for PECVD grown SiO_2 and SiN_x by SF_6 based plasma. Here, the SF_6 based plasma has a high etch selectivity for the SiO_2 layer, which prevents the shape of the final side-wall spacer from being lessened during over-etch. This feature does ensure the reproducibility of the proposed side-wall gate process.

The actual etch selectivity for the oxide layer by the SF_6 plasma was over 20 in this process.

Figure 3 shows the over-all SEM photograph of the proposed side-wall gate process in detail. The final gate length after the etch-back step was 40nm. In addition, the SF_6 gas has an advantage of low plasma-induced damage during the etch process, which can offer enough over-etch time without any degradation of the carrier transport property.

III. 40nm InGaAs HEMTs Using Sidewall Process

Pseudomorphic InGaAs/InAlAs HEMT epitaxial layers with InP etch-stopper were grown by solid-source molecular beam epitaxy on 3 inch semi-insulating InP substrate. The detailed structures are shown in fig. 4. A 10nm strained $In_{0.65}GaAs$ channel was adopted to enhance the carrier transport property, and a 4nm undoped InP layer acts as an etch-stopper for gate recess process. The results of Hall measurement indicated a 2-DEG (Two Dimensional Electron Gas) density of 3×10^{12} /cm^2 with a low field Hall mobility of 10,300 cm^2/V-sec at room temperature.

Device fabrication begined with mesa isolation down to the InAlAs buffer layer by wet chemical etching using a H_3PO_4 : H_2O_2 : H_2O mixture. For the S/D ohmic contact, an image reversal photo-resist was used to achieve a well-defined over-hang profile for a lift-off, and they were formed by Ni/Ge/Au metallization through e-beam evaporation and alloyed in H_2 ambient after the R-PECVD (Remote PECVD) grown 100 nm SiN_x pre-passivation. Figure 5 shows the optimization results of S/D ohmic contact for various metal systems. The ohmic metal system of Ni/Ge/Au(10/45/160nm) lowered drastically the contact resistance (R_c) below 0.035Ω-mm, which is acceptable for the sub-100nm gate device. The developed SiN_x/SiO_2 side-wall process was applied to define 40nm gate foot, and then selective gate recess etching using a citric acid and H_2O_2 mixture was done. The sputtered Tusten (W) metal was used effectively to fill a fine gate foot line with high aspect ratio. Second T-gate of 0.2μm was defined with PMMA/P(MMA-MAA)/PMMA tri-layer resist system to improve lift-off well, and the schottky gate of Ti/Au

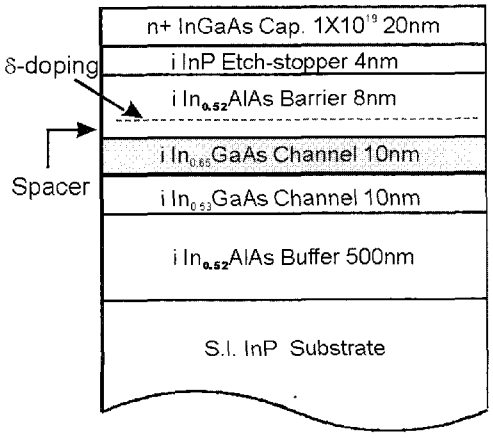


Fig 4 Cross-section of the InGaAs/InAlAs HEMT's.

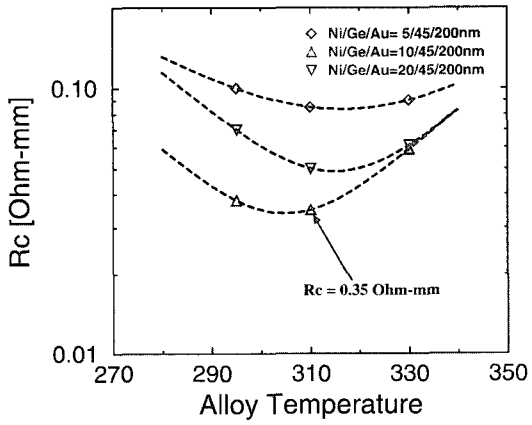


Fig 5 Contact resistance (R_c) versus the alloy temperature for the various Ni/Ge/Au structures.

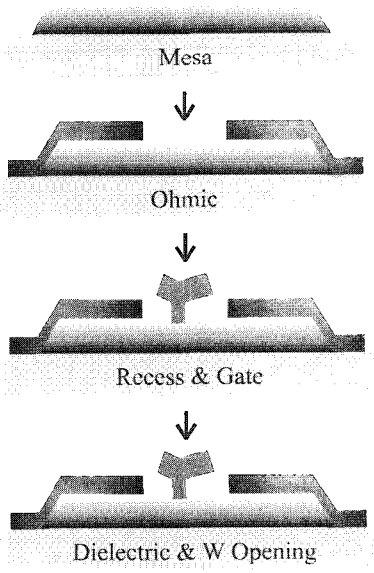


Fig 6 The over-all HEMT fabrication procedures.

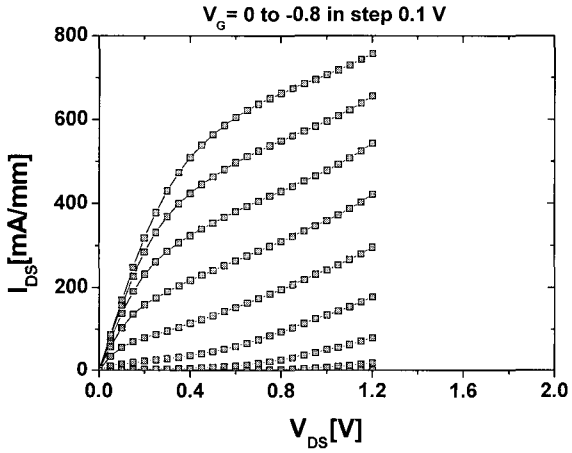
(50/350nm) was evaporated. The overall device fabrication procedures were summarized in fig. 6. [8]

III. DC AND MICROWAVE CHACTERISTICS

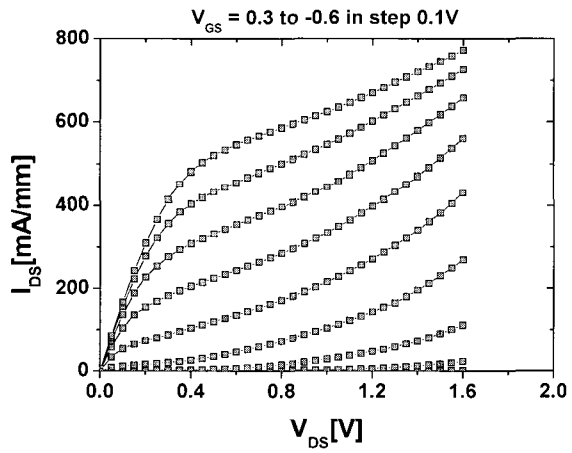
Two types of 40nm InGaAs HEMT devices were fabricated. One is an InP-schottky barrier device and the other is an InAlAs-schottky barrier device by means of Ar plasma RIE etch. The fabricated 40 nm HEMT's were characterized through on-wafer measurement for DC and microwave performance. The output I-V transfer curves for two types were plotted in fig. 7. The 40nm HEMT's with InP schottky barrier exhibit V_{th} of -0.6V and $G_{m.max}$ of 1.6S/mm. The 40nm HEMT's with InAlAs schottky barrier show somewhat higher $G_{m.max}$ of 1.7S/mm and lower V_{th} of -0.45V due to the etching of InP etch-stopper by Ar plasma.

Figure 8 shows the results of reverse and forward schottky-gate characteristics for two types. Because InP layer has a low schottky barrier height (SBH) of about + 0.35eV compared with $In_{0.52}AlAs$ layer with SBH of about + 0.6 eV, the similar behavior in the off-state breakdown characteristics was seen. These also explain an increase of forward turn-on voltage for an InAlAs schottky device.

The small signal scattering parameters (S-parameters) of 2×50μm InGaAs HEMT's were measured using on-wafer probing and 8510C network analyzer (1~40GHz). Shown in fig. 8 were the plots of H_{21} and unilateral gain



(a) I-V Transfer Curve for InP schottky HEMT



(b) I-V Transfer Curve for InAlAs schottky HEMT

Fig 7 Typcial DC transfer curve I-V characteristics of the 40nm InGaAs HEMT's. A device with InAlAs schottky barrier show that drain operating region would be more increased than that with InP schottky barrier.

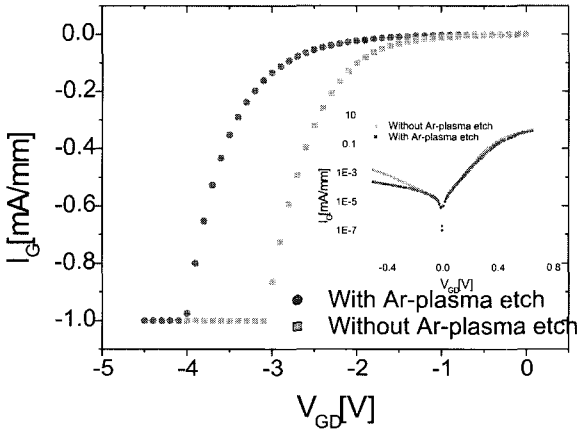


Fig 8 The Schottky Gate Characteristics. A device with InAlAs schottky shows BV_{GD} of – 4.0V and gate turn-on voltage (V_{on}) of + 0.45V.

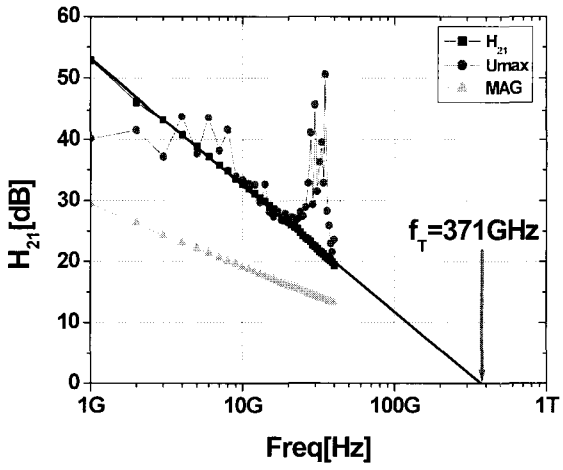


Fig 9 Current gain H_{21} and Unilateral power gain (U_{max}) versus measured frequency for the 40nm InGaAs HEMT's biased near the peak transconductance ($G_{m.max}$)

(U_{max}) versus the frequency biased near peak $G_{m.max}$ region. Extrapolating H_{21} and U_{max} to zero gain with -6 dB/octave slopes, an estimation of 371 GHz and 345 GHz were made to f_T and f_{max}. We believe that these results to be one of the excellent sub-100nm InGaAs HEMT's with a little short channel effect.

IV. Conclusion

We have presented a highly reproducible and damage-free technology for the formation of 40nm T-gate structure. The fine gate foot with reproducibility could be defined by the usage of the dual SiN_x and SiO_x dielectric layers and proper selection of the etching gas. Finally, we have used the developed side-wall process to fabricate 40nm gate-length InGaAs HEMT's with the 65% strained channel, which showed $G_{m.max}$ of 1.7 S/mm, f_T of 371 GHz, and f_{max} of 345 GHz. This highly reproducible and damage-free side-wall technology will be directly applicable to finer gate foot definition, if the first line length is lessened below 100nm scale.

Acknowledgments

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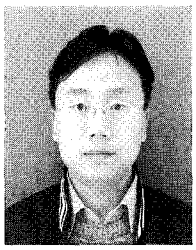

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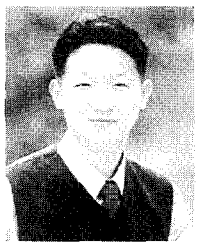

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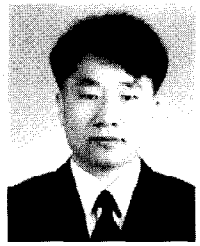

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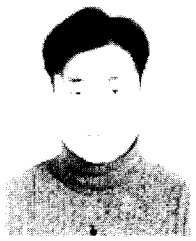

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