JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.3, NO. 1, MARCH, 2003

Analysis of Electrical Properties of Ti/Pt/Au Schottky Contacts on (n)GaAs Formed by Electron Beam Deposition and RF Sputtering

B K Sehgal, V R Balakrishnan, R Gulati, and S P Tewari

Abstract—**This paper describes a study on the abnormal behavior of the electrical characteristics of the (n)GaAs/Ti/Pt/Au Schottky contacts prepared by the two techniques of electron beam deposition and rf sputtering and after an annealing treatment. The samples were characterized by I-V and C-V measurements carried out over the temperature range of 150 – 350 K both in the as prepared state and after a 300 C, 30 min. anneal step. The variation of ideality factor with forward bias, the variation of ideality factor and barrier height with temperature and the difference between the capacitance barrier and current barrier show the presence of a thin interfacial oxide layer along with barrier height inhomogenieties at the metal/semiconductor interface. This barrier height inhomogeneity model also explains the lower barrier height for the sputtered samples to be due to the presence of low barrier height patches produced because of high plasma energy. After the annealing step the contacts prepared by electron beam have the highest typical current barrier height of 0.85 eV and capacitance barrier height of 0.86 eV whereas those prepared by sputtering (at the highest power studied) have the lowest typical current barrier height of 0.67 eV and capacitance barrier height of 0.78 eV.**

Index Terms— **Schottky contact, MESFET, Barrier height inhomogeneity, temperature variation**

Manuscript received February 13, 2003; revised March 4, 2003.
B K Sehgal, V R Balakrishnan and R Gulati are with Solid State Physics Laboratory, Lucknow Road, Delhi 110054, India
SP Tewari in place of Department of Physics, University of Delhi, Delhi 110007, India
E-mail : bk_sehgal/sspl@ssplnet.org

I. INTRODUCTION

The fabrication of high performance and reliable GaAs devices like metal-semiconductor field effect stransistor (MESFET), high electron mobility transistor (HEMT) and Schottky barrier diode require deposition of multilayer metal systems like Ti/Pt/Au, Pt/Au, Ti/Pd/Au, Cr/Pt/Au, Ti/W, WN, WBN and WSi as Schottky contacts on GaAs [1-8] (The first metal listed is the Schottky barrier metal in each case). Depending on the metallization system required and application, different techniques like sputter deposition or electron beam evaporation are generally employed to form these Schottky contact. Several studies [4-10] on the electrical properties of the Schottky metal contact indicate that they are closely linked to the technique of metallization. The reason for this is that metallization induced defects can significantly influence the Schottky barrier and near surface semiconductor properties. It is necessary to understand the electrical activity of these defects and find ways to control them. The defects can act as generation-recombination centers [6-9] and may generate local regions of electric fields and donor like defects in the semiconductor [7-10,14,15]. There are other competing processes like Fermi level pinning [12,29,32], presence of interfacial oxide layer [16,17] and barrier height inhomogeneities [18-23] causing non-ideal Schottky diode characteristics.

In the present work a detailed study of the effect of Schottky metallization technique on the electrical characteristics of the contact has been carried out. Ti/Pt/Au Schottky contacts were formed on (n)GaAs by

two different techniques viz.: magnetron RF sputtering at different power densities and electron beam evaporation. The I-V (T) and C-V (T) characteristics were investigated over the temperature range 150-350 K both before and after a sample annealing step. The abnormal dependence of ideality factor, η and Schottky barrier height on measurement temperature is analyzed in the framework of different models to understand the dominating current transport processes and the mechanism of Schottky barrier formation.

II. Sample Preparation And Electrical Measurements

The Schottky barrier diodes used in this study were fabricated on (100) oriented (n)GaAs wafers, uniformly doped with Si with the carrier concentration of $\sim 1 \mathrm{x} 10^{17}/\mathrm{cm}^3$. Ohmic contacts were formed by thermal evaporation of AuGe/Ni/Au on back side of the wafer. Immediately prior to Schottky metal deposition the GaAs wafers were etched first in H_2SO_4: H_20_2: H_20::1:1:100 for 3 min. followed by a native oxide etch in 50% HCl solution. The first etch removes about 1200 A of top GaAs layers. This step not only ensures a fresh surface of GaAs on which contacts are formed but also simulates the gate recess process, which is an integral part of MESFET fabrication. Circular shaped Ti/Pt/Au (300/300/2000) Schottky contacts were deposited on the front side of the wafer through a metallic contact mask. The contacts were formed by the two most prevalent techniques for gate metal deposition viz. magnetron rf sputtering at different power densities and electron beam evaporation. Three samples (named RF1, RF2, RF3) were prepared by rf sputtering at power densities of 1.25, 2.5 and 4 W/cm^2. One sample named EB was prepared by electron beam evaporation. The Schottky contact area for EB sample is 0.28 mm^2 and for the RF samples is 0.48 mm^2.

The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the contacts were measured at various temperatures in the range 150-350 K using a computer controlled system which includes a Keithley 428 current amplifier, 4140B voltage source, Boonton capacitance meter and a liquid nitrogen cryostat. The total series resistance of the experimental setup including the probe was $< 1\ \Omega$, which can be neglected. The C-V measurements were carried out with a test signal of 1 MHz frequency and 15 mV amplitude in the temperature range 150-350 K. After the measurements the samples were annealed in a furnace for 30 min. at 300 C in N_2 environment and the measurements were repeated.

III. Results On The Ideality Factor And Barrier Height

The measured semi-log forward I-V (T) characteristics for all the samples are linear over several orders of magnitude of current. There is three order of magnitude increase in the current for the case of RF3 sample in comparison to EB sample. In GaAs doped to $N_d \sim 10^{17}$ cm^{-3} and at room temperature the thermionic emission is the dominant current transport mechanism. For forward bias $V > (3kT/q)$, the zero bias barrier height, ϕ^{I-V}_{bo} and the ideality factor, η are given by [9-11]:

$$\eta = \left[\frac{q}{kT}\right] \left[\frac{1}{\partial(\ln I_f)\partial V_f}\right] \quad (1)$$

$$\phi^{I-V}{}_{bo} = \frac{kT}{q} \left[\ln A^{**} + \ln A + \ln T^2 - \ln I_s\right] + \Delta\phi_{bi} \quad (2)$$

where $A^{**} = 8.4$ A cm^{-2} K^{-2} is the effective Richardson constant, A is the contact area, I_s is the saturation current determined from the forward I-V curves at zero volt and $\Delta\phi_{bi}$ is the image force correction calculated to be 0.04 eV for the n-type contacts used [9,24]. The other symbols have their usual meaning.

Figs. 1(a)–(d) show the calculated ideality factor vs forward voltage at various temperatures for the four samples EB, RF1, RF2 and RF3. For sample EB, η is nearly unity at room temperature upto ~0.4 volts applied bias. As the temperature is lowered to 200 K, the ideality factor increases slowly. Further lowering of temperature to 150 K results in rapid increase in the value of η. The ideality factor also increases at lower forward bias and the increase is very steep below 200 K temperature. Similar behavior is observed for the RF1 sample fabricated at the lowest rf power of 1.25 W/cm^2. The increase in the ideality factor at higher forward bias is observed for all the samples and is because of the

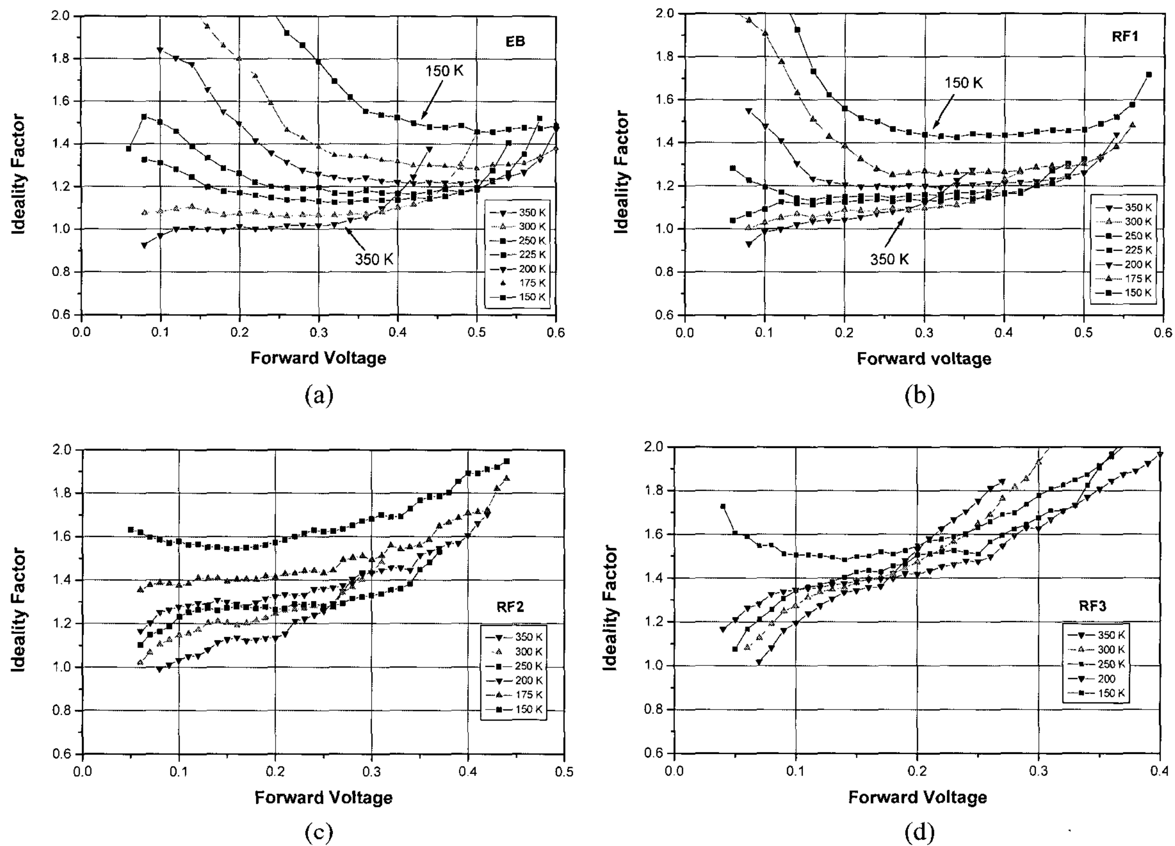


Fig. 1 Ideality factor η vs. forward voltage corresponding to the I-V (T) characteristics of (a) EB sample prepared by electron beam deposition, (b) RF1 sample prepared by rf sputtering at power density of 1.25 W/cm^2, (c) RF2 sample prepared by rf sputtering at power density of 2.5 W/cm^2, (d) RF3 sample prepared by rf sputtering at power density of 4 W/cm^2

voltage drop across the series resistance of the devices.

The η-V_f (T) characteristics at lower forward bias (<0.2 volts) and lower temperature (<200 K) is markedly different for the RF2 and RF3 samples (Figs. 1(c) and 1(d)). The increase in the η value at lower bias is not seen and it remains pinned to about 1.6 even for 150 K and very low bias values (0.06 volt). The room temperature η values deteriorate as the rf deposition power is gradually increased in the samples RF2 and RF3. The values of the ideality factor extracted from the flat portions of the η-V_f (T) curves have been plotted in Fig. 2 as a function of temperature. It is seen that the ideality factor increases with decreasing temperature.

The zero bias current barrier height, ϕ^{IV}_{bo} calculated from the forward I-V curves (including the image force correction) is plotted as a function of temperature in Fig. 3. It is seen that the room temperature (300 K) current barrier height of the Schottky contacts decreases in the order EB > RF1 > RF2 > RF3. Several investigations have ascribed the lower barrier height of sputter deposited contacts on n type semiconductors to the introduction of donor like defects in the semiconductor during sputter deposition [4,14,15]. As the temperature is lowered the barrier height, ϕ^{IV}_{bo}, of all the samples decreases.

The barrier height of a Schottky diode depends on the electric field across the contact and consequently on the applied bias. In order to compare different Schottky contacts it is necessary to specify standard field conditions. It has been shown previously that the flat band barrier height, ϕ^{f}_{b} is the fundamental barrier height, which should be used when comparing experiments with theory [12,13]. From theoretical considerations and from experiments it can be concluded that the flat band barrier

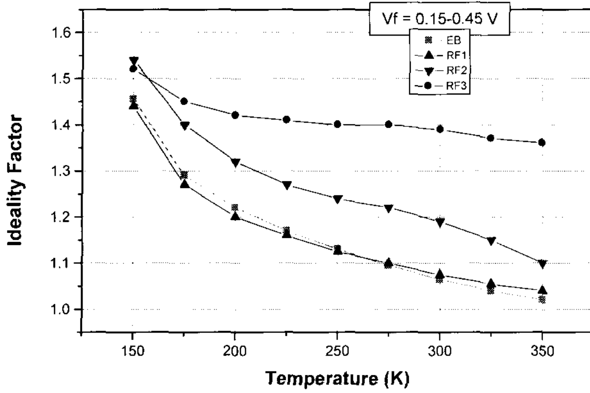


Fig. 2 Temperature dependence of the ideality factor, η for the four samples. The ideality factor values are extracted from Fig. 1 (a-d) and are the values calculated in the bias range 0.15-0.45 volt.

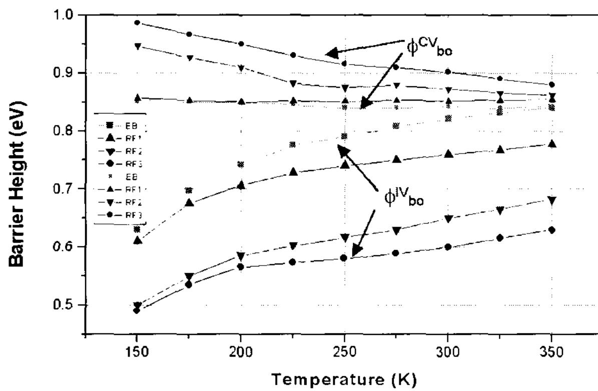


Fig. 3 The zero bias current barrier height ϕ^{IV}_{bo} from I-V measurements calculated using the eqn. (2) as a function of temperature for the Schottky contacts on samples EB, RF1, RF2 and RF3. The capacitance barrier ϕ^{CV}_{bo} from C-V measurements calculated using eqn. (3) is also plotted. The ϕ^{CV}_{bo} barrier height is essentially the same as the flat band barrier height. While the zero bias barrier height ϕ^{IV}_{bo} increases with temperature, the flat band barrier height decreases slightly.

Table 1 Values of the various Schottky diode parameters at 300 K for the four samples before and after a 573 K (300 C), 30 min sample anneal step. Each value reported is representative of the entire sample. The variation for all the quantities is within (± 0.01).

Parameter	As prepared				Annealed			
	EB	RF1	RF2	RF3	EB	RF1	RF2	RF3
η	1.06	1.07	1.18	1.39	1.06	1.05	1.09	1.12
ϕ^{IV}_{bo}	0.82	0.76	0.64	0.59	0.84	0.81	0.79	0.67
ϕ^{CV}_{bo}	0.85	0.86	0.88	0.91	0.86	0.84	0.85	0.78
ϕ^{IV}_{b} (Richardson)	0.90	0.82	0.75	0.72	0.86	0.83	0.82	0.75
ϕ^{IV}_{b}(Homo)	0.85	0.79	0.72	0.89	0.87	0.85	0.84	0.74

height is essentially the same as the barrier height, ϕ^{cv}_{bo}, determined by the capacitance-voltage (C-V) method [12,13]. The zero bias capacitance barrier height, ϕ^{cv}_{bo}, found from the intercept, V_i, on the voltage axis of the plots of C^{-2} as a function of reverse bias, V_r is given by :

$$\phi^{CV}_{bo} = V_i + \xi + (kT/q) \quad (3)$$

where ξ is the difference between the fermi level and the conduction band and can be calculated from $\xi = (kT/q)\ln(N_c/N_d)$. Here N_c is the effective density of states in the conduction band of the semiconductor, and is given by: $N_c = 2(2\pi m_e^* kT/h^2)^{3/2}$, where m_e^* is the effective mass of the electron. The value of N_c for the case of GaAs at 300 K , is 4.7e17 cm^{-3} [11]. The value of N_d is calculated from the slope of the C^{-2}-V plot and is in the range (0.85-1.0)e17 cm^{-3} . The value of capacitance barrier, ϕ^{CV}_{bo}, thus found from the C^{-2}-V plots of all the samples are also plotted in Fig. 3. It is seen that while the zero bias barrier height, ϕ^{iv}_{bo} , increases with temperature, the flat band barrier height, ϕ^{CV}_{bo} , decreases. In addition there is a large difference between the barrier heights obtained from the I-V and C-V measurements.

The temperature dependence of the saturation current, I_s has also been used to obtain the Schottky barrier height from the Richardson plots, log (I_s/T^2) vs $(1000/\eta T)$ for all the samples. The slope of the Richardson plot is used to calculate the barrier height at 0 K and the intercept at $(1000/\eta T)=0$ is used to calculate the Richardson constant A**. It has been reported [35], that inclusion of the ideality factor η in the saturation current I_s, is necessary to determine the correct Schottky barrier height. The calculated values of the barrier height, and ideality factor by the various methods are presented in Table 1.

IV. Discussion

The observations that ϕ^{iv}_{bo} decreases and η increases with decreasing temperature and the value of η > 1 are at first sight indicative of deviation from the pure thermionic emission theory. Several models of conduction mechanism have been applied to explain the

observed low temperature I-V and C-V characteristics. These models are based on either one or a combination of the following processes: Fermi level pinning by electronic states induced either because of metal induced gap states (MIGS) [37] or defect states at the interface [9,12,29], tunneling through the barrier [5,9], recombination in the depletion region [6-9], interfacial oxide layer [9,17] or barrier height inhomogeneities [18-23]. All the models except the barrier height inhomogeniety model have among them in common that they assume a spatially homogeneous and more or less atomically flat interface between the metal and semiconductor. In this section the measured data is analyzed in the framework of these models to understand the following discrepancies.

When the fermi level is pinned by MIGS, the temperature dependence of Schottky barrier height can be interpreted on the basis of the model developed by Tersoff [37]. There it is assumed that the Fermi level is pinned in the center of the band gap which is at or near the charge neutrality level. For this case the temperature dependence of the barrier height is governed by the temperature variation of the band gap E_g. If we linearize the temperature dependence of E_g, we would expect a linear behavior of the Schottky barrier height with temperature as:

$$\phi_b(T) = \phi_b(T=0) + T\,\alpha_\phi \qquad (4)$$

where α_ϕ is the temperature coefficient of the barrier height and is given by [21,37]

$$\alpha_\phi = (1/2)\,(dE_g/dT) \qquad (5)$$

For Schottky contacts on GaAs, eqn. (5) predicts a temperature coefficient of barrier height = (- 0.17) meV/K. In our case the experimentally measured value of the temperature coefficient for the capacitance barrier height, ϕ^{CV}_{bo}, determined from C-V measurements, is negative (Fig. 3 and table 1). Its value is near zero for for EB and RF1 samples and (- 0.43 to - 0.54) meV/K for the RF2 and RF3 samples. Thus the method of deposition used affects the temperature dependence of capacitance barrier height, $\phi^{CV}_{bo.}$ However, the temperature coefficient of current barrier height, ϕ^{IV}_{bo}, is positive and is = (+0.70 to +1.05) meV/K for different samples which can not be explained by Fermi level pinning models. In addition the variation of the ideality factor with temperature remains unexplained.

Now we analyze the presence of quantum mechanical tunneling through the Schottky barrier for the contacts under study. In GaAs at room temperature the transition from thermionic emission (TE) to thermionic field emission (TFE) occurs at Nd ~ 1×10^{17} cm^{-3}. The forward current voltage relationship for the case of contacts controlled by TFE is given by [5,9,34] :

$$I = I_s \exp(V_f/E_o) \qquad (6)$$

where

$$E_o = E_{oo}\coth(q E_{oo}/kT) = (\eta kT/q) \qquad (7)$$

and the ideality factor η is given by

$$\eta = (q E_{oo}/kT)\coth(q E_{oo}/kT) \qquad (8)$$

where $E_{oo} = (h/4\pi)(N_d/m^* \varepsilon \varepsilon_o)^{1/2} = 2.02 \times 10^{-11} (N_d)^{1/2}$ eV for GaAs. E_{oo} is the characteristic energy, which is related to the transmission probability of the carriers through the barrier. E_{oo} calculated for the contacts under study with a nominal Nd ~ 1×10^{17} cm^{-3} is 6.3 meV. Now TFE dominates only when E_{oo} ~ kT and this corresponds to $T \leq 75$ K. The value of ideality factor at temperature of 300 K and 150 K calculated using equation (7) are η = 1.02 and η = 1.09 respectively, and thus do not fully account for the large value of $\eta > 1.4$ observed for the contacts at T = 150 K. The effective barrier lowering due to the tunneling current is given by the expression: $\Delta\phi_l = (3/2)^{2/3}(E_{oo})^{2/3}(V_d)^{1/3}$, where V_d is the built in potential of 0.8-0.85 volts at 350 K and 0.8-0.92 K at 150 K. Thus the calculated barrier lowering $\Delta\phi_l$ is 40-45 meV over the 350-150 K temperature range in contrast to the observed barrier lowering of several hundred meV.

The temperature dependence of η as shown in Fig. 2 has been investigated by many workers and is also called the T_o effect [9,36]. For a diode displaying T_o effect the η as a function of temperature follows the relationship:

$$\eta = (1 + T_o/T) \text{ or } \eta T = T + T_o \qquad (9)$$

where T_o is a constant independent of temperature. According to eqn. (9) a plot of ηT vs T is a straight line with Y-intercept equal to T_o. The extrapolated value of T_o from the plot of ηT vs T for different samples are found to be in the range 35 – 93 K. To get to this value of T_o only the data in the temperature region of 200 – 350 K has been used. For lower temperatures the value of T_o is much higher. Similar result has been obtained by Hackman and Harrop [9], for Ni/GaAs diodes. In a thorough investigation Padovani [36] showed that the T_o value of Au/GaAs diodes which were fabricated on the same slice of GaAs can vary between 10 and 100 K. The T_o effect has been explained recently by Werner and Guttler [20] and Tung [18,19] by assuming barrier height inhomogeniety model for the Schottky barrier diode.

Another component of current which is responsible for high ideality factor is recombination in the depletion region arising from defects such as deep levels in the forbidden gap and interface state density distribution [6-9]. Depending on the ratio of the thermionic and recombination currents the ideality factor of a diode having both the currents is between 1 and 2. The recombination current is particularly significant at moderately low temperatures (<225 K) and low bias. The η vs V_f plots (Fig. 1) show that for the EB and RF1 samples the η value rises rapidly at low bias and low temperature and reaches a value of 3-4 at 150 K. This type of variation in η can only partly be explained by the presence of recombination current in our samples. For the RF2 and RF3 diodes the η remains constant at 1.5 both at moderate and lower bias and at temperature as low as 150 K. A constant value of η as a function of forward bias can not be explained by the dominance of recombination current as the ideality factor must show an increase at lower bias values.

The Schottky contacts on our GaAs samples are deposited on etched surfaces and a native oxide layer of ~ 10 - 20 A is invariably present on such a surface [9,10,16]. Such an interfacial insulative film is unavoidably formed during usual diode fabrication procedure and the localized electronic states ordinarily exist at the interface between this film and the semiconductor. The electron population of these interface states is assumed to change with applied bias due to which the space charge within the semiconductor and the potential drop across the interfacial layer changes. For an MIS diode with oxide layer of thickness δ and interface states in equilibrium with the semiconductor, an increase $\Delta\eta$ in the ideality factor is given by the relation [9] : $\Delta\eta = [\delta (\varepsilon_o \varepsilon_s + q W D_s)/(\varepsilon_o \varepsilon_i W)]$ where D_s is the surface state density on the substrate, ε_s and ε_i are the dielectric constants of GaAs and of the oxide layer respectively and W is the depletion depth. For a surface state density of 1×10^{13} $cm^{-2} eV^{-1}$ and interfacial oxide of thickness, $\delta = 10$ A, we get $\eta = 1.53$. The above analysis predicts the large increase in η with increase in δ but its dependence on temperature and bias is better understood by the model developed by Maeda et al [16].

Maeda and co-workers [16,17] proposed a non-equilibrium approach in which all the interface states communicate both with the semiconductor and metal. The position of the interface Fermi level is determined by a balance between the capture and release of electrons from and into the interface states from the conduction band and the metal. The expression for the occupation ratio of the interface states is [17] :

$$\frac{D_{sb}}{D_s} = \frac{C n_s}{B^* + v \exp(-U/kT) + C n_s} \qquad (10)$$

where D_{sb} is an average density of occupied interface states between the Fermi levels of the interface states and the metal. D_s is the interface state density, B^* is a tunneling probability of electrons from the interface states to the metal, ν is an attempt-to-escape frequency of the thermal release of electrons from the interface states to the conduction band, U is an activation energy of the thermal release, C is a capture coefficient of electrons by the interface states from the conduction band and n_s is the carrier concentration at the top of the barrier. The ideality factor is given by the relationship

$$\eta = [1 - (1-\gamma) D_{sb} / D_s]^{-1} \qquad (11)$$

where γ is estimated by a slope of the ϕ_{bo} vs ϕ_m plot according to the equation : $\phi_{bo} = [\gamma (\phi_m - \chi) + (1 - \gamma) (Eg - q \phi_o) / q]$. The value of γ estimated by Ikoma et al [17], is ~ 0.08. Now the occupation ratio (D_{sb} / D_s) given by eqn. (10) increases as temperature is lowered, because the probability of the thermal release of

electrons from the interface states to the conduction band is substantially decreased. In addition the occupation ratio also increases as the forward bias is lowered because of the same reason. Ikoma et al [17] have shown that for a change in the occupation ratio (D_{sb} / D_s) from 0.1 to 0.7, ideality factor increases from 1.1 to 3.0. This model thus explains the increase in η above a value of 2 with decreasing temperature at lower bias observed for the EB and RF1 samples. For the case of RF2 and RF3 samples however, the η increase observed is up-to 1.6 at 150 K and low bias. This is possibly because of the affect of the high energy plasma on the interfacial oxide layer. It has been reported that a process of cleaning of the surface of the substrate is taking place during sputter deposition because of the chemical reactivity of the plasma tail and the high energy of the sputtered atoms [5]. This process may have a very large effect on the thickness of the interfacial oxide layer present in the metal-semiconductor interface and therefore on the mechanism of current transport. However the other main observations on $\phi^{IV}{}_{bo}$ and $\phi^{CV}{}_{bo}$ are not explained.

4.1. *Barrier height inhomogeneities*

All the processes modeled above explain one or the other anomaly. However, there has been no theory, which is capable of explaining all of these inconsistencies in a coherent manner. The temperature dependence of barrier height, ideality factor and the difference between the current barrier height and capacitance barrier height shown in Fig.3 are not fully explained. An assumption on which above models are based is that the metal-semiconductor interface is spatially homogeneous and more or less atomically flat. According to Henisch [41], fluctuations in barrier height within the same contact are unavoidable as they exist even in the most carefully fabricated systems. Recent experimental investigations utilizing ballistic electron emission microscopy (BEEM) technique have revealed lateral non- uniformity of the local Schottky barrier height on Si and III-V semiconductors [25-27,38].

The Schottky barrier height inhomogeneity models have been developed recently by Tung [18,19] and Werner and Guttler [20] and many of the anomalies observed in our I-V and C-V characteristics have been explained using these models. The barrier height inhomogeneity model explains the large discrepancy observed in the barrier heights obtained from the I-V and C-V measurement. Ohdomari and Tu [30] were the first to show that the effective barrier height controlling the I-V characteristics of a mixed barrier phase contact is the low barrier phase. On the other hand the barrier height determined from the C-V measurements is dominated by the phase which occupies the larger contact area. These results were obtained on mixed phase contacts isolated from one another. However, in real Schottky barriers, barrier height differences over the contact area occur because of variations in the interfacial layer thickness and/or composition and also because of interfacial charges [27].

According to Werner and Gutler model [20], the interface between the metal and semiconductor is not atomically flat but rough, with the result of spatial fluctuations of the built-in voltage, V_d and the Schottky barrier height. Apart from the roughness of the interface due to thickness modulation of the metal as well as atomic steps, dislocations and grain boundaries in the metal, these potential fluctuations may also arise from a local effective barrier lowering due to field emission at metallic diffusion spikes with narrow radii of curvature, non-uniformities of the interfacial charge and locally defective hot regions [13,20]. The shape and position of the ridges in the potential "hills" depend on the bias voltage and therefore, cause $\eta > 1$ in I-V curves. Various types of distribution patterns of SBH e.g. a Gaussian [20,28-31] or normal [22] or log-normal [32] have been proposed to explain the abnormal I-V behavior and the difference in the SBH's deduced from the I-V and C-V characteristics. Evidence for the Gaussian distribution of the barrier height to be present has been found from the investigations carried out using the BEEM technique. The barrier height data shown in Fig. 3 is analyzed according to the following equation given by Werner and Guttler for the Gaussian distribution of barrier heights [20,28] :

$$\phi^{IV}{}_{bo} = \phi_{b-mean} - \left[\frac{\sigma^2{}_s}{(2kT/q)} \right] \tag{12}$$

where σ_s is the standard deviation of the barrier distribution around a mean barrier and $\phi_{b\text{-mean}}$ is the mean barrier height, which is also equal to the capacitance

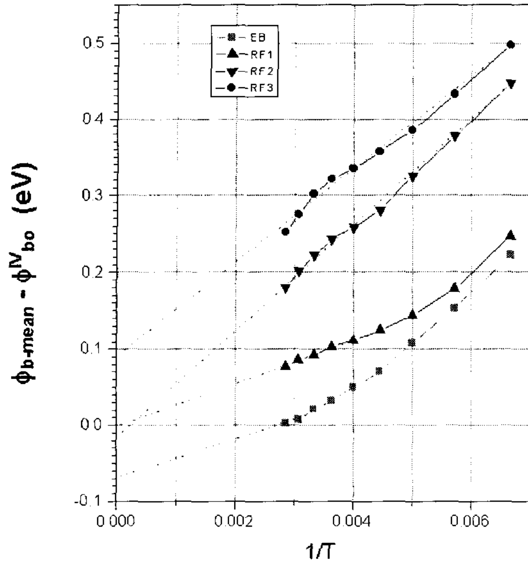


Fig. 4 Plot of difference of capacitance barrier and current barrier, ($\phi_{b\text{-mean}}$ - ϕ^{IV}_{bo}) vs (1/T) for the four samples under study.

Table 2 Temperature coefficient of Schottky barrier height determined from the I-V and C-V measurements and from the data presented in Fig. 3.

Sample	α_ϕ^{CV} (meV / k)		α_ϕ^{IV} (meV / K)	
	As prepared	Annealed	As prepared	Annealed
EB	-0.05	0	1.05	1.1
RF1	0	-0.05	0.64	1.08
RF2	-0.43	-0.125	0.91	1.2
RF3	-0.54	-0.225	0.70	1.02

Table 3 The values of standard deviation of barrier height, σ_s and its temperature coefficient α_σ as defined by eqn. (13) for the as prepared and annealed samples.

Sample	Standard deviation, σ_s (meV)		α_σ (meV)^2 / K	
	As prepared	Annealed	As prepared	Annealed
EB	65 – 110	85 – 105	- 10.3	-19.75
RF1	68 – 112	84 – 105	0	-18.9
RF2	110	108	-2.55	-27.5
RF3	105	105	+12.9	-17.2

barrier height, ϕ^{CV}_{bo} [20]. Equation (12) thus explains the current barrier, ϕ^{IV}_{bo} is indeed always smaller than the mean barrier and decreases with decreasing temperature and explains the barrier height vs temperature characteristic of Fig. 3.

The mean SBH, $\phi_{b\text{-mean}}$ and the standard distribution, σ_s may be both temperature and bias dependent. The temperature dependence of the mean SBH is approximately linear as can be seen in the ϕ^{CV}_{bo} data plotted in Fig. 3 [also in 12,20-22]. For the case of σ_s being independent of bias and temperature, eqn. (12) suggests that a plot of ($\phi_{b\text{-mean}}$ - ϕ^{IV}_{bo}) vs (1/T) is a straight line passing through origin and with a slope of (q σ^2_s / 2k), which can be used for σ_s determination. Fig 4 shows such a plot and Table 3 lists the range of standard deviation observed for different samples in the temperature range 150-350 K. It is seen that the standard deviation for the EB and RF1 samples at 300–350 K is 65 mV but it continuously increases and reaches a value of 110 mV as the temperature is lowered to 150 K. This result indicates the existence of low barrier height patches which dominate the I-V characteristics only at lower temperatures. The standard deviation for the RF2 and RF3 samples is high ~ 105-110 mV at all temperatures. Thus the standard deviation of barrier height increases as the RF power is increased. This indicates that the increased plasma damage because of the higher RF power increases BH inhomogeneity. The observation of non-zero Y- intercept in Fig. 4 can also be understood because of temperature dependence of the standard deviation of the SBH. Werner and Guttler [21] postulated a temperature dependence of the form:

$$\sigma^2_s(T) = \sigma^2_s(T{=}0) + \alpha_\sigma T \qquad (13)$$

Putting eqn. (13) in eqn. (12), it changes to:

$$\phi^{IV}{}_{bo} = \phi_{b-mean} - \left[\frac{\sigma^2{}_s(T=0)}{(2kT/q)}\right] - \left[\frac{\alpha_\sigma}{(2k/q)}\right] \qquad (14)$$

Thus a plot of ($\phi_{b\text{-mean}}$ - ϕ^{IV}_{bo}) is still a straight line with slope of (q σ^2_s(T=0) / 2kT) and intercept (q α_σ / 2k) . From eqn. (13), we get a value of α_σ as (-10.3), 0, (-0.015) and (+12.9) (meV)^2 / K for the EB, RF1, RF2 and RF3 samples respectively.

According to the barrier height inhomogeneity model the increase in the ideality factor at lower temperatures is modeled by the equation [18-20,31]

$$\frac{1}{\eta} = 1 - \rho_2 + \frac{q\rho_3}{2kT} \qquad (15)$$

where ρ_2 and ρ_3 are the voltage coefficients of barrier

Table 4 Values of the voltage coefficients ρ_2 and ρ_3 which fit the measured ideality data to eqn. (15)

Sample	ρ_2		ρ_3 (mV)	
	As prepared	Annealed	As prepared	Annealed
EB	-0.17	-0.15	-11.8	-11.9
RF1	-0.13	-0.13	-10.3	-11.6
RF2	-0.05	-0.13	-9.9	-11.9
RF3	+0.23	-0.11	-2.5	-11.1

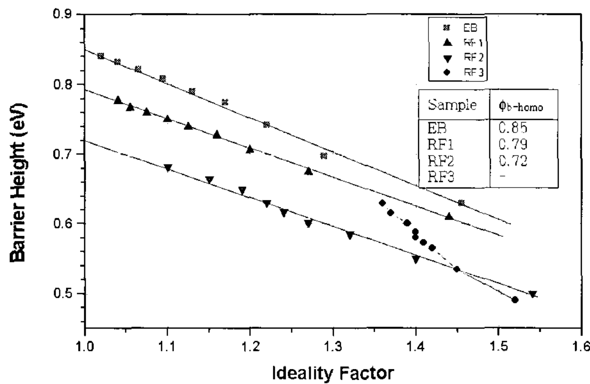


Fig. 5 The zero bias barrier height vs ideality factor at different temperatures. The extrapolation to $\eta = 1.01$ yields the homogeneous barrier height shown in the inset. The data for sample RF3 has not been extrapolated as it spans a very narrow range of high ideality factor.

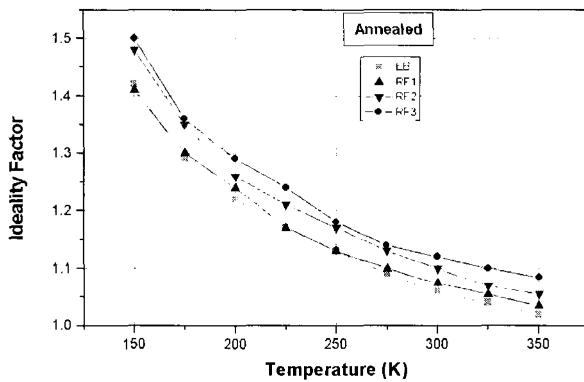


Fig.6 Ideality factor as a function of temperature for the samples after a 300 C, 30 min. anneal step.

height and standard deviation respectively which quantify the voltage deformation of the inhomogeneous barrier distribution. This equation correctly predicts the decrease of η with increasing temperature. According to Tung's model [18], the ideality factor of an inhomogeneous Schottky contact with a distribution of patches of different barrier heights will increase when the measurement temperature is lowered. This is because the patches with lower barrier height have a larger ideality factor and vice versa. Eqn. (15) indicates that a plot of $\{(1/\eta) - 1\}$ vs $(1/T)$ should yield a straight line with slope of $(q\ \rho_3 / 2\ k)$ and Y-intercept of $(-\rho_2)$. Table 4 shows the voltage coefficient ρ_2 and ρ_3 obtained by a fit of the temperature dependent ideality data to eqn (15). The data in table 4 shows that $\rho_2 < 0$, $\rho_3 < 0$ for all the samples except RF3. Similar data on ρ_2 and ρ_3 has been obtained on the measured idealities of other authors [20].

Using Tung's theoretical approach, Schmitsdroff et al. and Hudait et al. [33,34] found a correlation between the zero bias barrier height and the ideality factor. The extrapolation of the linear fit to the ϕ^{IV}_{bo} vs η data shown in Fig. 5 gives a homogeneous barrier height at an ideality factor of about 1.01. According to Schmitsdroff et al [33], and Zussman [5], the larger the discrepancy between the homogeneous barrier height and the C-V barrier height, ϕ^{CV}_{bo}, poorer is the quality of the metal-semiconductor interface. It is seen from table 1 that the difference between these two barrier heights is maximum for the RF3 sample and minimum for the EB sample.

V. Effect Of Heat Treatment

The electrical characteristics of diodes were studied after a 300 C, 30 min. anneal step in N_2 environment. The Ti Schottky contacts have been reported to be electrically stable with annealing upto 400 C [1-3,5,40] and so this step should not affect the metallurgical interface much.

The annealing step causes a reduction in the forward current for all the samples, although the extent of reduction is different for different samples. For the EB sample the forward current, I_f at 300 K reduces by a factor of 2, whereas for the RF samples the reduction is much larger. Thus I_f reduces by a factor of 6-10 for the RF1, 120-200 for the RF2 and 20-30 for the RF3 samples. The ideality factor η as a function of measurement temperature for the annealed samples is shown in Fig. 6. The data for annealed and as prepared samples is presented in Tables 1 to 4 suggests the following:

1. The temperature coefficient of capacitance barrier height decreases to a value closer to the theoretical value.

However, the temperature coefficient of current barrier height increases for all samples (table 2).

2. The ideality factor in the temperature range of 250-350 K is seen to improve considerably for the RF2 and RF3 samples. The ideality factor for the RF1 and EB samples shows negligible change after the annealing treatment. Thus the plasma damage which is considerably higher in the RF2 and RF3 samples anneals out with the anneal step.

3. The current barrier height increases after annealing for all the samples. Although the increase for the EB sample is very little but still the EB barrier height is maximum at 0.84 eV. The barrier height increase for all the RF samples is appreciable indicating decrease in the low barrier height patches. These low barrier height patches may be produced because of donor like defects and high electric field regions formed due to plasma damage and are reduced by the process of annealing.

4. The annealed samples show closer agreement between the barrier heights measured by different methods i.e. ϕ^{IV}_{bo}. ϕ^{CV}_{bo}. $\phi^{IV}_{b\ (Richardson)}$ and $\phi^{IV}_{b\ (homo)}$. However for the RF3 sample the ϕ^{IV}_{bo} is still quite small indicating remnant low barrier height patches.

5. The standard deviation of barrier height, σ_s remains same at 105-110 mV for all samples. However, the lower value of σ_s observed at higher temperatures for the EB and RF1 samples increases after the anneal cycle (table 4). The process of anneal makes the interfacial oxide layer thin and this implies that more intimate contacts have higher inhomogeneities.

VI. CONCLUSIONS

In this paper a study on the electrical characteristics of the Au/Pt/Ti/(n)GaAs Schottky contacts prepared by the two techniques of electron beam deposition and rf sputtering is described. The presence of high ideality factor at lower bias for the EB and RF1 samples was also analyzed. The characteristics were analyzed in the framework of different models viz. Fermi level pinning model, interfacial layer model, barrier height inhomogeneity model and the presence of recombination and tunneling currents.

The variation of current barrier height, capacitance barrier height, ideality factor and the difference between the values of current and capacitance barrier heights are fully explained by assuming the dominating process to be the presence of patches having different barrier heights with a distribution. This barrier height inhomogeneity model also explains the lower barrier height for the RF samples because of the presence of low barrier height patches produced because of high plasma energy. The variation of capacitance barrier height can be explained by the Fermi level pinning model predicting the rate of change to be governed by the rate of change of band gap with temperature.

The recombination current model explains the higher ideality factor at lower temperature and lower bias but the increase of η above 2 for the EB and RF1 samples can only be explained by the presence of tunneling currents or occupation ratio of the interface states in the interfacial oxide layer.

The annealing of the samples have the effect of increase in the barrier height, more so for the RF samples with high deposition power indicating reduction in plasma damage which may be responsible for low barrier height patches and thus affecting the current barrier height. This is proved by the fact that for the EB sample, where this plasma damage is not there the barrier height increase is very nominal.

The EB Schottky contacts have the highest typical current barrier height of 0.85 eV and capacitance barrier height of 0.86 eV after annealing and so are most suitable for use as gate contacts in the fabrication of MESFETs and HEMTs. The RF3 Schottky contacts have the lowest typical current barrier height of 0.67 eV and capacitance barrier height of 0.78 eV and so are most suitable for fabricating millimeter wave mixer and detector diodes where the local oscillator power and the RF signal to be detected are very weak. In addition the low temperature performance of the RF2 and RF3 contacts where their ideality factor remains <1.6 even at a low bias of 50 mV makes them better diodes for space applications involving low temperatures.

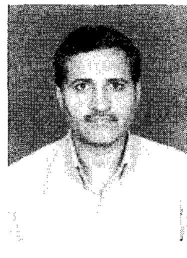
ACKNOWLEDGEMENTS

The help of Mrs. Seema Vinayak in sample preparation and Mrs. Rachna Manchanda in electrical measurements is gratefully acknowledged. The authors

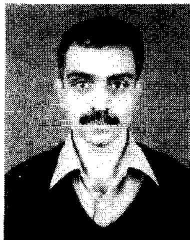
are thankful to Dr. Vikram Kumar and Dr. H.P.Vyas for encouragement and permission to publish this work.

REFERENCES

[1] Y.T.Kim, C.W.Lee, and D.J.Kim, Appl. *Phys. Lett.*, 72, 1507 (1998).
[2] B.K.Sehgal, R.Gulati, A.A.Naik, S.Vinayak, D.S.Rawal, H.S.Sharma, *Materials Science and Engineering* B48, 229 (1997).
[3] S.P.Kwok, *J. Vac. Sci. Technol.*, B4, 1383 (1986).
[4] A.Cola, M.G.Lupo, L.Vasanelli and A.Valentini, *J. Appl. Phys.*, 71, 4966 (1992).
[5] A.Zussman, *J. Appl. Phys.*, 59, 3894 (1986).
[6] M.D.Dio, A.Cola, M.G.Lupo and L.Vasanelli, *Solid State Electron.*, 38, 1923 (1995).
[7] F.D.Auret, S.A.Goodman, Y.Leclerc, G.Myburg and C.Schutte, *Materials Science and Technology*, 13, 945 (1997).
[8] W.J.Devlin, *Electronics lett.*, 16, 92 (1980).
[9] E.H.Rhoderick, R.H.Williams, *Metal-Semiconductor Contacts*, Oxford, Clarendon Press (1988).
[10] B.L.Sharma, *Metal-Semiconductor Schottky Barrier Junctions and their applications* (ed. B.L.Sharma), New York, Plenum (1984).
[11] S.M.Sze, *Physics of Semiconductor Devices* 2nd ed., New York, Wiley (1981).
[12] H.W.Hubers and H.P.Roser, *J. Appl. Phys.*, 84, 5826 (1998).
[13] V.W.L.Chin, M.A.Green and J.W.V.Storey, *J. Appl. Phys.*, 68, 3470 (1990).
[14] E.Grussel, S.Berg and L.P.Andersson, *J. Electrochem. Soc.*, 127, 1571 (1980).
[15] S.J.Fonash, S.Ashok and S.Singh, *Appl. Phys. Lett.*, 39, 423 (1981).
[16] K.Maeda, H.Ikoma, K.Sato and T.Ishida, *Appl. Phys. Lett.*, 62, 2560 (1993).
[17] H.Ikoma, T.Ishida, K.Sato, T.Ishikawa and K.Maeda, *J. Appl. Phys.*, 73, 1272 (1993).
[18] R.T.Tung, *Phys. Rev.*, B45, 13509 (1992)..
[19] R.T.Tung, *Appl. Phys. Lett.*, 58, 2821 (1991).
[20] J.H.Werner and H.H.Guttler, *J. Appl. Phys.*, 69, 1522 (1991).
[21] J.H.Werner and H.H.Guttler, *J. Appl. Phys.*, 73 1315 (1993).
[22] Y.P.Song, R.L.V.Meirhaeghe, W.T.Laflere and F.Cardon, *Solid State Electron.*, 29, 633 (1986).
[23] A.Gumus, A.Turut and N.Yalcin, *J. Appl. Phys.*, 91, 245 (2002).
[24] J.R.Waldrop, *Appl. Phys. Lett.*, 44, 1002 (1984).
[25] A.Olbrich, J.Vancea, F.Kreupl and H.Hoffman, *J. Appl. Phys.*, 83, 358 (1998).
[26] G.M.Vanalme, L.Goubert, R.L.V.Meirhaeghe, F.Cardon and P.V.Daele, *Semicond. Sci. Technol.*, 14, 871 (1999).
[27] H.Palm, M.Arbes and M.Schulz, *Phys. Rev. Lett.*, 71, 2224 (1993).
[28] S.Chand and J.Kumar, *Semicond. Sci. Technol.*, 12, 899 (1997).
[29] P.Revva, J.M.Langer, M.Missous and A.R.Peaker, *J.Appl. Phys.*, 74, 416 (1993).
[30] I.Ohdomari and K.N.Tu, *J. Appl. Phys.*, 51, 3735 (1980).
[31] S.Zhu, R.L.V.Meirhaeghe, C.Detavernier, F.Cardon, G.Ru and B.Z.Li, *Solid State Electron.*, 44, 663 (2000).
[32] Zs.Horwvath, *Mater. Res. Soc. Symp. Proc*, 260, 359 (1992)
[33] R.F.Schmitsdroff, T.U.Kampen and W.Monch, *J. Vaç. Sci. Technol.*, B15, 1221 (1997).
[34] M.K.Hudait, P.Venkateswarlu and S.B.Krupanidhi, *Solid State Electron.*, 45, 133 (2001).
[35] S.Ashok, J.M.Borego and R.J.Gutman, *Solid State Electron.*, **22,** 621 (1979).
[36] F.A.Padovani, *Semiconductors and semi-metals* (ed. Wilardson RK, Beer AC) NY, Academic Press (1971).
[37] J.Tersoff, *Phys. Rev.*, B35, 6182 (1987).
[38] M.Forment, R.L.V.Meirhaeghe, A.D.Vrieze, K.Strubbe and W.P.Gomes, *Semicond. Sci. Technol.*, 16, 975 (2001).
[39] S.Dhar, V.R.Balakrishnan, V.Kumar and S.Ghosh, *IEEE Trans. Electron Dev.*, 47, 282 (2000).
[40] B.K.Sehgal, B.Bhattacharya, S.Vinayak and R.Gulati, *Thin Solid Films*, 330, 146 (1998).
[41] H.K.Henisch, *Semiconductor contacts,* Oxford Univ. Press. (1984).

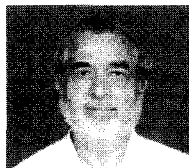


Dr. B. K. Sehgal is a senior scientist at the Solid State Physics Laboratory, Delhi, India. He has more than 20 years of experience in the development of GaAs microwave Device technology. Currently, he is leading a group of scientists working on the development of MESFET's, HEMT's and MMIC's and their technology transfer for production. He has published more than 20 research papers and is a recipient of Young Scientist award and path breaking research award for development of 12 GHz MMIC technologies.
He is PhD in physics from University of Delhi, Delhi.



Dr. V.R. Balakrishnan joined the Solid State Physics Laboratory, Delhi in 1986. He received the Doctorate in Physics from Indian Institute of Science, Bangalore in 1997. Currently he is leading a group of scientists on deep level characterisation of semiconductor materials and devices. He was a visiting scientist at the Paul Drude Institute, Berlin, Germany during 2001-2002. He has published more than 10 papers in reputed international journals. He is a recipient of the National Science Talent Scholarship instituted by Government of India.

Dr. (Mrs) R. Gulati is heading the GaAs Device fabrication facility at the Solid State Physics Laboratory, Delhi, India. She has done M.Sc. (Solid State Physics) and PhD (Physics) from University of Delhi, Delhi. She has over 30 years research experience in the development of high frequency microwave devices and integrated circuits and their technology transfer for production. Currently she is leading team of scientists for the development of 40 GHz HEMT based MMIC technology. She has published over 30 research papers and is the recipient of several awards such as IETE award for development of microwave components and path breaking research award for development of 12 GHz MMIC technologies.



Dr. S. P. Tewari is a professor of Physics in the Department of Physics & Astrophysics, University of Delhi, India for the last 16 years. Since joining Delhi University over 30 years ago, he is involved in various academic activities, supervising research work leading to the award of PhD degrees and organising/ chairing several national/international conferences. He has published over 100 research papers in international reputed journals in different branches of condensed matter physics such as superconductivity, density-density distinct and auto-correlation functions, ordered and disordered materials, electron dielectric functions in solid state plasma ranging from highly degenerate (metallic) to non-degenerate state (semiconductors), transport and production of intense beams of cold neutrons and fullerite and Bose-Einstein condensates.

He has co-authored seven research level books. He was a visiting professor at North-western University, USA and Commonwealth Academic staff Fellow at Bristol University, UK. He has been a consultant and senior participant at International Center for Theoretical Physics, Trieste, Italy and has also visited many countries for his research activities.