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고속 네트워크를 위한 ATM Switch 설계

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A Design of ATM Switch for High Speed Network

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요 약

본 논문은 중재기가 제공되는 새로운 타입의 입출력 버퍼 ATM 스위치를 제안하고 다양한 트래픽 상태하에서 그 성능을 연구하였다. 제안된 스위치는 PRI 신호를 제어할 수 있는 중재기의 구조와 특성을 최대한 활용하기 위한 목적으로 설계되었다. 제안된 스위치의 기본적인 목적은 간단한 입력 버퍼 스위치에서 발생하는 HOL 블록킹 현상을 제거하거나, 적어도 줄일 수 있도록 하는 것이다. 여러 가지 HOL 중재 알고리즘들이 이러한 목적으로 논문을 통해 제안되었다. 제안된 스위치에서는 중재기와 출력단에 버퍼를 이용하여 HOL 블록킹 현상의 억제를 효과적인 방식으로 시도하였다. 중재기는 다수의 잘 알려진 HOL 조정 알고리즘 중에서 Three Phase Algorithm을 사용하도록 설계되었다. 제안된 스위치는 REQ 신호를 통하여 우선 전송의 제어를 요청, 이 신호를 중재기로 전송함으로써 중재기는 입력 버퍼로부터 전송된 신호를 제어한다. 컴퓨터 시뮬레이션 결과는 비균일 random 트래픽 상태 하에서 제안된 스위치의 효과를 설명하기 위해 제공하였다.

Abstract

This thesis proposes a new type of Input-Output Buffered ATM Switch which employs an arbiter and its performance under different traffic conditions studied. The proposed switch is designed with a view to exploit the architecture and other characteristics of the arbiter. The primary aim of the proposed switch is the elimination, or at least, the reduction of HOL blocking phenomenon which occurs in the simple input buffered switch.

Several HOL arbitration algorithms have been proposed for this purpose in the literature. The proposed switch attempts to reduce the HOL blocking as it uses the arbiter and the buffer at the output port in an effective manner. The arbiter is designed to work with Three Phase Algorithm which is one of the many well known HOL arbitration algorithms. The proposed switch acquires control over priority transmission through the REQ signal. As the signals are transmitted to the arbiter, the latter controls the one which is sent by the input buffer. Computer simulation results have been provided to demonstrate the effectiveness of the proposed switch under non-uniform random traffic conditions.

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Ⅰ. Introduction

ATM switches are the core components of the ATM network, which has been emerging as one of the best candidates for integrated broadband communications.

Among these ATM switches, first we will consider the input buffered switch with a view to introduce the Head Of Line(HOL) blocking phenomenon. If multiple cells addressed to the same destination arrive at an input buffered switch, then only one cell is served at the current time slot and the others remain at the head of each input buffer for serving at next time slot.

This phenomenon is called the HOL blocking, which limits the maximum throughput of the input buffered switch to only 58.6 percent $(2-\sqrt{2})$[3].

In order to reduce the HOL blocking which occurs at input buffer, many HOL arbitration algorithms have been proposed. These algorithms have been reported in the literature[4]-[9]. They include, the Recirculation Algorithm(proposed Huang and Knauer), Three Phase Algorithm (proposed Hue and Arthurs), Ring Reservation Algorithm(proposed Bingham and Bussey), Look-Ahead Contention Resolution Algorithm(proposed Karol and Hluchyj).

In this paper, a new type ATM switch architecture has suggested, which can not only reduce the HOL blocking but also control the priority signal by the arbiter.

Therefore, the main idea of the proposed switch is to reduce the HOL blocking which occurs in the input buffered switch and control the priority signal which employs as it exceeds the value of threshold which is predefined at input buffer using the arbiter. This thesis proposes a high-speed input-output buffered switch that employs an arbiter to eliminate of at least reduce the HOL blocking which occurs in the input buffered switch. The arbiter is adopted to the three phase algorithm which is one of algorithms mentioned above. The proposed switch also includes a buffer at the output port to reduce the HOL blocking. To control the priority signal, the following method is used. First, we assume that the value of threshold is predefined. In this thesis, the value of threshold is set at 80% of the input buffer in the computer simulations.

If the input buffer exceeds the value of the threshold, it sends a REQ signal with the PRI signal during the current time slot to receive the power of priority of transmission. Then the arbiter sends the ACK signal earlier than the other cells which send only the REQ signal. As mentioned before, the proposed switch controls the priority signal by the arbiter.

Based on above scheme, we will investigate the proposed switch performance through computer simulations. This switch will be studied under diverse traffic condition in terms of several viewpoints such as cell loss probability, mean cell delay and throughput the traffic condition include Uniform random traffic as well as bursty traffic.

Ⅱ. Proposed Input-Output Buffered Switch

An Input-Output Buffer Switch which employs an Arbiter is proposed. The main emphasis of this thesis is on reducing the HOL blocking and

on controlling the power of prority of transmission by the PRI signal.

1. Proposed Switch Architecture

An input-output buffered switch which employs an Arbiter is proposed here. It consists of N input and output buffers and a space- division switch block. The switch block is enclosed within dotted lines in Fig. 1. It consist of a crossbar switch and Control Logic(CL). In Fig. 1, CL is the square box composed of N Arbiters which perform the routing function from the input port to the destination output port.

The Input and Output buffers facilitate the tasks of entry, storage and sending of cells to the destination port. The switch block has arbiters which implement appropriate routing functions.

A detailed description of the proposal follows.

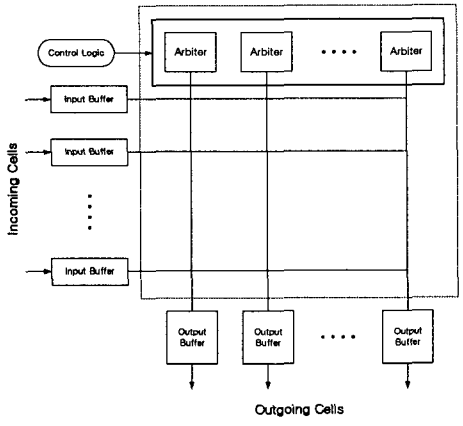

Fig. 1 The architecture of the proposed switch

2. The principle of Switching Operation

It is assumed that only one cell arrives at any input during any time slot. Further, the threshold level of the input buffer is fixed before the switching begins. Also, it is assumed that it operates in a time-slotted fashion and each REQ signal in the cell transmission algorithm is (N+1)-bit long, the priority being specified in the last bit.

If a cell which has the destination output port number arrives at the input port, then the incoming cells are stored at each input buffer in their natural order(FIFO). Also, each input buffer checks if the input buffer size exceeds the value of the threshold or not, during every time slot. If the input buffer size exceeds the value of the threshold at a particular input buffer, then the REQ signal's last bit is set to '1'. And the REQ signal is transmitted to the destination output port through space-division switch block in the same order as shown in Fig. 1. Cell transmission is initiated when the arbiter acknowledges the REQ signal corresponding to the value of the routing tag of the head cell(that is, the head cell at the input buffer).

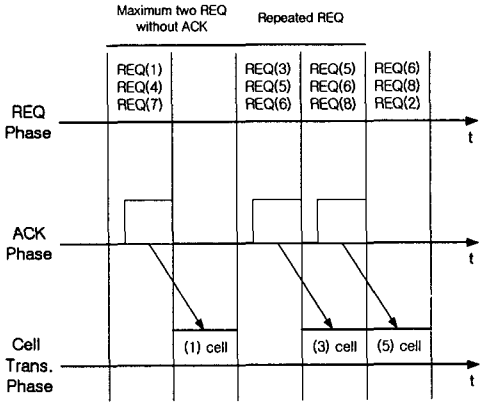

Fig. 2 The Cell Transmission Algorithm at input buffer to the Arbiter

If a cell appears at the head of each input buffer, the corresponding bits are set to '1'(See Fig. 2). Also the input buffer checks its size in order to find its priority state. If it exceeds the value of the threshold, then the REQ signal's last bit, that is, the priority bit is set to '1'. In that case, the input buffer gets the ability of sending the REQ signal for the first time. When it requests the power of transmission of the head cell at each input buffer, each input port checks the REQ signal's last bit, that is , the priority

bit, to find out the priority state. If the last bit is set to '1', the input buffer sends the REQ signal together with PRI signal. Each arbiter which requested the power of transmission of the head cell at each input buffer checks the REQ signal that is sent at the input port first, and ASBM's corresponding bit is set to '1' as shown in Fig. 3. If the priority bit is set to '1'(this means that the input buffer sends the REQ signal together with the PRI signal), then the arbiter can be acknowledged.

If the number of input buffers that send the REQ signal and PRI signal together is more than two, each arbiter can be allocated the power of priority transmission as it sends the ACK signal directly to each input port by a round-robin policy. The transmission of ACK signal to the rest of the input ports may also adopt a round-robin policy. If the input buffer has not received the ACK signal from the arbiter during the current time slot, then the head cell of that input port must wait to be served during the next time slot. The input port that is assigned the power of transmission, that is, the input port that receives the ACK signal from the arbiter, can transmit the head cell from the current input port to the destination output port during the next time slot. This is the mode of information flow in the proposed switch. This procedure repeats during every time slot. As mentioned above, there can be an m-fold increase in the input cell stream speed signalling reduction in HOL blocking that occurs in the input-buffered switch.

The cell transmission algorithm is described below. Fig. 2 Shows the cell transmission Algorithm. The well known three-phase algorithm has been adopted here. That is, the cell transmission algorithm is composed of a request phase(REQ), an acknowledgment phase(ACK), and a cell transmission phase(Cell Trans.). Cell transmission is related closely to the arbitration of CL as shown Fig. 1.

3. The Operation of Priority Round-Robin Arbiter(PRRA)

The arbiter assigns priorities according to a round-robin policy. It decides the power of priority transmission among the input ports that send the PRI signal by examining whether the PRI signal occurs more than once or not. If no input port carries the PRI signal, then it assigns the power of priority transmission by adopting a round-robin policy on the head of the input buffer. Transmission to a full output buffer is suppressed by making the normally High TE(Transmission Enable) signal low.

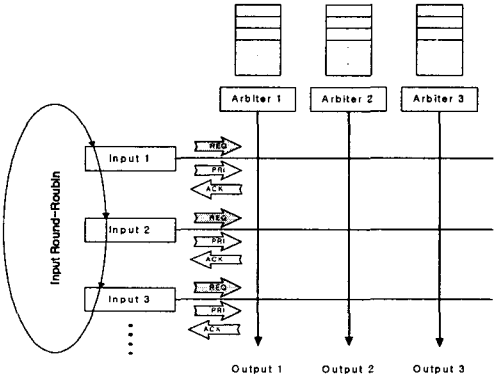

Fig. 3 The Principle of the Arbiter Operation

Fig. 3 depicts the operation of the arbiter. The arbiter is the core of the CL(see Fig. 1). It consists of N arbiters and an Arbiter Status Bit Map(ASBM) corresponding to each output port. The N inputs shown in Fig. 3 designate N input buffers. The signal lines connected between the arbiter and inputs are bus lines. Details of the components or functions are described below.

The signal lines are classified into two types deponding on where it is connected to: the input signal buses and the output signal buses. The horizontal lines in Fig. 3 are the input lines(buses) connected to N inputs, that is, N input buffers. The signal from the input buffer flows through these lines. The signals passing

through these buses have been described earlier. There are : REQ signal and PRI signal in REQ phase and ACK signal in ACK phase. This signal performs the services in different classes(Such as setting the 1 bit in the REQ signal's last bit position etc). This signal is also used for designating whether each bit of the REQ signal is of higher priority or not.

The vertical lines are the output signal lines(buses) which are connected between N arbiters and N output buffers. If one cell to be delivered is determined by the arbitration, this cell goes to the output buffer through this line.

The operation of the arbiter is very simple since no complicated arbitration algorithm is used. All the procedures follow the round-robin algorithm. The two ovals in Fig. 3 emphasize this algorithm. left oval is the input round-robin and three small oval in top is top is the arbiter roun d - robin according to the priority, respectively.

A particular time slot is shown in Fig. 2. Each input port sends the REQ signal via the input signal line synchronously. It may be recalled that each bit of REQ signal corresponds to each output port and each bit of ASBM corresponds to an input buffer. Then, the ith bit of each REQ signal from all input buffers. If there is only one ith whose state is high, the input port which sent the REQ signal with 'high-state' i the bit is selected for service. If there are two or more ith bits whose state is high, then the arbiter looks up ASBM in the sequence of input round - robin. In this case, we must consider the PRI signal which can change the round - robin sequence. If the ith bit having higher priority (by input round-robin) has an unmarked ASBM bit, then the input is selected for serving a cell in the current time slot. But, if the corresponding ASBM bit is marked, (that is, the input port of ASBM bit is selected previously by another arbiter(s)), another ASBM bit is tested, and so on. Each bit of ASBM is used for designating whether the corresponding input is selected for service or not.

Ⅲ. Experimental Results

The primary aim of the computer simulation is to study the performance of the algorithm. The performance parameters which have been singled out for investigation are Cell Loss Probability (CLP), Mean Cell Delay(MCD) and Throughput. A 8×8 switch is simulated with a view to study its efficiency. The incoming cells at the input buffer are assumed to have identical distribution. They are assumed to realize independent identically distributed Bernoulli trials with parameter p at the beginning of every time slot. The traffic distribution at the output port is assumed to be uniform. That is, with a switch size of N×N, the probability that the cell finds itself at the output port is 1/N. Cell loss only occurs owing to an overflow at the input buffer.

1. Bursty Traffic

In this model, input traffic alternates between active(busy) and silent(idle) periods, while output port addresses are still uniformly distributed. In particular, each of the inputs is described by the same On - Off model where both busy and idle periods have durations that are geometrically distributed. Cells within the same burst are destined to the same output port(i.e., cell belong to the same fragmented packet). Basically, each time slot is governed by a Bernoulli process, where given an input is in an On(busy) state, it will remain in that state (i.e., during the next time slot) with probability 1-p, while it will switch to the Off(idle) state with probability p.

An On state corresponds to a burst being transmitted on an input link while the Off state corresponds to a silence period (Fig. 4)[11].

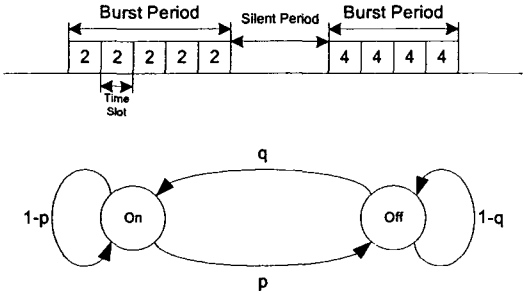

Fig. 4 On(Burst) - Off(silent) Traffic Model

The probability of a burst consisting of k time slots is given by :

$$B(k) = p(1-p)^{k-1}, \quad k \geq 1$$

Note that we assume there is at least one packet in the burst.

If the input is in the Off(idle) state, where no cells arrive, it will stay in the same state with probability 1-q and then the probability that an idle period lasts k time slots is simply :

$$I(k) = q(1-q)^{k}, \quad k \geq 0$$

It also takes into account the case where a burst can be followed immediately by another burst (i.e., two different streams being multiplexed) in which case there is no idle period (k = 0). The offered load can then be calculated as:

$$\rho = \frac{E[busy-period]}{E[busy-period] + E[idle-period]} = \frac{q}{q+p-pq}$$

It is assumed that there is no correlation between different bursts, and the destination of each burst is uniformly distributed among the output.

So far, we have discussed the model of bursty traffic in brief. The computer simulation results are given below. Here, we only consider the case in which the average burst length is 8.

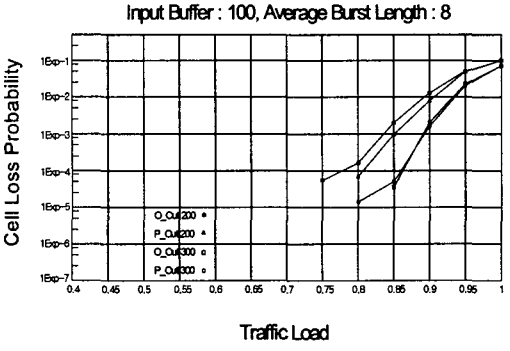

Fig. 5 The Cell Loss Probability according to the Traffic Load

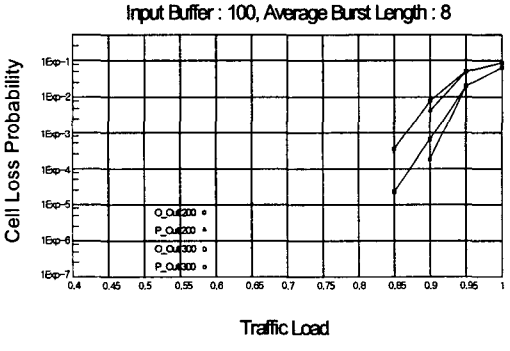

Fig. 6 The Cell Loss Probability according to the Traffic Load

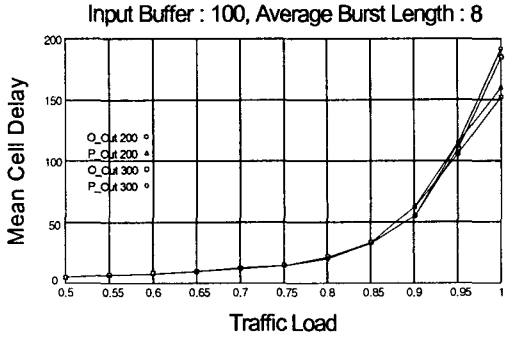

Fig. 7 The Mean Cell Delay according to the Traffic Load

First, we investigate the effect of a change in the input buffer size on the CLP. Figs. 5 and 6 depict the cell loss probability versus the traffic load. The input buffer sizes are 100 and 300, respectively. The output buffer size is fixed at 200 and 300.

Fig. 7 and 8 show the effect of traffic load on the mean cell delay while the input buffer size is fixed at 100, 200 and 300, respectively. The output buffer size is fixed at 200 and 300. For a load of 0.85 and a load of 1.0, the difference of the MCD between the proposed switch and the conventional switch becomes wider during the period when the input buffer size is large. This means that the CLP of the proposed switch is smaller than that of the conventional one as shown in Figs. 5 and 6.

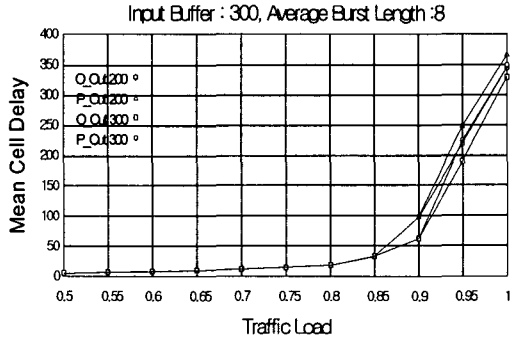

Fig. 8 The Mean Cell Delay according to the Traffic Load

We consider the maximum throughput from the viewpoint of two factors: the average burst length(ABL) and the output buffer size. Fig. 9 shows the variation maximum throughput with average burst length and Fig. 10 depicts the maximum throughput versus output buffer size.

Output buffer sizes are kept 200 and 300 while investigating the variation of ABL. As shown in Fig. 9, the maximum throughput decreases slightly if there is an the increase in ABL. If the output buffer size is 300, the size of reduction is small than that in the case with an output buffer size of 200. When the ABL is 8, the maximum throughput is about 90% and 94%, in the two cases respectively. While the ABL is about 30, the difference is about 10%(Fig. 9). Fig. 4 examines the situations with ABL 1 and ABL 8. When the ABL is 1, unicast cell cast is realized in essence. With ABL of 1, the maximum throughput approaches about 100% as the output buffer size increases. But, When the output buffer size is 300, the maximum throughput is about 94%(See in Fig. 10).

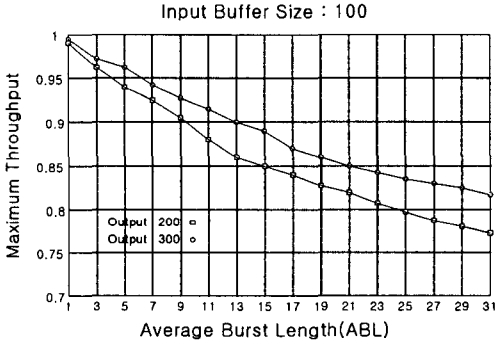

Fig. 9 The Maximum Throughput according to the Average Burst Length(ABL)

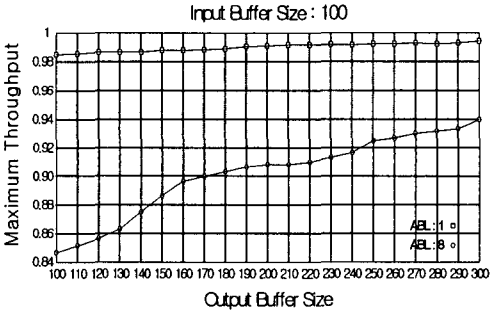

Fig. 10 The Maximum Throughput according to the Output Buffer Size

Ⅳ. Conclusions

A new type of input-output buffered ATM switch which employs an arbiter has been proposed in this thesis. Its performance has been studied under varying traffic conditions.

The proposed switch exploits the architecture and other characteristics of the arbiter which influence the PRI signal. The primary objective of the investigation has been the elimination of HOL blocking. The threshold level is prefixed at the input buffer. The arbiter acquires, through the REQ signal, control over the power of priority transmission at the input buffer when the threshold is exceeded.

The proposed switch can altogether eliminate or at least reduce HOL blocking. The arbiter adopts the Three Phase Arbitration Algorithm. Control over the power of priority transmission is exercised by setting the priority bit in accordance with the size of the input buffer. When this signal is transmitted to the arbiter, the latter can control the one which is sent by the input buffer.

Computer simulation results have been provided to demonstrate the effectiveness of the proposed switch in reducing HOL blocking. Futher, the switch is seen to return enhanced performance as the input buffer size is increased. Indeed, the switch has many advantages over the conventional switch in respect of the CLP and MCD.

Non-uniform traffic conditions have been considered. Cell multicasting has also been investigated in this regard.

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