SiO_2/Si_3N_4 이중 박막의 C-V 특성

論 文
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Capacitance-Voltage Characteristics in the Double Layers of SiO_2/Si_3N_4

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Abstract - The double layers of SiO_2/Si_3N_4 have superior charge storage stability than a single layer of SiO_2. Many researchers are very interested in the charge storage mechanism of SiO_2/Si_3N_4 [1,2]. In this paper, the electrical characteristics of thermal oxide and atmospheric pressure chemical vapor deposition (APCVD) of Si_3N_4 have been investigated and explained using high frequency capacitance-voltage measurements. Additionally, this paper will describe capacitance-voltage characteristics for double layers of SiO_2/Si_3N_4 by "Athena", a semiconductor device simulation tool created by Silvaco, Inc.

Key Words : Electret, Oxide (SiO_2), Nitride (Si_3N_4), C-V Plot, HTB(High Temperature Bias)

1. Introduction

Many applications in the field of sensors and actuators benefit from the possibility of advanced charge storage in electrets as an important component. Various devices based on the characteristics of electrets, such as microphones, air filters, and radiation dosimeters, have already been proposed and utilized in the industry [2, 3].

SiO_2 is well known as a superior electrets material. Unfortunately, the thermal oxide layer shows compressive stress and significant surface conduction, which affects the charge storage lifetime [4]. In recent years, the double layers of SiO_2/Si_3N_4 electrets were widely investigated because of their excellent charge storage stability [5,6]. Due to the tensile stress of the double layers of SiO_2/Si_3N_4, electrets can be directed to the compensate the internal stress by variation of the ratio of their layer thickness [7]. In this paper, the electrical characteristics of thermal oxide and atmospheric pressure chemical vapor deposited (APCVD) nitride were investigated using high frequency capacitance-voltage measurements.

This paper will describe the C-V characteristics of double layers SiO_2/Si_3N_4 with the help of the semiconductor device simulation tool, "Atlas" manufactured by Silvaco, Inc.

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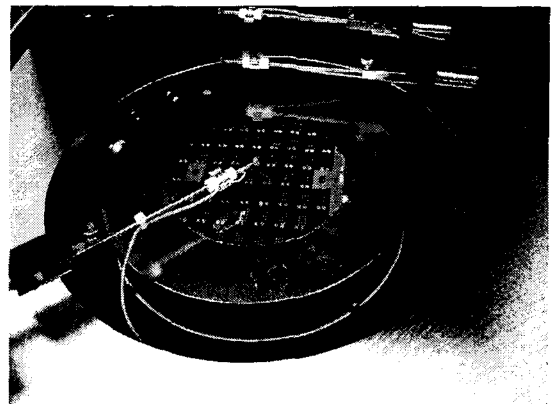
2. Experimental

2.1 Composition of samples

We started with a 100[mm] silicon wafer (manufactured by ShinEtsu Co.), and <111> oriented and p-doped materials (substrate resistivity of 25[Ωcm]) were chosen as substrate.

These wafers were thermally oxidized at 1000[℃] for several minutes in quartz furnaces. To obtain a higher density thermal oxide, they are made with two additional dry oxidation steps and are thus called dry-wet-dry structures. The photograph of the wafer probe station for capacitance-voltage characteristics is shown in Photo 1.

Photo. 1 The photo of wafer probe station for capacitance-voltage characteristics.



The Si_3N_4 layer was deposited by the APCVD (Atmospheric Pressure Chemical Vapor Deposition) method at 780[℃]. The desired film thickness was extracted by variation of the deposition duration and then measured using a Nanometrics210 (Film Thickness System).

The silicon wafers were made from the front side with an evaporated aluminum electrode of 1[㎛] thickness. The unwanted SiO_2 layer and Si_3N_4 films on the backside of the substrate wafer were removed by chemical etching using the SEG102(Spin Processor Co.). 1[㎛] of aluminium was deposited on the oxide. The mask for C-V measurement was used. The composition of the samples is provided in Table 1.

Table 1 The sample composition information

No.	SiO_2 Thickness [Å]	Si_3N_4 Thickness [Å]
#1	2000	1000
#2	2000	1500
#3	2000	2000
#4	3000	1000
#5	3000	1500
#6	3000	2000
#7	3000	0
#8	0	1500

Total capacitance of the double layers per unit area were calculated with

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_{nit}} \quad (1)$$

where $\varepsilon_0, \varepsilon_{ox}$ and ε_{nit} are the relative permittivity of the vacuum, SiO_2 and Si_3N_4, respectively. The equivalent thickness of the double layer is

$$d_{tot} = d_{ox} + (\frac{\varepsilon_{ox}}{\varepsilon_{nit}}) \cdot d_{nit} \quad (2)$$

3. Results and Discussion

To investigate the capacitance voltage characteristic exactly and to compare it theoretically, computer simulation and actual testing were executed.

3.1 Simulation result

Figures 1 and 2 show the simulated capacitance-voltage characteristics at several samples with varying thickness. We can see that the capacitance value decreases with increasing positive gate bias, from 7[V] to +7[V].

This thickness dependent characteristic can be explained by a simple diagram. For negative bias, the majority carrier (hole) in the p-substrate follows the accumulation mode near the p-substrate surface.

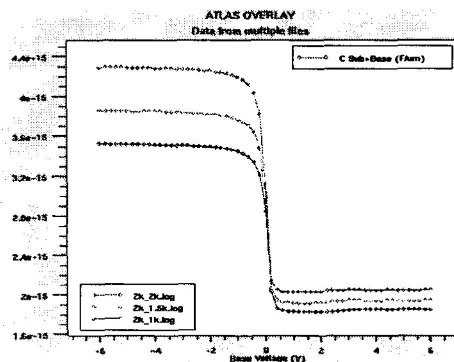


Fig. 1 C-V characteristic due to various thickness.

When the gate bias voltage is lower than 1[V], the hole carrier can be accumulated. The capacitance value reaches a maximum and does not change further with a negative bias. In this case, the total capacitance value of the sample equals the capacitance of the $SiO_2(C_{ox})$ and the capacitance of the $Si_3N_4(C_{nit})$ series connection.

Increasing the positive gate bias, the depletion capacitance value by majority carrier in p-substrate far away from the surface in silicon bulk is added to the series connection. Due to this reason, total capacitance value $C_{tot} = \left(C_{nit} + C_{ox} \pm C_{dep}\right)^{-1}$ decrease.

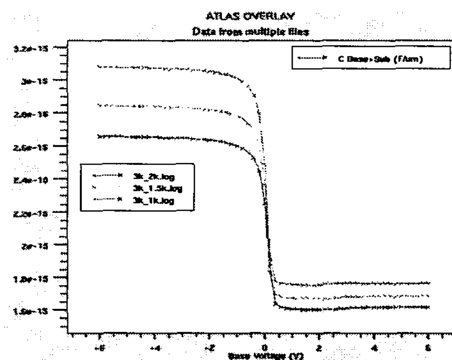


Fig. 2 Capacitance of the sample at different thickness.

Figure 3 shows the simulated potential profile and electric field profile at double layers of SiO_2(2000[Å])/Si_3N_4(1000[Å]).

The potential distribution and electric field in SiO_2/Si_3N_4 electrets samples has beeen estimated and the electric field crowding phenomenon near the base electrode edge can be seen. In the case of potential distribution, it gets the uniformity potential is under the base electrode.

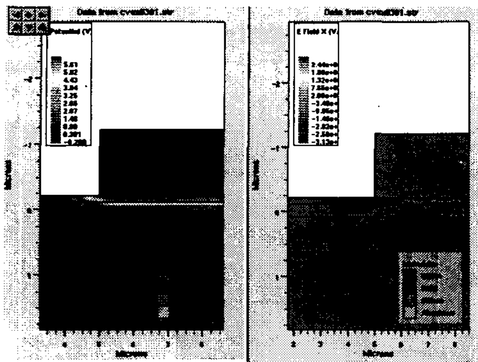


Fig. 3 Simulated potential profile and electric field distribution of the SiO_2(2k[Å])/Si_3N_4(1k[Å]) sample.

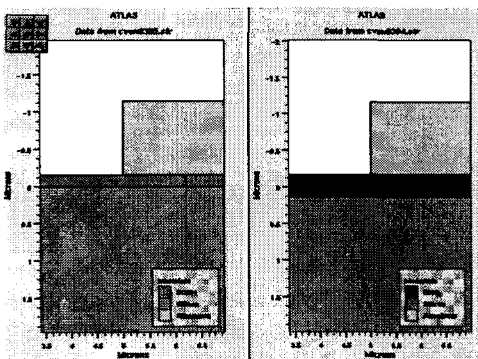


Fig. 4 Simulated model of the SiO_2(3[Å]) and Si_3N_4(1.5 [Å]) sample

Figure 4 shows the simulation structure model single layers of SiO_2 and Si_3N_4, respectively. Figure 5 shows the simulated results of capacitance characteristics in single layer and double layers, respectively. In contrast, for the single Si_3N_4 layer, thickness-dependent capacitance value was observed at the base bias by high dielectric constant and lower sample thickness. The single layer of Si_3N_4 has a very high capacitance value during the negative base biased state due to the high dielectric constant and lower thickness as compared to other samples.

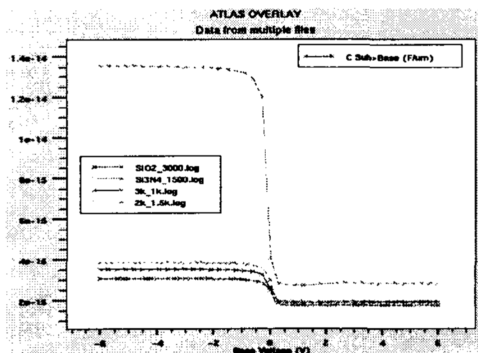


Fig. 5 Capacitance of the samples at SiO_2 and Si_3N_4 single layer and double layer, respectively.

3.2 Experimental results

To measure the mobile charge of SiO_2/Si_3N_4 double layer, we progress to HTB, which adds both positive & negative voltage at high temperatures. This experiment helps to maximize the ion's mobility at high temperatures.

Figures 6 and 7 show the experimental capacitance-voltage characteristics of several samples with varying thickness. We can see that the actual result decreases with increasing positive gate bias, from 50[V] to +50[V].

This plot provides information on the location in the double layers of SiO_2/Si_3N_4 of any contamination. The total capacitance value increase with increasing Si_3N_4 thickness during the positive base bias in figures 6, 7, and 8.

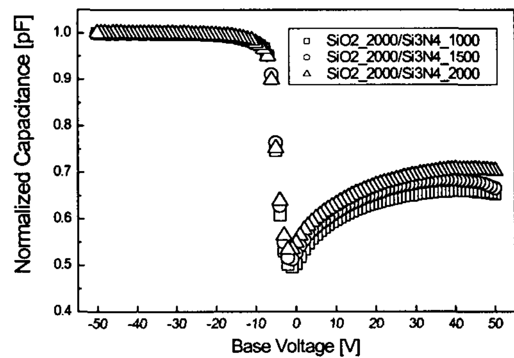


Fig. 6 Capacitance characteristics of the SiO_2(2k[Å]) /Si_3N_4(1k[Å], 1.5k[Å], 2k[Å]) samples.

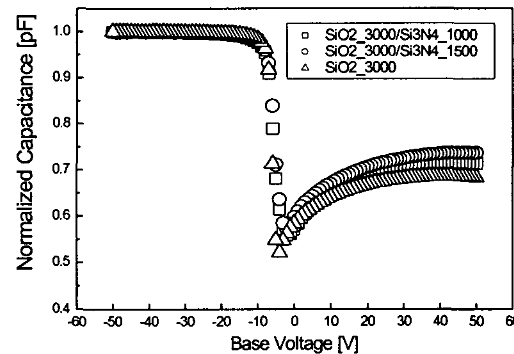


Fig. 7 Capacitance characteristics of the SiO_2(3k[Å]) /Si_3N_4(1k[Å], 1.5[Å]) and single SiO_2(3k[Å]).

Specially, in figure 8, it can be confirm that Si_3N_4 single layer's dielectric constant is about twice as much as than SiO_2. Therefore, under normalized C-V plot, we can check whether it shows low value around the positive bias compared to SiO_2/Si_3N_4 double layers.

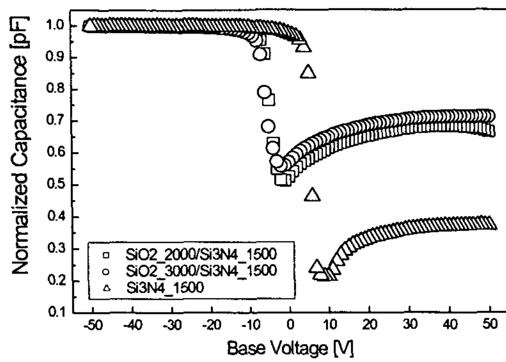


Fig. 8 Capacitance characteristics of the SiO_2(2k[Å], 3k[Å])/Si_3N_4(1.5k[Å]) and single Si_3N_4(1.5k[Å]).

Figure 9 illustrates the experimental capacitance-voltage characteristics of the SiO_2/Si_3N_4 sample after thermal stress. The actual result shows a decrease with increasing positive gate bias, from 50[V] to +50[V].

Two stress cycles should be used in this experiment. It is necessary to measure all the mobile ions in the double layers sample. The first stress of 100[V] forces the mobile ions to a known position. The second stress of 100[V] then moves the ions across the double layers after reaching a 200[℃] soak temperature.

The shift between the second(+100[V] stress plot) and third plots(-100[V] stress plots) provides the most accurate mobile charge.

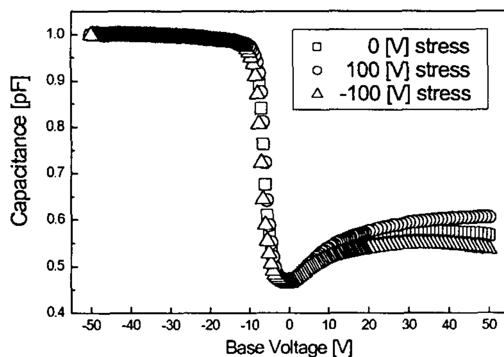


Fig. 9 Capacitance characteristics of the SiO_2(3k[Å])/ Si_3N_4(1k[Å]) sample after thermal stress.

Different capacitance-voltage characteristic values at negative stress bias and positive stress bias in single layers can be achieved.

In figure 9, we confirm that the capacitance-voltage characteristics at the positive bias condition are stable. However, we can find voltage shift with about 10 to 20[V] for single layers in figure 10 and 11. From figure 10, we can forecast the quantity of mobile charge of SiO_2 single layer followed by C-V pilot's shifted value by THB treatment. In figure 11, we can confirm that C-V plot has been affected by the movement of positive ions. Compared to SiO_2 single layer, it has been moved by +100[V] stress to Si_3N_4-Si interface, whereas, the capacitance multiplied by ΔV(shifted voltage) is mobile ionic charge.

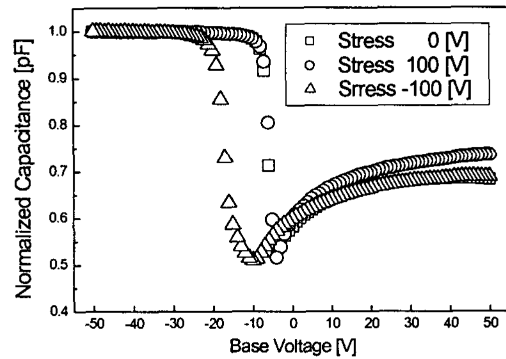


Fig. 10 Capacitance characteristics of the single layer SiO_2(3k[Å]) sample after thermal stress.

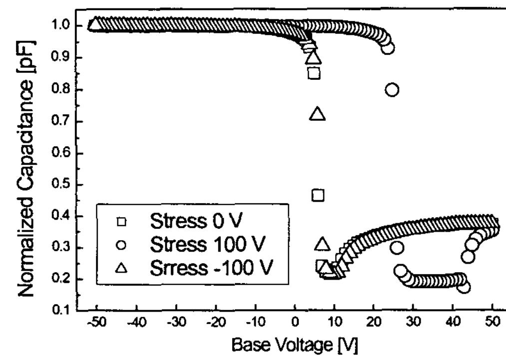


Fig. 11 Capacitance characteristics of the single layer Si_3N_4(1.5k[Å]) sample after thermal stress.

The following equation describes the relationship between the flat-band voltage shift and the total charge.

$$\Delta V_{FB} = \frac{Q_m}{q}\frac{T_{tot}\cdot q}{K_{tot}\cdot \varepsilon_0} \quad (3)$$

Therefore, the total mobile charge, *Qm*, is found by definition from the flat-band voltage.

$$Q_m = q\cdot \Delta V_{FB}\frac{2.1E10}{T_{tot}}\ [C/cm^2] \quad (4)$$

Table 2 shows total results of experiment results. The SiO_2/Si_3N_4 double layer's voltage has been changed from max. 0.43 [V] to min. 0.19[V]. However, on the other

side, single layer can be changed from max. 19.53[V] to min. 11.38[V]. According to these figures, we can learn that under single layer, the mobile charge's movement is unrestrained but under double layers, the mobile charge's movement is very limited. In addition, from the charge stability view point, double layers have greater predominance characteristics than single layer.

Table 2 Charge measuring data by C-V plot after HTB.

Condition	Vfb range	Qm $*e^{11}[C/cm^2]$
2000/1000	-6.49 ~ -6.86	4.41
2000/1500	-6.47 ~ -6.78	4.08
2000/2000	-6.83 ~ -7.02	4.09
3000/1000	-7.73 ~ -8.16	4.26
3000/1500	-7.68 ~ -7.97	3.97
3000/2000	-7.48 ~ -7.78	3.67
SiO2_3000	-7.12 ~ -18.5	4.74
Si3N4_1500	24.9 ~ -6.86	-17.1

4. Conclusion

We investigated the SiO_2/Si_3N_4 electrets according to the various layer structures in order to obtain the optimal condition.

In double layers of SiO_2/Si_3N_4 electrets, by increasing the thickness of the Si_3N_4 layer reduces the charge stability. The actual capacitance voltage value depends slightly on the thickness of the Si_3N_4 layers. The traps, which are responsible for the charge stability in the investigated electrets, are much deeper than the traps in the single layer. We supposed the origin of these traps might be the interface between the SiO_2 and Si_3N_4 layers.

In this paper, we can see the peculiarity of charge stability of SiO_2(2k[Å])/Si_3N_4(2k[Å]) by the experiment of single layer and SiO_2/Si_3N_4 double layers. A more detail dissertation of double layer electret's charge stability can be achieved by additional TSC experiments.

Futher study will help in understanding more about charge stability. We will update the status once additional investigation has been performed.

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