# A 1.8 GHz SiGe HBT VCO using 0.5 μm BiCMOS Process

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## Abstract

In this paper, we fabricated an 1.8 GHz differential VCO using a commercial 0.5 μm SiGe BiCMOS process technology. The fabricated VCO consumes 16 mA at 3 V supply voltage and has a $1.2 \times 1.6$ mm$^2$ chip area. A phase noise measured at 100 kHz offset carrier is $-110$ dBc/Hz and a tuning range is 1795 MHz~1910 MHz when two varactor diodes are biased from 0 V to 3 V.

*Key words* : SiGe, BiCMOS, VCO, Phase Noise, Flicker Noise.

## I. Introduction

The phase noise of a VCO has significant effects on digital cellular systems. A SiGe device is a good candidate for designing an oscillator of low power and low phase noise since that device has advantages of low turn-on voltage and good phase noise characteristics due to low 1/f noise and noise figure [1],[2].

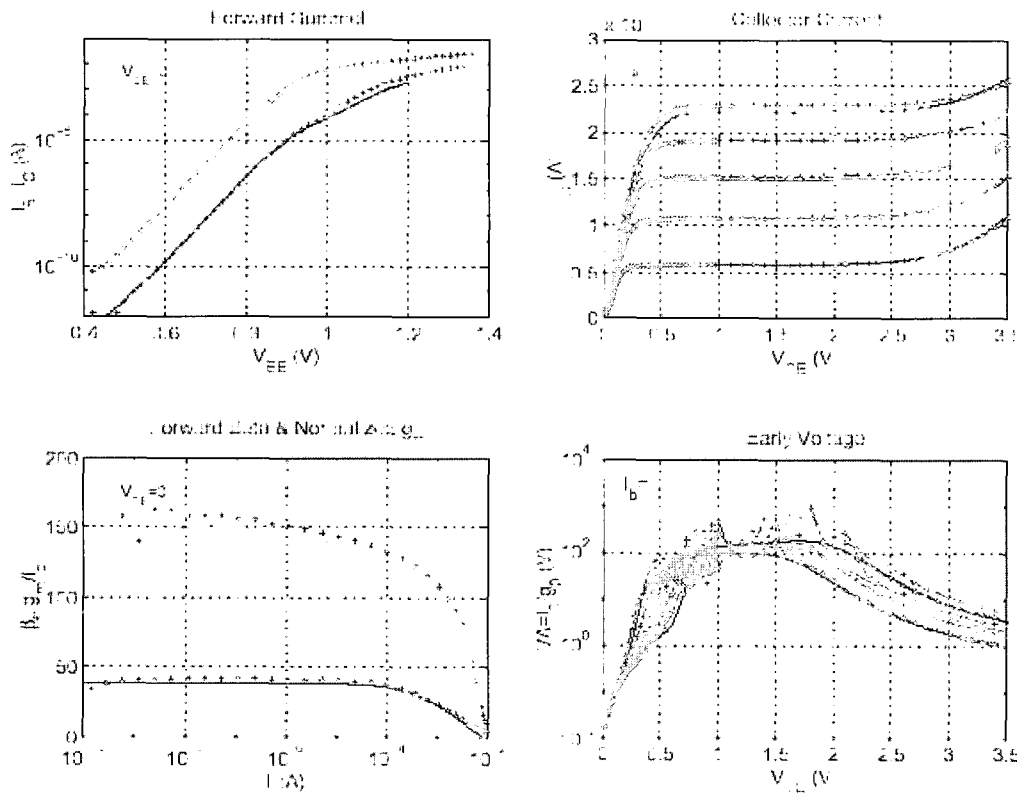In this paper, a fully monolithic differential VCO is designed and fabricated using a commercial 0.5 μm



Fig. 1. SiGe HBT DC characteristics.

SiGe BiCMOS process. The fabricated VCO achieved a low phase noise of $-110$ dBc/Hz at 100 kHz offset carrier and 115 MHz tuning bandwidth. The third harmonic suppression of more than 22 dBc was obtained. A current 16 mA at 3V supply voltage runs in the VCO of $1246 \times 1649 \, \mu m^2$ chip area.

## II. SiGe HBT and Inductance Characteristics

In this section, The DC and AC characteristics of HBT, and the Q factor of inductor used in VCO design are showed. In Fig. 1, it is known that forward beta $\beta_f$ is 150 and an early voltage is 110 V. Fig. 2 shows that a cutoff frequency $\beta_f$ is 50 GHz at Ic = 1.5 mA. In Fig. 3, it is shown that the Q-factor of 8.2 nH inductor is 6.6 at 1.6 GHz[3].

## III. VCO Design

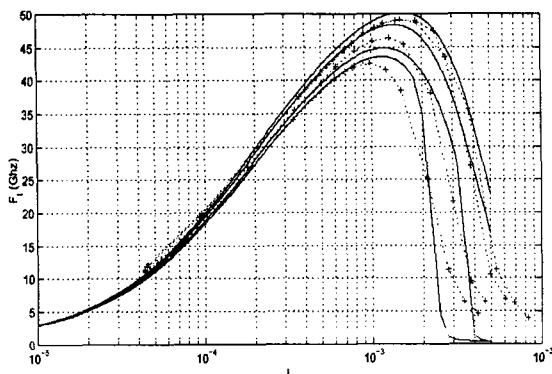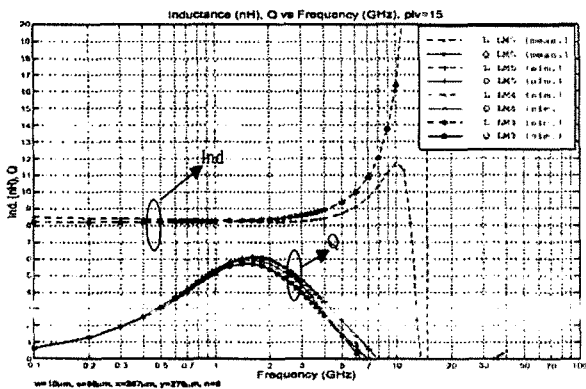Fig. 4 shows the VCO circuit diagram. The VCO core is a differential cross-coupled type that generates a negative resistance. The VCO core is divided into three parts. The description of this VCO circuit will be made into three parts, in turn. The first of them is the active part which gives rise to a negative resistance, required to start oscillation in VCO circuit. The negative-resistance part is composed of HBT Q1, Q2, Q3 and Q4. The output of Q1 does positively feedback into Q2 and that of Q2 into Q1 through the base-emitter capacitances Cbe3, Cbe4 of Q3 and Q4, respectively. For that reason, a wide range of negative resistance is caused and if some oscillation conditions are achieved with resonators coupled, the circuit starts to oscillate. Here, Q3 and Q4 have a part to amplify an oscillation signal as well as to cause a positive feedback[4],[5].

The cross-coupled type is shown in Fig. 5. The input resistance $R_{in}$ of the cross-coupled pair is as follows[6].

$$R_{in} = -2/g_m \qquad (1)$$

Here, $g_m$ is transconductance.

The second is the resonance part of the VCO which consists of varactor diodes, inductors and capacitors,



Fig. 2. SiGe HBT AC characteristics.
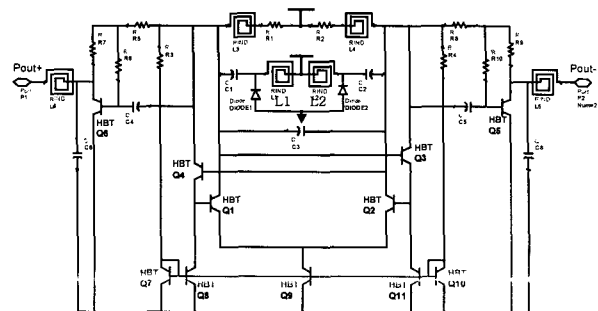


Fig. 3. Inductor characteristics.



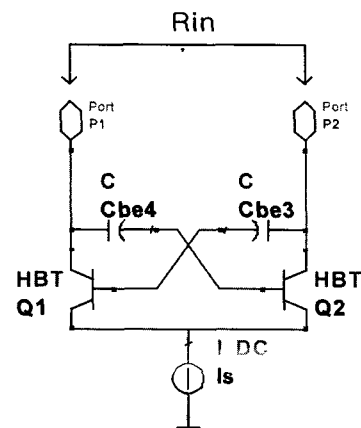Fig. 4. Differential VCO Full Schematic.



Fig. 5. Cross-Coupled Topology generating negative resistance.

and does primarily determine the phase noise characteristics of the designed VCO. In the resonator of this VCO, L1 and L2 were used having 8.2 nH inductance, and a pair of varactor diodes were symmetrically placed The last is a buffer that amplifies an oscillation power of the VCO core, which consists of HBT(Q5 & Q6), inductor and capacitor. The amplifier operates in common emitter configuration, and a shunt capacitor and a series inductor are used for transferring maximum power to load.

## IV. Simulation and Measurement

Fig. 6 shows the chip photograph of the fabricated VCO. The chip size of the VCO has $1246 \times 1649$ $\mu\,m^2$. The oscillation frequency of the VCO was measured using Agilent 85652 spectrum analyzer as can be shown in Fig. 7. Fig. 7 shows second harmonic suppression of $-22$ dBc and third harmonic suppression more than it at 1.8 GHz in the fabricated VCO. Also, the VCO obtained a phase noise of $-110$ dBc/Hz at 100 kHz offset from carrier frequency as represented in Fig. 8. In Table 1, the simulation and measurement results are compared.

Our target was to design PCS VCO using cadence tool, but the frequency range was shifted down by about 170 MHz. It is supposed that the frequency deviation is due to various parasitic elements, such as
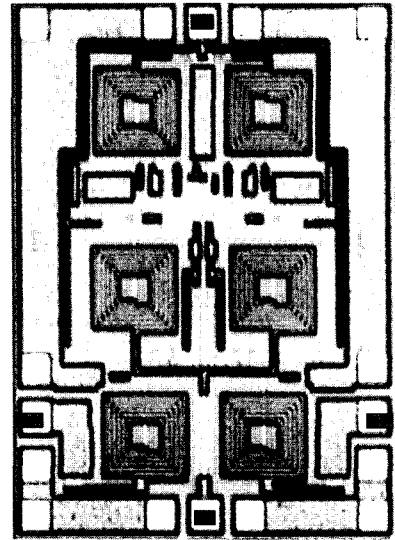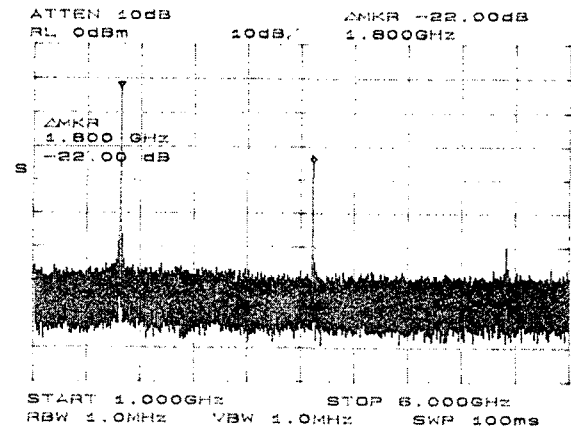


Fig. 6. Die photograph of the VCO.



Fig. 7. Oscillation Frequency Spectrum.

capacitances, inductances, resistances on layout.

In Table 2, the performance results of this VCO and others are summarized and compared. This VCO is better than any other using silicon process in phase noise. The phase noise of VCO can be represented by the following formula[7]:

Table 1. Summary of simulated and measured results.

| Parameter | Simu. | Meas. |
|---|---|---|
| Supply voltage [V] | 3 | 3 |
| Current [mA] | 16 | 16 |
| Tuning range [MHz] | 1837~2084 | 1795~1910 |
| Phase Noise @ 100 kHz | – | – 110[dBc/Hz] |
| 2nd harmonic suppression [dBc] | – 20 | – 22 |
| Output power | – 4 ~ – 6 | – 9.3 ~ – 11.7 |

Table 2. Comparison of this VCO and others.

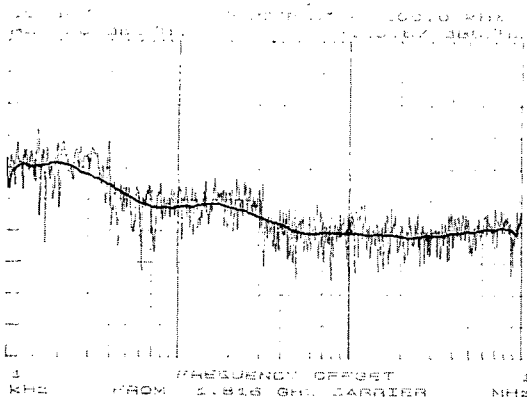| Reference number | Fabrication Process | $f_t$ [GHz] | $f_o$ [GHz] | $V_{cc}$ [V] | Power [mW] | $P_{out}$ [dBm] | Bandwidth [MHz] | Phase Noise [dBc/Hz] |
|---|---|---|---|---|---|---|---|---|
| [7] | 0.8 μm BiCMOS | 11 | 1.48 | 3.6 | 40 | – 9.4 | 150 | – 105 @100 kHz |
| [8] | BiCMOS | 10 | 1.75 | 5 | 70 | – 25 | 200 | – 88 @100 kHz |
| [9] | 0.5 μm Bipolar | 25 | 1.9 | 3.3 | 41 | – 5 | 200 | – 103 @100 kHz |
| this VCO | 0.5 μm SiGe BiCMOS | 50 | 1.82 | 3 | 48 | – 10.4 | 115 | – 110 @100 kHz |

Fig. 8. Phase Noise.

$$L(f_m) = 10 log \left\{ \left( \frac{f_o}{2Qf_m} \right)^2 \left[ \frac{FkT}{2P_{out}} \left( 1 + \frac{f_c}{f_m} \right) \right] + \frac{1}{2} \left( \frac{K_{vco}V_m}{2f_m} \right)^2 \right\} \quad (2)$$

where $L(f_m)$ is the phase noise in dBc/Hz, $f_o$ is the output signal frequency of VCO in Hz, $Q$ is the quality factor of VCO, $f_m$ is the offset frequency in Hz, $F$ is the noise figure of transistor, $k$ is Boltzmann' constant in J/° K, $T$ is the temperature in° K, $P_{out}$ is the output signal power of VCO in $W$, $f_c$ is the flicker noise corner frequency in Hz, $K_{VCO}$ is the gain of VCO in Hz/V and $V_m$ total amplitude of all low frequency noise sources in V/$\sqrt{}$Hz.

Thus, the phase noise of VCO using SiGe device is supposed to be better because the $f_c$ and NF of SiGe process are lower than those of silicon process[1]. Fig. 9 shows the frequency pushing of the VCO. The graph indicates that oscillation stops below 2 V and above 5 V supply voltage. Also, we can see that the VCO could be used in PCS band at 4 V supply voltage. In Fig. 10, we obtained a tuning range of 1795 MHz~1910 MHz as biased to two varactor diodes from 0 V to 3 V. The output powers of the VCO are −9.3 dBm at 1795 MHz and −11.7 dBm at 1910 MHz. Those measured power levels are lower than the simulated ones by 4 dB. It was found out that about 1 dB loss was due to coaxial cable and connector.

## V. Conclusion

A 1.8 GHz fully differential monolithic HBT VCO has been designed and fabricated using a commercial 0.5 $\mu$m SiGe BiCMOS process technology. The manufactured chip size of VCO is 1246×1649 $\mu m^2$. The VCO achieved a low phase noise of −110 dBc/Hz at 100 kHz offset carrier and a third harmonic suppressionof more than 22 dBc. The tuning range of the VCO
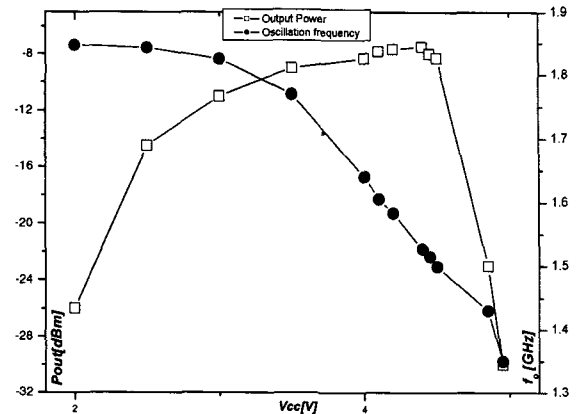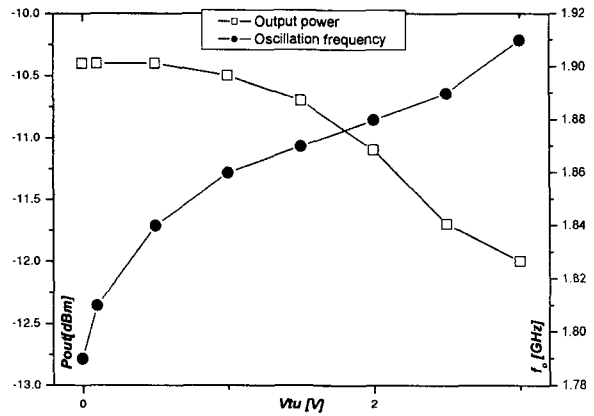


Fig. 9. Frequency Pushing.



Fig. 10. Tuning Range.

was 1795 MHz~1910 MHz as the output power levels were varied from −9.3 dBm to −11.7 dBm including about 1 dB of cable and connector losses. The VCO consumed 16 mA at 3 V supply voltage. The fabricated SiGe VCO showed good phase noise performance.

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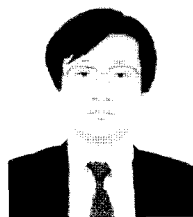
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