Cascode Low Noise Amplifiers with Coplanar Waveguide Structure for Wireless LAN Application

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Abstract

In this paper, low noise amplifiers with coplanar waveguide structure are presented for Wireless LAN data communication application. For comparison of microwave performance, LNAs of cascode type and balanced type using cascode cell with the same substrate and same bias conditions are designed and implemented. A cascode type of LNA shows the gain of 12.45 dB, input return loss of 11.63 dB, and noise figure of 1.52 dB. A balanced type of LNA using cascode cell shows the gain of 6.58 dB, input return loss of 16.6 dB, and noise figure of 1.18 dB.

Key words : CPW, Cascode Cell, LNA, Balanced Type.

Ⅰ. Introduction

Recently, the demand of small size and high performance in wireless communication systems leads to active research in the area on the HMIC(hybrid microwave integrated circuits) and MMIC(monolithic microwave integrated circuits).

In development of the HMIC and MMIC, back metal ground has been used in microstrip structure. Although microstrip is the most widely used planar transmission lines for circuit design, uniplanar transmission lines such as CPW, slotline, and coplanar strip have been introduced as alternative elements.

Some drawbacks for microstrip include sensitivity to substrate thickness, difficulty of inserting shunt solid-state device, and the requirement of high impedance lines for dc biasing. Coplanar waveguide has small diserpersion, simple realization of short-circuited end, the possibility of simple integration of lumped elements or active components, and circumventing the need for via holes. These characteristics make CPW be an important transmission line structure in microwave and millimeter-wave integrated circuit design.

LNA is one of the most important parts of the receiver in wireless communication systems.

In this paper, CPW LNAs with cascode cell are designed, fabricated, and measured for wireless LAN communication application.

Ⅱ. Cascode Topology

A cascode amplifier is composed of a common-source amplifier and a common-gate amplifier in cascade. Fig. 1 shows a simplified schematic for a cascode amplifier.

The cascode topology has a major advantage, in which current consumption is minimized because both transistors are located in the same drain current path. Due to this current re-use, the cascode LNA consumes half the power compared to that of two-stage cascade LNA[1].

The cascode structure has been considered to be the best topology for an integrated low noise amplifier because it can satisfy requirements for both noise and power gain simultaneously. In order to achieve high receiver sensitivity, the LNA is required to have not only low noise figure but also high gain and low input VSWR(Voltage Standing Wave Ratio).

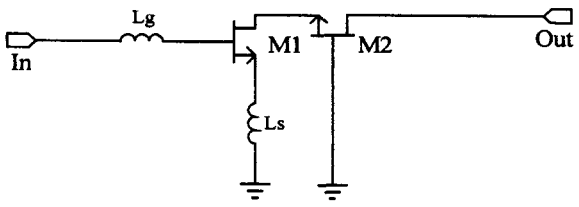

Fig. 1. Schematic for a cascode LNA.

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The cascode LNA can be considered as a two-stage amplifier. The input impedance of the first stage is given by

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs1}} + R_g + \frac{g_{m1}}{C_{gs1}} L_s \quad (1)$$

where g_{m1} and C_{gs1} are the transconductance and the gate-to-source capacitance of M_1 in Fig. 1, respectively. L_g and L_s are the gate inductance and the source inductance, which are estimated by ignoring Miller effect of the capacitance between the gate and drain, C_{gd1} of M_1. Also, R_g is the effective gate resistance, which can also be included in the parasitic series resistance of L_g. The input matching criteria give the following equations:

$$L_S = \frac{(R_s - R_g) C_{gs1}}{g_{m1}}, \quad (2)$$

$$L_S = \frac{1}{\omega_0^2 C_{gs1}} - L_s, \quad (3)$$

where R_s is the source resistance (50 Ω) and ω_0 is the operating frequency[2]~[4].

Ⅲ. CPW LNA Design

For comparison of microwave performance, two types of CPW LNAs are implemented with the same substrate of dielectric constant($\varepsilon_r = 10.2$, $h = 0.635$ μm) and the same bias condition($V_{ds} = 3$ V, $I_{ds} = 10$ mA).

3-1 Cascode-type CPW LNA

Fig 2 shows the layout of the designed CPW type cascode LNA. Since the width of slot line as well as the width of center-line should be considered to determine the characteristic impedance in CPW structure, it is difficult to decide the suitable width of the CPW in hybrid circuit design environment. For C-band LNA implementation in dielectric substrate, the simulation tool, IMST COPLAN™ for ADS ver. 1.3. has been used for the design. DC bias circuit is difficult to realize in CPW structure. Therefore, in this paper, CPW dc bias circuit is tried to construct by adjusting the width of slot and center-line for impedance variation. For RF block, the impedance is realized as $\lambda/4$ short line of 120 Ω and open line of 30 Ω[5].

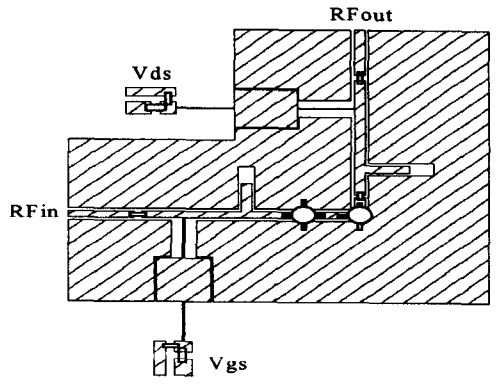
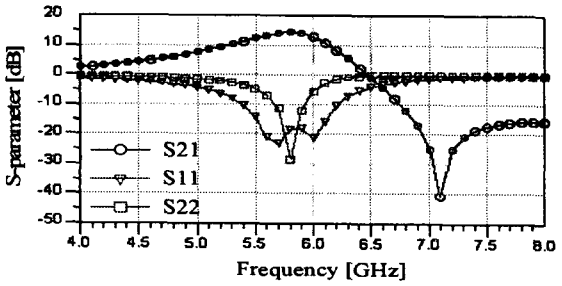


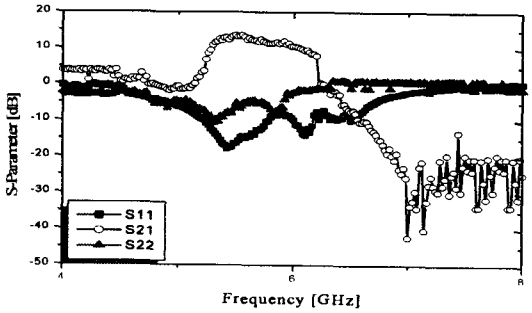
Fig. 2. Layout for the cascode-type CPW LNA (4.5 cm × 4.5 cm).

The cascode-type of LNA is designed using two Agilent GaAs MESFETs, ATF-26884. The bias conditions are $V_{ds} = 3$ V, $V_{gs} = -0.7$ V, and $I_{ds} = 10$ mA.

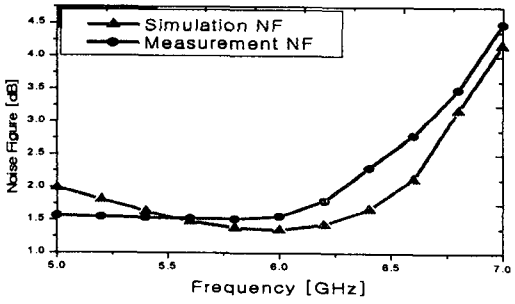
Fig. 3 shows the simulation and measurement results for the cascode-type CPW LNA.



(a) S-parameters(simulation)



(b) S-parameters(measurement)



(c) Noise figure

Fig. 3. Simulation and measurement results for the cascode-type CPW LNA.

From the figure, the measurement results for the S-parameters and noise-figure agree well with the simulation data while the data of measurement are a little worse than those of simulation. These differences between the simulation and the measurement are due to the process margin for making the circuit and due to imperfect analysis for discontinuity of CPW. The cascode-type CPW LNA shows the gain of 12.45 dB, input return loss of 11.63 dB, and noise figure of 1.52 dB in desired frequency range.

3-2 Balanced-type CPW LNA with Cascode Cell

Critical requirements on RF system applications are the size, weight, dc power, cost of RF modules, and subsystem assemblies. In addition, the module or system such as the receivers and transmitters are very expensive, heavy, large in size, necessary for more dc power, and complex for integration of system, which ultimately translate into high cost. Therefore, a balanced LNA with cascode cell is suggested in order to achieve dc power savings and eliminate the system complexity and size. For current-efficient operation, the current-shared biasing approach is suggested and shown in Fig. 4[6],[7].

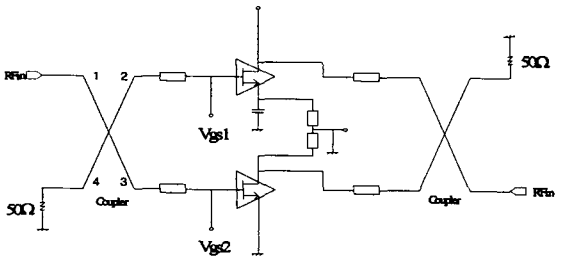


Fig. 4. Schematic diagram for the balanced-type LNA with cascode cell.

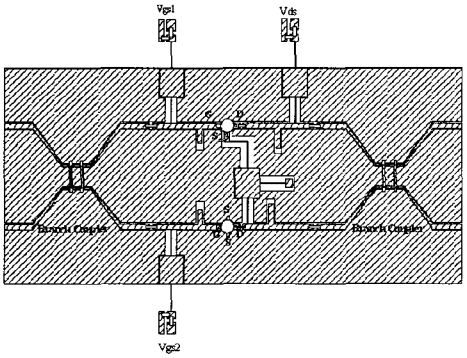
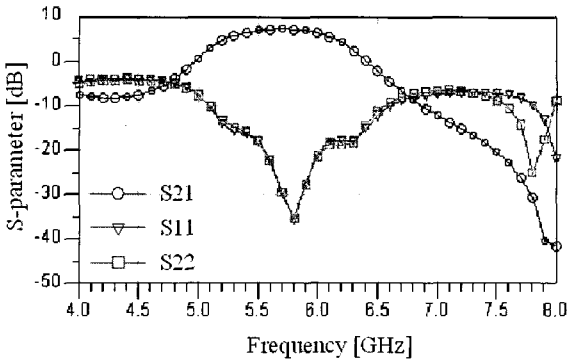
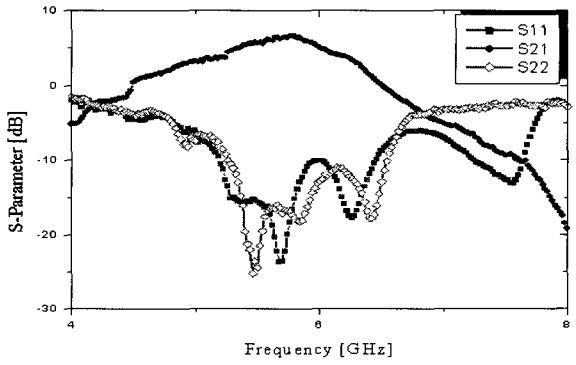


Fig. 5. Layout for balanced-type CPW LNA with cascode cell(12.5 cm × 6 cm).

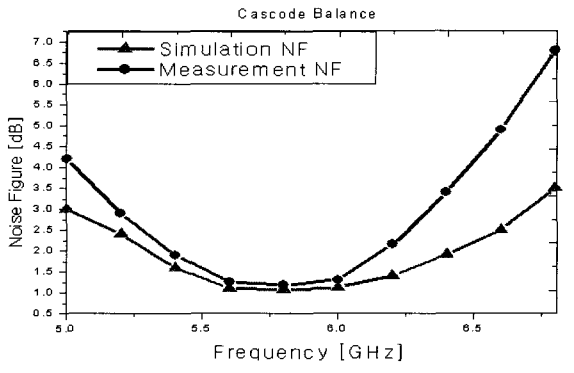
From the dc point of view, the transistors appear to be connected in cascode, that is, the source of one transistor is connected to the drain of another transistor, with sharing the same bias current. From an RF standpoint, both stages appear to be common-source amplifiers. Fig. 5 shows the layout of CPW balanced-type LNA with cascode cell. The CPW balanced-type LNA with cascode cell is designed using two Agilent GaAs MESFETs ATF-26884. The bias conditions are $V_{ds} = 3$ V, $V_{gs1} = 0.73$ V, $V_{gs2} = -0.78$ V, and $I_{ds} = 10$ mA.



(a) S-parameters(simulation)



(b) S-parameters(measurement)



(c) Noise figure

Fig. 6. Simulation and measurement results for the balanced CPW LNA with cascade cell.

Table 1. The characteristics of the two types of CPW LNAs.

Items	Cascode LNA		Balanced cascode cell LNA	
	Sim.	Meas.	Sim.	Meas.
Center Frequency [GHz]	5.8	5.8	5.8	5.8
ε_r	10.2	10.2	10.2	10.2
Conductor Thickness [μm]	18	18	18	18
Substrate height [mm]	0.635	0.635	0.635	0.635
Current Consumption [mA]	10	10	10	10
Gain [dB]	14.36	12.45	7.25	6.58
Noise Figure [dB]	1.38	1.52	1.03	1.18
Bandwidth [MHz]	120	120	120	120
Gain Flatness [dB]	$\pm$0.1	$\pm$0.5	$\pm$0.01	$\pm$0.25

Fig. 6 shows the simulation and measurement results of the balanced-type CPW LNA with cascode cell. From the figures, the measurement results for the S-parameters and noise-figure agree well with the simulation data. The gain of the implemented LNA is 6.58 dB, input return loss is 16.6 dB, and noise figure is 1.18 dB as shown in Fig. 6.

The characteristics of the CPW LNAs are summarized in Table 1.

Ⅳ. Conclusion

In this paper, CPW low noise amplifiers have been demonstrated for Wireless LAN application. For comparison of microwave performance, two types of LNAs have been implemented on the same substrate and bias conditions with the supply voltage(V_{ds}) of 3 V and current consumption of 10 mA. The CPW cascode-type of LNA shows high gain characteristic because of the same current operations for two active devices while not a good noise figure and gain flatness. Implemented balanced LNA with cascode cell has characteristics of low noise figure and excellent gain flatness. In this balanced type of CPW LNA with cascode cell, the half current consumption can be obtained compared with the case in general single stage balanced amplifier. Also, it shows good input/output VSWRs, good stability, and high reliability[8].

The CPW LNAs suggested in this paper are expected to be used not only in mm-wave range but also commercial frequency range because of the size reduction, easy fabrication, and the possibility of integration with MMIC.

References

[1] B. K. Ko. *Circuit Design Techniques of Monolithic Microwave Low Noise Amplifiers*, Ph. D. dissertation, Dept. of Elec. Eng., Korea Adv. Inst. Sci. Technol., Taejeon, Korea, 1997.

[2] D. K. Shaeffer, T. H. Lee, "A 1.5 – V, 1.5 – GHz CMOS Low Noise Amplifier", *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745-749, May 1997.

[3] Q. Huang, P. Orsati and F. Piazza, "Broadband, 0.25 μm CMOS LNAs with Sub-2 dB NF for GSM Applications", *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 67-70, 1998.

[4] A. Parssinen, S. Lindfors, J. Ryynanen, S. I. Long and K. Halonen, "1.8 GHz CMOS LNA with on-chip DC-Coupling for a Subsampling Direct Conversion Front-end", *Proc. IEEE Int. Symp. on Circuits and Systems*, vol. 2, pp. 73-76, 1998.

[5] P. C. Hsu, C. Ngugyn and M. Kintis, "Uniplanar Broadband Push-Pull FET Amplifiers", *IEEE Trans. Microwave Theory Tech.*, vol. 45, no. 12, pp. 2105-2152, Dec. 1997.

[6] K. W. Kobayashi, L. T. Tran, "A 44-GHz High IP3 InP-HBT Amplifier with Practical Current Reuse Biasing", *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 1237-1241, Dec. 1998.

[7] K. W. Kobayashi, L. T. Tran, J. Cowles, T. R. Block, A. K. Oki and D. C. Streit, "Low DC Power High-Gain-Bandwidth Product InAlAs/ InGaAsInP HBT Direct-Coupled Amplifiers", *IEEE GaAs IC Symp. Dig.*, pp. 141-144, 1996.

[8] S. Y. Liao, *Microwave Circuit Analysis and Amplifier Design*, Prentice Hall, 1987.

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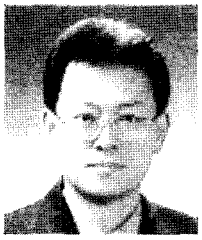

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