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Measurement and Simulation Study of RSFQ OR gate

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Abstract-- **There are several simulation programs in studying superconductor RSFQ (Rapid Single Flux Quantum) electronic devices, which include WRspice, WinS, PSCAN, and JSIM. Even though different research groups use different simulation programs, it is not well known about which program gives the simulation results closer to the measurement values. In this work, we used both WRspice and WinS to simulate RSFQ OR gate and to compare the results from the different simulations. This comparison would help in deciding which program is better in the RSFQ circuit design. In the confluence buffer, which is the one of the main components of the OR gate, the measured bias margins were ±23.2%, while the margins from the simulations were ±35.56% from WRspice and ±53.1% from WinS. However, with the actual fabricated circuit parameters WRspice gave ±27%. In WinS the circuit did not operate. We concluded that WRspice is more reliable.**

1. Introduction

We often use several kinds of simulation tool for the superconductive electronics deice development. However, the designers always wonder if the fabricated devices may behave as they did in simulations. In this work, various simulation results were compared with the measurement results to find the good simulation tool for our work. In this work, we used WRspice and WinS to compare the simulation results, by applying these programs in simulating an RSFQ OR gate.

2. Simulations of an OR gate

The circuit diagram of an OR gate is as shown in Fig. 1 [1]. The circuit was composed of a Confluence buffer and an RS flip-flop [2], [3]. Simulated transient behavior of the OR gate is shown in Fig. 2, where the normal operation of the OR gate can be seen [2]. Whenever there is an input from either IN 1 or IN 2, we observed an output from the designed OR gate.

The normal operation of the OR gate is obtained from the proper pulsing of the Josephson junctions and the proper storage of SFQ pulses in the inductors. Through the confluence buffer, an input from IN 1 enters to the RS flip-flop. The path of the input pulse from IN 1 to arrive at the RS flip-flop is B8-L7-B10-L12-L13-B7-L14 Input pulse from IN2 follows the path of B9-B11-L12-L13-B7-L14. The confluence buffer just adds the SFQ pulses from IN 1 and IN 2 without altering the data unless they coincide.

SFQ pulses from the confluence buffer is saved in the RS flip-flop through the path of LCT41-B6-BTT22-LTTIN. Subsequent clock pulse may pulse the junction BITS and emits an output pulse to L5.

In the circuit diagram, as shown in Fig. 1, buffer junctions are shown as B10 and B11 in the confluence buffer and B6 in the RS flip-flop. Buffer junctions play a role in the operation of devices to prevent the counter-flows.

In this work, we attempted to find the common device parameters and then find the margins to compare the two simulators. However, the circuit constructed with the optimum device parameters obtained from WRspice

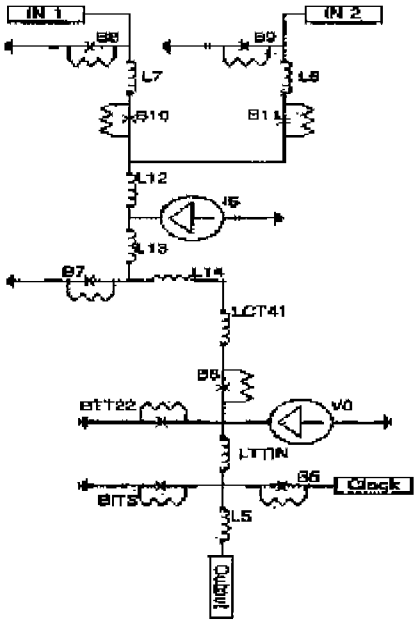

Fig. 1. OR gate circuit diagram.

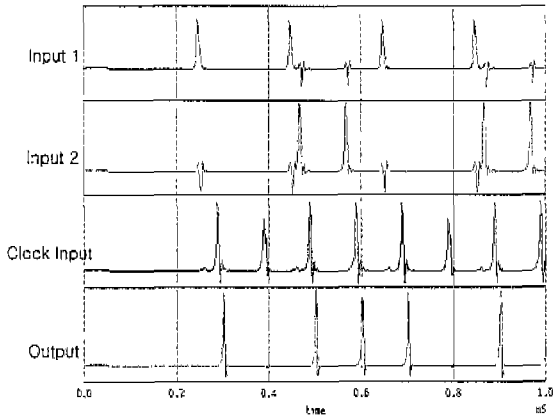

Fig. 2. Simulation result of OR gate circuit.

simulator did not work with WinS simulator [4], [5]. Therefore, we had to reoptimize the circuit by using WinS. With their own optimized circuits we calculated the margins and the results were compared.

To perform the circuit simulations with WRspice, first we have to design the circuit with Xic program that converts the designed circuit to a spice file [4]. In this way, we can confirm the proper operation of the circuit and find the optimal parameters.

Since WRspice does not support the automatic optimization process we have to find the optimum device parameters by repeatedly replacing with new values. We have performed this process for an OR gate, and the results are shown in Table 1. The best results obtained in this way gave the margins of over ±35%.

WinS program can support the circuit design and the circuit simulation at the same time. First, we design a circuit and assign the device parameters in "Schematic Editor". After finishing the circuit design we simulate the circuit with the functions in "Analysis" menu.

There is a similarity in simulating the circuits with WinS and with WRspice. Only WinS has the "Optimize" function that searches automatically the best values of the device parameters. WRspice does not have this function. Therefore, finding the optimum device parameters are much easier in using WinS than using WRspice. In WinS, the margins are expressed with only percentage values, which then have to be manually converted to the device parameter values. Also when the margins are over ±90%, it only expresses as ±90%.

Due to these problems the correct device parameter values are not easy to obtain in some cases. When the maximum and the minimum margin width are ± 90%, the maximum and the minimum margin widths as shown in Table 2 may not be the true maximum value and the true minimum value. If we simulate th e circuits by using WinS, we have to interpret the results very carefully.

TABLE I Margins of OR gate optimized with WRspice.

Device Name	Center	(-) Value	(+) Value	(-) %	(+) %
B7	0.24	0.00	0.47	100.00	95.83
B8	0.22	0.00	0.63	100.00	186.36
B9	0.22	0.00	0.65	100.00	195.45
B10	0.18	0.04	1.15	77.78	538.89
B11	0.18	0.04	0.31	77.78	72.22
L6	0.60	0.00	Very High	100.00	Very High
L7	0.60	0.00	Very High	100.00	Very High
L12	0.40	0.00	6.20	100.00	1450.00
L13	2.53	0.00	6.20	100.00	145.06
L14	1.00	0.00	11.00	100.00	1000.00
I6	0.45	0.26	0.61	42.22	35.56
B5	0.25	0.11	0.37	56.00	48.00
B6	0.24	0.06	Very High	75.00	Very High
BTT22	0.24	0.00	0.38	100.00	58.33
BITS	0.20	0.00	0.34	100.00	70.00
LCT41	2.60	0.00	12.37	100.00	375.77
LTTIN	8.50	1.68	20.50	80.24	141.18
L5	3.20	1.00	Very High	68.75	Very High
V0	2.50	0.70	4.60	72.00	84.00

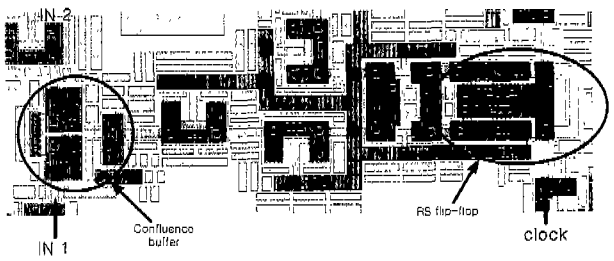

Fig. 3. Mask layout of the OR gate.

From the simulation results shown in Table 2 we can see that the circuit margins are more than ±29%.

3. Measurements

Based on the existing confluence buffer and RS flip-flop, we laid out the OR gate as shown in Fig, 3 [6]. The circuits were fabricated by using the ten-level Nb process with junction critical current density of 2.5 kA/cm^2 [7].

24-pin high-speed probe was used to measure the fabricated chips immersed into the liquid helium. Multi-channel stable current sources were used to bias the circuits and an 8-channel oscilloscope was used to monitor the various inputs and outputs. A function generator was used to produce an input signal and an oscilloscope was used to monitor the outputs of the circuit. The measurement was performed at the liquid

helium temperature. The test speeds of 10kHz and 1MHz were selected, limited by the bandwidth of the oscilloscope.

The block diagram of the test setup, including the paths of the SFQ pulses in the circuit is as shown in Fig.

TABLE II Margins of OR gate optimized with WinS.

Device Name	Center	(-) Value	(+) Value	(-) %	(+) %
B7	0.2400	0.0425	0.3970	82.30	65.40
B8	0.1594	0.1084	0.2378	32.00	49.20
B9	0.1778	0.1259	0.2347	29.20	32.00
B10	0.1800	0.0180	0.3420	90.00	90.00
B11	0.2392	0.1459	0.4545	39.00	90.00
L6	0.2160	0.0216	0.4104	90.00	90.00
L7	0.6000	0.0600	1.1400	90.00	90.00
L12	0.6000	0.0600	1.1400	90.00	90.00
L13	2.6565	0.3400	5.0474	87.20	90.00
L14	1.0000	0.1000	1.9000	90.00	90.00
I6	0.1700	0.0666	0.2603	60.80	53.10
B5	0.1900	0.1125	0.3610	40.80	90.00
B6	0.2400	0.0806	0.4560	66.40	90.00
BTT22	0.1800	0.0180	0.3420	90.00	90.00
BITS	0.2400	0.0418	0.3742	82.60	55.90
LCT41	2.6000	0.2600	4.9400	90.00	90.00
LTTIN	5.6000	0.5600	10.6400	90.00	90.00
L5	5.6000	0.5600	10.6400	90.00	90.00
V0	2.5	0.2500	4.3375	90.00	73.50

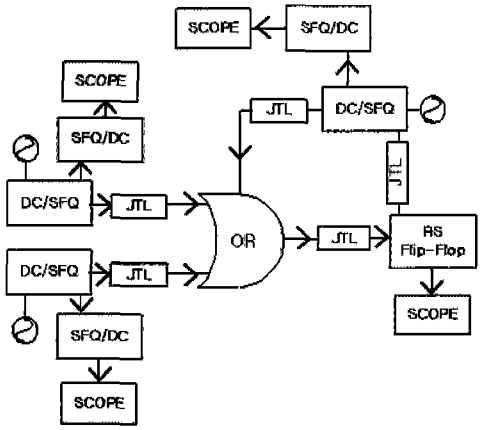

Fig. 4. Diagram of OR gate for measurement.

4. The measured circuit included DC/SFQ circuits, SFQ/DC circuits, and an RS flip-flop type readout circuit in addition to the OR gate. A DC/SFQ circuit was used to produce data pulses feeding to the OR gate. An SFQ/DC circuit was used to monitor if the correct SFQ pulses are generated from the DC/SFQ circuits. Two DC/SFQ circuits connected to the external function generators were used to produce the input pulses to feed into the OR gate. The clock pulses were generated with a DC/SFQ circuit connected to a function generator and was fed into the OR gate and the RS flip-flop type readout circuit. The clock pulses were used to read the output of the OR gate and the RS flip-flop type readout circuit and also to reset the circuits. Compared to the T flip-flop type readout circuits, the RS flip-flop type readout circuit is more convenient to measure the logic circuits.

Fig. 5 and Fig. 6 show the scope traces obtained in the OR gate measurements. Fig. 5 shows the measurement results at 10 kHz, and Fig. 6 shows the results at 1 MHz. The tests at higher frequencies were not possible because of the bandwidth limitations set by the oscilloscope. In Fig. 5 and Fig. 6, the first two traces show the input patterns, the third the clock pulses, and the fourth the output pattern. The output pulse exists when either IN 1 or IN 2 was "1," or both inputs were "1." From the measurements we found that the confluence buffer had the bias current margin of 23.2% and the RS flip-flop had the bias current margin of 38.6%.

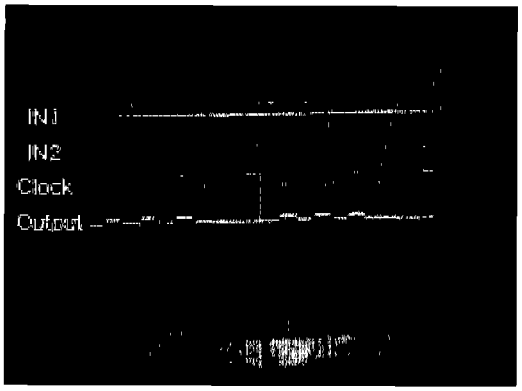

Fig. 5. Measurement of SFQ OR gate using oscilloscope and arbitrary waveform generator at 10kHz.

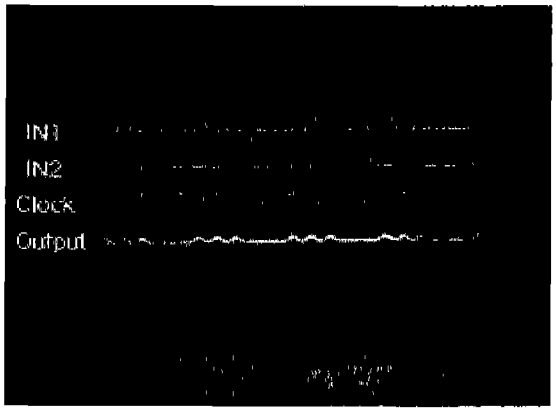

Fig. 6. Measurement of SFQ OR gate using oscilloscope and arbitrary waveform generator at 1MHz.

From the series array made in the chip we estimated the junction critical values. These data are as shown in the Table 3, along with the inductance values from the circuit layout.

Table 4 shows the comparison of the simulated bias current values and the measured bias current values. With their own optimized circuit parameters, the bias

margins obtained from the WRspice simulations was 35.6% for the confluence buffer while the bias margins from the WinS simulation was 53.1%, as shown in Table 1 and Table 2. However, when we inserted the circuit parameters obtained from the fabricated circuit values the bias margins have changed. Compared to the margins of ±23.2% in measurements, the margins of ±27% in WRspice simulations were in good agreement. However,the circuit did not operate in WinS simulations, even though the margins from WinS program was the largest with its own optimized circuit parameters.

TABLE Ⅲ Circuit parameters of the fabricated OR gate.

Cell name	device name	value
confluence buffer	B7	0.34 mA
	B8	0.34 mA
	B9	0.34 mA
	B10	0.24 mA
	B11	0.24 mA
	L6	0.6 pH
	L7	0.6 pH
	L12	0.5 pH
	L13	0.6 pH
	L14	1 pH
	I6	0.69 mA
RS flip-flop	B5	0.3 mA
	B6	0.3 mA
	BTT22	0.3 mA
	BITS	0.3 mA
	LCT41	1 pH
	LTTIN	4.5 pH
	L5	1 pH
	V0/R	0.27 mA

TABLE Ⅳ Bias current comparison between the measurements and the simulations. "-" means that the circuit did not operate and "( )"means values of simulation.

		Confluence buffer
Measurements	Center(mA)	0.69
	(-) %	23.2
	(+) %	23.2
WRspice Reasults	Center(mA)	0.67 (0.45)
	(-) %	27 (42.22)
	(+) %	27 (35.56)
WinS Reasults	Center(mA)	- (0.17)
	(-) %	- (60.80)
	(+) %	- (53.10)

3. Conclusions

Various simulation programs have their own advantages and disadvantages in designing superconductive electronics circuits. In this work, we WRspice simulations and WinS simulations to the compared the bias current values obtained from the values from the measurements. We concluded that the results obtained with WRspice simulations are more reliable than the ones from WinS.

Acknowledgment

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