A New EST with Dual Trench Gate Electrode (DTG-EST)

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In this paper, the new dual trench gate Emitter Switched Thyristor (DTG-EST) is proposed for improving snap-back effect which leads to a lot of serious problems of device applications. Also the parasitic thyristor that is inherent in the conventional EST is completely eliminated in this structure, allowing higher maximum controllable current densities for ESTs. The conventional EST exhibits snap-back with the anode voltage and current density 2.73V and 35A/㎠, respectively. But the proposed DTG-EST exhibits snap-back with the anode voltage and current density 0.96V and 100A/㎠, respectively.

Keywords : Dual trench gate, EST, Snap-back effect, Parasitic thyristor, FBSOA

1. INTRODUCTION

The advent of MOS-gated power devices has had a tremendous impact on Power Electronic Applications, such as motor control. Especially, The Insulated Gate Bipolar Transistor (IGBT) [1-5] is the most widely used device for this application, but this device has on-state voltage drop of over 3.5 V. For this reason, MOS-gated thyristor based devices are of great interest due to their low forward voltage drop and high input impedance. The MOS-Controlled Thyristor (MCT), the Base Resistance controlled Thyristor (BRT), Emitter Switched Thyristor (EST) [6-10] are MOS-gated devices that use a thyristor to carry the forward current.

Among the various MOS gated thyristors, The EST has the unique feature of gate controlled current saturation of the thyristor current and can be fabricated with the double diffused MOS process used to make power MOSFETs and IGBTs. The dual channel emitter switched thyristor (DC-EST) is only three terminal devices that exhibits the high voltage current saturation characteristics essential to replace the IGBT in medium/high power applications. And a good forward bias safe operating area (FBSOA) is desirable in a power device to perform gate controlled turn-on and turn-off. The DC-EST has been shown to possess a better FBSOA than the IGBT.

In this paper, we proposed a new DTG-EST with dual trench gate electrodes for improving FBSOA and forward blocking characteristics. Numerical simulations on the latch-up characteristics of the proposed DTG-EST are shown in comparison with that of the conventional EST at the same size.

2. DEVICE STRUCTURE AND OPERATION

A cross-section view of the conventional EST and the proposed dual trench gate EST (DTG-EST) is shown in Fig.1a, Fig.1b, respectively. The main difference between the conventional EST and the proposed DTG-EST is the placement of the cathode and gate electrode and is the position of the turn-off and turn-on MOSFET. The emitter switched thyristor (EST) is a device in which the on-state current flows via a thyristor region.

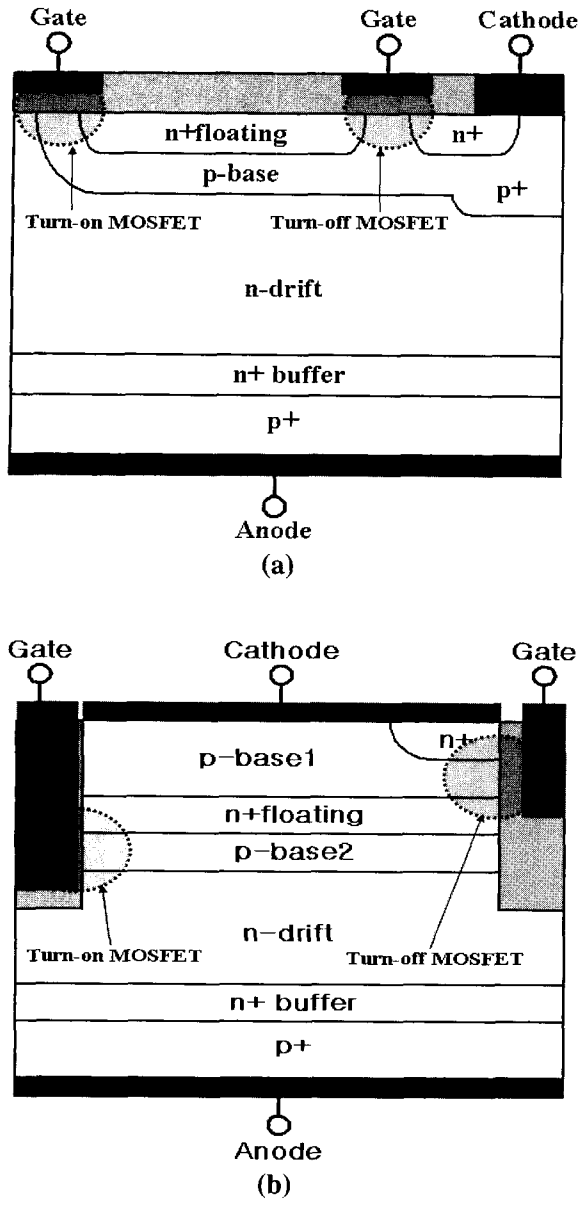


Fig. 1. Cross-section view of (a) the conventional EST and (b) the proposed DTG-EST.

But, in this device, the n+ emitter of the thyristor is not directly connected to the cathode electrode. Instead, the thyristor emitter forms the drain region of a turn-off MOSFET which is integrated into the p-base region of the thyristor.

In the proposed structure, a turn-off MOSFET is integrated in series with the thyristor formed between the p+ anode and n+ floating. Turn-off MOSFET is formed between n+ cathode and n+ floating, turn-on MOSFET is formed between n+ floating and n-drift. And the gate oxide thickness of turn-on MOSFET is 0.05 μm in order to latch up main thyristor at the low voltage, the gate oxide thickness of turn-off MOSFET is 0.2 μm for improving current saturation characteristics of unique feature in the EST. Also the p-base 2 region is shorted to the p-base1 region in the third dimension. It is important to note that by using the dual trench gate the parasitic thyristor that is inherent in the conventional EST is completely eliminated in the proposed DTG-EST.

With zero gate bias, the device operates in the forward blocking mode and the junction formed by the p-base 2 and the n-drift regions supports any applied positive anode voltage. The proposed structure can be turned-on by applying a positive potential to the dual trench gate while the anode is kept positive with respect to the cathode. A positive voltage on the gate causes an inversion layer region to form both in the p-base 1 region of the turn-off MOSFET and the p-base 2 region of the turn-on MOSFET. The inversion channel allows electrons to flow from the cathode through the channel into the n-drift region. And these electrons provide the base drive current for the vertical P-N-P transistor formed between the p+ anode as the emitter, the n-drift region as the base, and the p-base 2 region as the collector. In response to the base drive current, the holes injected from the anode are collected by the reversed biased junction formed between the p-base 2 and n-drift region. The holes collected by the p-base 2 flow under the n+ floating into the cathode in the third dimension. Under these conditions the EST operates like a trench IGBT. At higher current levels the hole current flowing under the n+ floating forward biases the junction formed by n+ floating and p-base 2, the thyristor latches up. Since the thyristor current is constrained to flow through the turn-off MOSFET, gate control over the thyristor current can be established. It is important to note that by reducing the gate voltage the thyristor current can be saturated. The maximum voltage to which the thyristor current can be saturated is limited by the breakdown of the turn-off MOSFET. A high maximum controllable current can be achieved in this structure due to the absence of the parasitic thyristor.

3. SIMULATION AND RESULT

3.1 Forward I-V characteristics

The forward I-V characteristics of two devices were obtained through two-dimensional numerical simulations using MEDICI.

Simulations were performed using the device structures in Fig.1a, Fig.1b and the device parameters of the proposed DTG-EST in Table1.

Table 1. Device parameters of the proposed DTG EST used in the simulations.

	Depth/thickness (μm)	Concentration (cm^{-3})
Gate Oxide Thickness	0.05 (left), 0.2 (right)	-
Trench depth of gate	10 (left), 5.5 (right)	-
Cell width	40	-
n+ cathode layer	0.1	10^{21}
p-base1 layer	5	10^{16}
n+ floating layer	1	10^{20}
p-base2 layer	2	10^{16}
n-drift layer	56	10^{13}
n+ buffer layer	3	10^{16}
p+ anode layer	3	10^{21}

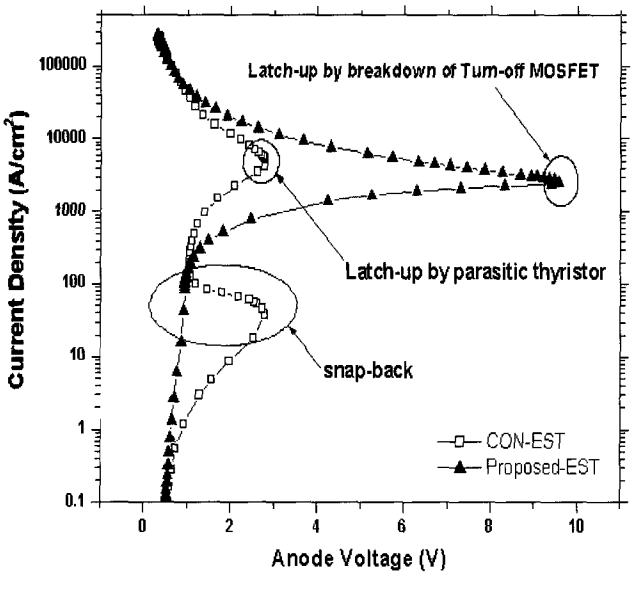


Fig. 2. Forward conduction characteristics of the conventional EST and the proposed DTG-EST (Vg=20V).

In Fig. 2, the simulated I-V characteristic of the proposed DTG-EST is compared with that of the conventional EST. It can be seen from this figure that the proposed DTG-EST has superior characteristics as compared to conventional EST. Snap-back effect is completely eliminated in this structure. And saturation current density of the proposed DTG-EST at anode voltage 9.6 V is 2388 A/㎠.

In the conventional EST, a large n+ floating length is required to the reduced the latching and holding currents. But this increases the current flowing through the lateral MOSFET and consequently increases the forward voltage drop across the MOSFET. In the proposed DTG-EST, the latching current is determined by the n+ floating width in the third dimension. This reduces the current flowing through the trench MOSFET. And the gate oxide thickness of turn-off and turn-on MOSFET is not equal. As the gate oxide thickness of turn-on MOSFET is 0.05 μm, the main thyristor latches up at the low voltage, which is compared with the conventional EST. Consequently, snap-back effect is completely eliminated in the proposed DTG-EST. Thus, the forward voltage drop is very low. The gate oxide thickness of turn-off MOSFET is 0.2 μm for improving current saturation characteristics of unique feature in the EST. Therefore a high maximum controllable current can be achieved in the proposed DTG-EST.

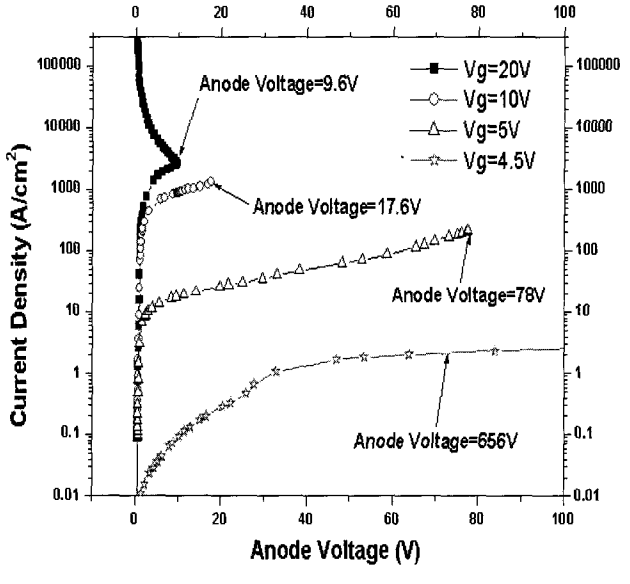
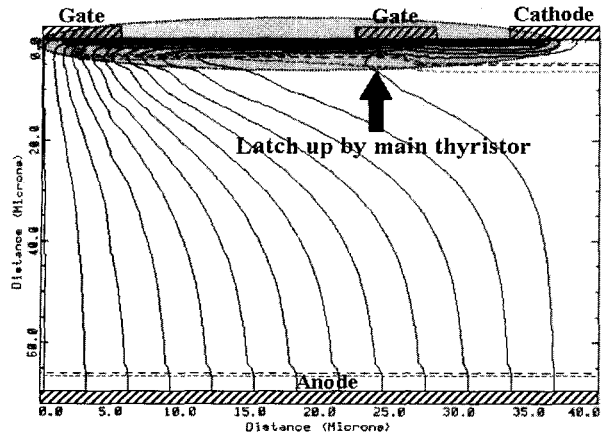


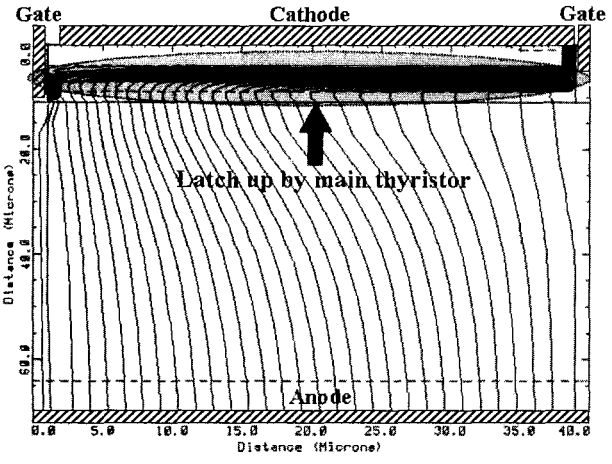
Fig. 3. Forward conduction characteristics of the proposed DTG-EST for different gate biases.

Figure 3 is the forward I-V characteristics of proposed DTG-EST with different gate bias. It is observed that high voltage saturation current is possible in the proposed DTG-EST.

Figure 4(a) and Figure 4(b) are the flow line of conventional EST and proposed DTG-EST for a gate bias 20V when main thyristor are operating properly. From these figures it can be seen that the dual trench gate allows vertical current flow resulting in a uniform current distribution across the device. And Fig.5a is the flow line of conventional EST when parasitic thyristor latches up. But Fig.5b is the flow line of the proposed DTG-EST for a gate bias 20V when breakdown of turn-off MOSFET occurs.



(a)

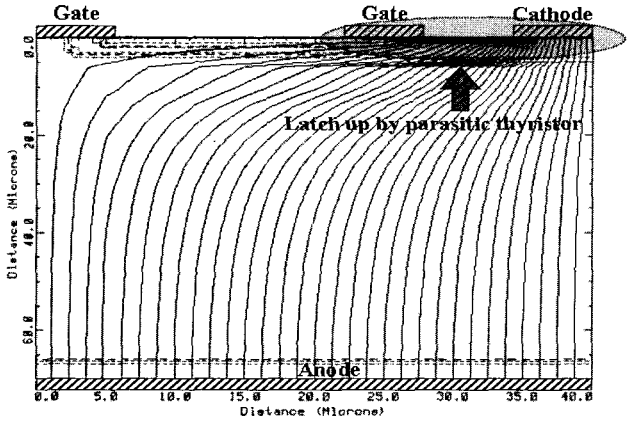


(b)

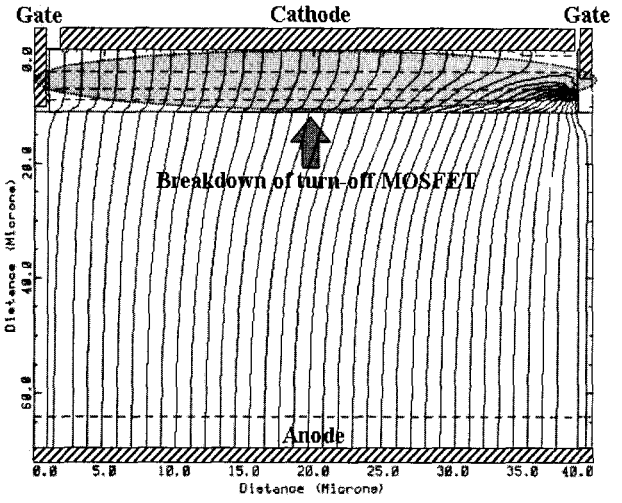
Fig. 4. Current flow line in the (a) conventional EST and (b) proposed DTG-EST (Vg=20V).

3.2 Forward Blocking Characteristics

The FBSOA (Forward Biased Safe Operating Area) of the proposed DTG-EST was investigated by increasing the anode voltage at zero gate bias. In Fig. 6,



(a)



(b)

Fig. 5. Current flow line when breakdown occurs (Vg=20V): (a) in the conventional EST and (b) in the proposed DTG-EST.

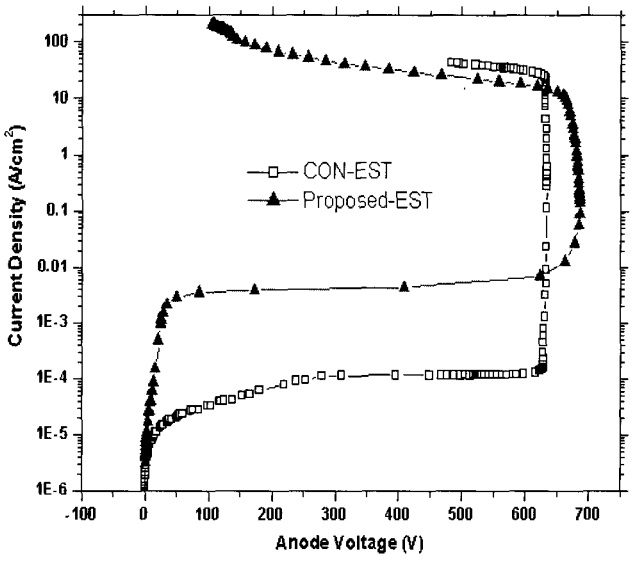


Fig. 6. Forward blocking characteristics of the conventional EST and proposed DTG-EST (Vg=0V).

the proposed DTG-EST has a higher blocking voltage than conventional EST. The three-dimensional electric field distribution of each device is illustrated in Fig. 7(a), Fig. 7(b). When the breakdown of the conventional EST occurs, the whole electric field is concentrated on channel region under gate electrode. But the electric field applied to the proposed DTG-EST is distributed throughout the n-drift region.

Consequently, the breakdown of the conventional EST occurred at the anode voltage of 620V and the breakdown of the proposed DTG-EST occurred at the

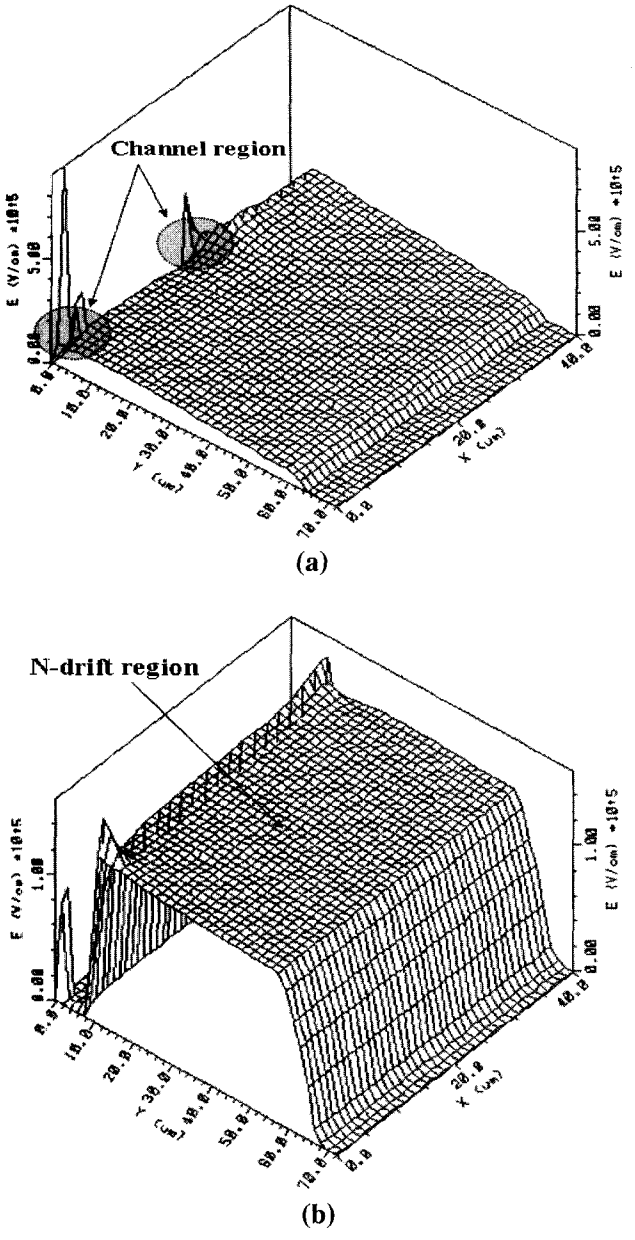


Fig. 7. The electric field distribution when the breakdown occurs (Vg=0V): (a) in the conventional EST and (b) in the proposed DTG-EST.

anode voltage 698 V. If trench oxide layer thickness of proposed DTG-EST is made thicker, a higher breakdown voltage is possible in the proposed DTG-EST.

4. CONCLUSION

A new Dual Trench Gate EST (DTG-EST) has been proposed in this paper. The snap-back effect is completely eliminated in this structure. As the saturation current voltage is higher with low gate bias, a high maximum controllable current can be achieved in the proposed DTG-EST. Also it is shown that high voltage saturation current capability is possible. In addition, it can maintain the higher safe operation region than the conventional EST.

ACKNOWLEDGEMENT

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