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통계적 실험계획 및 분석: Gate Poly-Silicon의 Critical Dimension에 대한 계층적 분산 구성요소 및 웨이퍼 수준 균일성

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Statistical Design of Experiments and Analysis: Hierarchical Variance Components and Wafer-Level Uniformity on Gate Poly-Silicon Critical Dimension

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Gate poly-silicon critical dimension is a prime characteristic of a metal-oxide-semiconductor field effect transistor. It is important to achieve the uniformity of gate poly-silicon critical dimension in order that a semiconductor device has acceptable electrical test characteristics as well as a semiconductor wafer fabrication process has a competitive net-die-per-wafer yield. However, on gate poly-silicon critical dimension, the complexity associated with a semiconductor wafer fabrication process entails hierarchical variance components according to run-to-run, wafer-to-wafer and even die-to-die production unit changes. Specifically, estimates of the hierarchical variance components are required not only for disclosing dominant sources of the variation but also for testing the wafer-level uniformity. In this paper, two experimental designs, a two-stage nested design and a randomized complete block design are considered in order to estimate the hierarchical variance components. Since gate poly-silicon critical dimensions are collected from fixed die positions within wafers, a factor representing die positions can be regarded as fixed in linear statistical models for the designs. In this context, the two-stage nested design also checks the wafer-level uniformity taking all sampled runs into account. In more detail, using variance estimates derived from randomized complete block designs, Duncan's multiple range test examines the wafer-level uniformity for each run. Consequently, a framework presented in this study could provide guidelines to practitioners on estimating the hierarchical variance components and testing the wafer-level uniformity in parallel for any characteristics concerned in semiconductor wafer fabrication processes. Statistical analysis is illustrated for an experimental dataset from a real pilot semiconductor wafer fabrication process.

Keywords: design of experiments, variance components, uniformity test, critical dimension, semiconductor

1. Introduction

1.1 Motivation

Semiconductor industry continues to pursue developing semiconductor devices (e.g. CPU, memory, logic, etc.) with shrunk device and interconnection dimensions in order to achieve a smaller die (i.e. semiconductor device chip) size, more rapid operating speed, lower electric power consumption and so forth. Based on the capability of a semiconductor wafer fabrication process (i.e. fab) as well as the limitation of device

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manufacturing technologies, a device design rule tends to specify a shorter length of gate poly-silicon for an integrated circuit (IC). Gate poly-silicon is a basic component consisting a transistor in an IC, so that the length of it is a critical transistor characteristic to be monitored in fabs.

Boynton *et al.* (1997) and Orshansky *et al.* (2000) show that the variation on the length of gate poly-silicon may have a serious impact on die loss due to unacceptable electrical test characteristics of transistors in a die. From a semiconductor wafer manufacturing point of view, net-die-per-wafer yield is one of the most important factors for the overall yield of a fab (Cunningham, 1990). Stine *et al.* (1997) decompose spatial variation in fabs and devices with the aim of process optimization as well as robust design of devices. In the paper, they focus more on wafer- and die-level spatial variation (e.g. wafer edge effects, circuit pattern or layout induced deviation), and present several models for the variation extraction based on statistical methodologies such as moving average, regression, etc.. Nassif (1998) discusses a within-die variation where two major sources of within-die variation are; 1) environmental source including electric power supply voltage and temperature; and 2) physical source like imperfections in device designs and fab processes. Badgwell *et al.* (1992) mention that wafer-to-wafer variation can be observed even in a single batch process.

Retajczyk and Larsen (1977) use a three-stage nested sampling plan to isolate variance components for contact window diameters into the sampling level components representing differences; 1) between runs (i.e. lots); 2) wafers within runs; and 3) within wafers. In the nested sampling plan, every five measurements are made at the same location on all wafers so that they can't test a wafer-level uniformity on the diameter. Garling and Woods (1994) also utilize a nested design of experiments so as to quantify epitaxial film thickness variations. In their paper, thickness measurements are taken at five standard positions across wafer, but they do not investigate whether there is a thickness difference according to positions. Regarding these two nested designs abovementioned, five runs are experimented to estimate run-to-run variation. Assuming a nested-random-effects model, Yashchin (1994) gives variance components estimation formulas for lot-to-lot, wafer-to-wafer and within-wafer variation associated with IC manufacturing. Based on the estimates, cumulative sum control charts are applied to monitoring the variance estimate sequences. Roes and Does (1995) also study the use of Shewhart-type control charts for fab process control, which uses a mixed model including a fixed factor for a wafer positioning effect in batch equipment, not for the wafer-level differences relating to positions within wafers. Besides, regarding design and analysis of experiments in manufacturing industries, statistical methodologies have been widely used for process and product optimization (Yin and Jillie, 1987; Hood and Welch, 1992; Antony, 2000).

1.2 Gate poly-silicon critical dimension

In a fab, gate poly-silicon is patterned during photolithography process. Major steps in photolithography process are; 1) application of resist; 2) resist exposure through a mask; 3) after development; and 4) after oxide etching and resist removal. Since photolithography is one of the bottlenecks in many fabs, extensive research focuses on this. Recently, Doniavi *et al.* (2000) consider a photolithography process optimization.

Metal-oxide-semiconductor field effect transistor (MOSFET) is a key component of present-day microelectronics, and gate poly-silicon is a basic element in MOSFET transistors. A typical MOSFET may have a planar structure with; 1) a thermally grown oxide layer functioning as the gate insulator; and 2) a surface-inversion channel and islands doped opposite to the substrate acting as the source and drain (Streetman, 1990). By a design rule, a transistor has its own nominal length of gate poly-silicon and the length of gate poly-silicon (i.e. L_{gate}) is critical to main features of a semiconductor device including size, speed and electric power consumption, etc.. Particularly, L_{gate} has a relationship with the saturation current (i.e. I_{Dsat}, an important electrical test characteristic of a transistor) as equation (1) (Pierret, 1996).

$$I_{Dsat} \propto \frac{1}{L_{gate}} \tag{1}$$

It is strongly demanded to achieve the uniformity on L_{gate} throughout all transistors in a die, so that inspection on L_{gate} is an inevitable fab step. Only a semiconductor device satisfying the specification on L_{gate} is regarded acceptable, and then passed to subsequent steps. In real fabs, as a terminology, a critical dimension (CD) designates an actual measurement of L_{gate} patterned inside a transistor. There are two different types of CDs; 1) after development inspection (ADI); and 2) after cleaning inspection (ACI). ACI CD is more influential to electrical test characteristics compared with ADI CD. In this paper, the term CD means ACI CD hereafter.

1.3 Statement of the problem

Research assumption: From the viewpoint of production units, a run composed of multiple wafers can be regarded as a superior level on wafer, and a die is a subordinate level against wafer. In this paper, it is assumed that the sources of CD variation might be classified into three hierarchical levels; 1) run-to-run; 2) wafer-to-wafer; and 3) within-wafer variation. Intra-die variation is supposed to be smaller than others comparatively, so that it is not analyzed. Generally, a sampling plan should be chosen where the largest sample corresponds to what is expected to be the largest source of variation. However, only three runs are sampled taking the cost of sampling into account.

Research objective: Unfortunately, CD uniformity is not easy to achieve due to various sources of variation interposed in device designs and fab processes. Particularly, wafer-level CD uniformity is very closely related to proactive yield management because wafer edge effects, for instance, can cause a comparable die loss. Meanwhile, variance component estimates might be a prerequisite not only for effective CD variation reduction but also for testing the uniformity. In this perspective, we aim to provide guidelines to fab practitioners for estimating the hierarchical variance components as well as testing wafer-level uniformity on CD in a single framework. Using this framework, it is possible to figure out the contribution of each sampling level to the overall CD variation. In parallel, if distinct CD patterns in wafers are detected, practitioners can scrutinize fab conditions and even circuit designs that may cause this phenomenon. Therefore, practitioners can enhance the efficiency of experimental design and analysis for any fab process characteristics in the framework.

Research subjects: Specifically, this study discusses two research subjects; 1) because runs and wafers can be selected at random, it is reasonable to focus on estimating hierarchical variance components for run-to-run, wafer-to-wafer and within-wafer CD variation; and 2) it is attempted to test wafer-level CD uniformity according to predetermined specific (i.e. fixed) die positions. By doing this, within-wafer CD variation can also be estimated, not confounded by the fixed effect relating to the positions.

Research methodology: A two-stage nested design and a randomized complete block design are employed for estimating the hierarchical variance components associated with one whole dataset and subsets, respectively. By two different linear statistical models, one for random and the other for mixed, the nested design is analyzed. Subsequently, Duncan's multiple range test scrutinizes wafer-level CD uniformity for each run using a variance estimate obtained from a randomized complete block design. General explanation on the methodologies can be found in Montgomery (1997) and Montgomery and Runger (1999).

2. Design of Experiments

2.1 Application of a two-stage nested design to a whole dataset

In a fab, each run contains a number of wafers (e.g. generally, up to 25 wafers in a run). A bundle of wafers in a run are usually numbered in series for identification purpose. Meanwhile, each wafer may have five different test element groups (TEGs) in general. Those can be typically positioned at the top, left, center, right and bottom (i.e. denoted by T=1, L=2, C=3, R=4 and B=5) in a wafer where circuit patterns as well as electrical test characteristics of a transistor are tested. In order to estimate the hierarchical variance components, a design for sampling is implemented as shown in <Figure 1>. Even if five wafers numbered 1 to 5 within each run are repeated three times throughout three distinct runs, there is no connection among three wafers with the same identification number. Because all 15 wafers can be renumbered from 1 to 15 in series, this is a two-stage

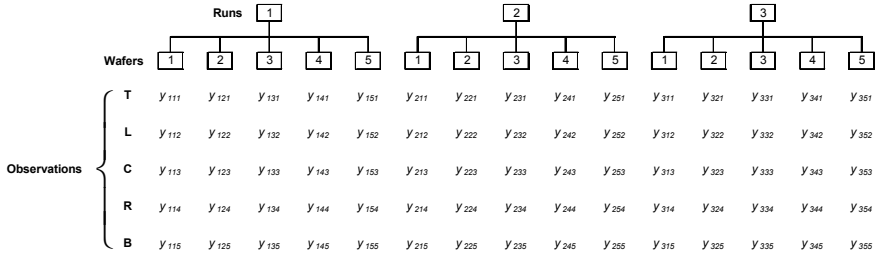

Figure 1. A two-stage nested design.

nest design, with wafers nested under runs.

The linear statistical model for the two-stage nested design is

$$y_{ijk}=\mu+RUN_i+WAF_{j(i)}+\varepsilon_{(ij)k}\begin{cases}i=1,2,\cdots,I\\ j=1,2,\cdots,J\\ k=1,2,\cdots,K\end{cases} \quad (2)$$

where y_{ijk} is a CD observation when factor A (i.e. runs) is at the ith level and factor B (i.e. wafers) is at the jth level for the kth replicate, μ is the overall mean, RUN_i is the effect of the ith level of factor A, $WAF_{j(i)}$ is the effect of the jth level of factor B under the ith level of factor A, and $\varepsilon_{(ij)k}$ is a random error component within the combination of levels of the ith and jth for factor A and B. The subscript *j(i)* indicates that the jth level of factor B is nested under the ith level of factor A, thus the subscript *(ij)k* is used for the random error term. Since there is an equal number of levels of factor B within each level of factor A and an equal number of replicates within each combination of levels of the ith and jth for factor A and B, equation (2) is for a balanced nested design. In equation (2), there is no interaction between factor A and B because every level of factor B does not appear with every level of factor A. In figure 1, there are I = 3 levels of factor A, J = 5 levels of factor B and K = 5 replicates.

Since a single replicate is collected from a certain TEG position (i.e. die position) in each wafer, the variance estimate for $\varepsilon_{(ij)k}$ relates to within-wafer variation. Two factors A and B should be regarded as random factors because runs and wafers can be selected at random. Hence, it is assumed that RUN_i is normally and independently distributed with mean 0 and variance σ^2_{RUN} abbreviated NID(0, σ^2_{RUN}), and $WAF_{j(i)}$ is NID(0, σ^2_{WAF}), and $\varepsilon_{(ij)k}$ is NID(0, σ^2_{ε}). In equation (2), all terms are independent to the others, so the variance of any CD observation is decomposed as equation (3).

$$V(y_{ijk})=\sigma^2_{RUN}+\sigma^2_{WAF}+\sigma^2_{\varepsilon} \quad (3)$$

where $V(y_{ijk})$ is the variance of y_{ijk}. Equation (4) gives the expected mean squares of the two-stage nested design. With equation (4), it is possible to estimate separately the three variance components in equation (3), and two null hypotheses can be tested as follows; 1) H_0: $\sigma^2_{RUN}=0$ by $MS_A/MS_{B(A)}$; and 2) H_0: $\sigma^2_{WAF}=0$ by $MS_{B(A)}/MS_E$.

$$\begin{aligned}E(MS_A)&=\sigma^2_{\varepsilon}+K\sigma^2_{WAF}+JK\sigma^2_{RUN}\\ E(MS_{B(A)})&=\sigma^2_{\varepsilon}+K\sigma^2_{WAF}\\ E(MS_E)&=\sigma^2_{\varepsilon}\end{aligned} \quad (4)$$

By adding a fixed factor C regarding TEGs into equation (2), equation (5) can be established where TEG_k is the effect of the kth level of factor C, and $\varepsilon_{(ij)k}$ is the random error component after the fixed effect separated. It is assumed that $\sum_{k=1}^{K} TEG_k=0$. The expected mean square of factor C is given in equation (6). In equation (5), factor A and B are random, and factor C is fixed, so this is a mixed model. Regarding factor C, a null hypothesis can be tested like H_0: $\mu_1=\mu_2=\cdots=\mu_K$ by MS_C/MS_E.

$$y_{ijk}=\mu+RUN_i+WAF_{j(i)}+TEG_k+\varepsilon_{(ij)k}\begin{cases}i=1,2,\cdots,I\\ j=1,2,\cdots,J\\ k=1,2,\cdots,K\end{cases} \quad (5)$$

$$E(MS_C)=\sigma^2_{\varepsilon}+\frac{IJ\sum_{k=1}^{K}TEG^2_k}{K-1} \quad (6)$$

2.2 Application of a randomized complete block design to a subset

Each run isolated from <Figure 1> can be viewed as a randomized complete block design. The randomized complete block design is presented in <Figure 2>. In each run, every wafer containing five CDs is a block.

The linear statistical model for this design is

$$y_{jk}=\mu+BLK_j+TEG_k+\varepsilon_{jk}\begin{cases}j=1,2,\cdots,J\\ k=1,2,\cdots,K\end{cases} \quad (7)$$

where y_{jk} is a CD observation when factor B (i.e. blocks) at the jth level and factor C (i.e. TEGs) is at the kth level, μ is the overall mean, BLK_j is the effect of the jth block with NID(0, σ^2_{BLK}), TEG_k is the effect of the kth level of factor C with $\sum_{k=1}^{K} TEG_k=0$, and ε_{jk} is the usual random error component with NID(0, σ^2_{ε}). The randomized complete block design is a mixed model with factor B random and factor C fixed. In <Figure 2>, there are J = 5 levels of factor B and K = 5 levels of factor C. Similar to equation (2) and (5), in equation (7), it is assumed that; 1) there is no interaction between factor B and C; and 2) all terms are independent to the others. Therefore, at the kth level of factor C, the variance of any CD observation is decomposed as equation (8).

$$V(y_{jk}) = \sigma^2_{BLK} + \sigma^2_{\varepsilon} \quad (8)$$

where $V(y_{jk})$ is the variance of y_{jk}. The expected mean squares for the randomized complete block design is presented in equation (9). With equation (9), we can estimate the two variance components in equation (8), and two null hypotheses can be tested as follows; 1) H_0: $\sigma^2_{BLK} = 0$ by MS_B/MS_E; and 2) H_0: $\mu_1 = \mu_2 = \cdots = \mu_K$ by MS_C/MS_E.

$$\begin{aligned} E(MS_B) &= \sigma^2_{\varepsilon} + K\sigma^2_{BLK} \\ E(MS_C) &= \sigma^2_{\varepsilon} + \frac{J\sum_{k=1}^{K} TEG^2_k}{K-1} \\ E(MS_E) &= \sigma^2_{\varepsilon} \end{aligned} \quad (9)$$

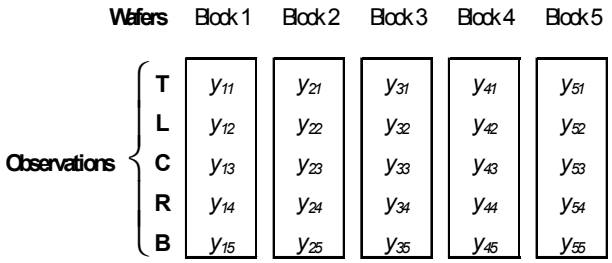

Figure 2. A randomized complete block design.

3. Analysis of Experimental Data

3.1 Variance components estimation with the random effects model

A device considered in this study is a type of complementary MOSFET, and there are two kinds of CDs collected from; 1) N MOS; and 2) P MOS transistor area. The whole dataset is presented in <Table 1>. Because the dataset is collected from a real pilot fab (i.e. during a developing stage of the device concerned), it should be noted that it does not represent a typical CD pattern of a stable mass production line. The panel (a) and (b) show CDs measured in nanometer (nm) by an inline scanning electron microscope at N and P MOS area respectively. Each panel has three runs, five wafers for each run, and each wafer has five CDs from five distinct TEGs.

<Figure 3> depicts sample CD means, and fab practitioners might be interested in two obvious CD variations for both N and P MOS case; 1) CDs in W1 in Run1 are comparatively larger; and 2) on the whole, CDs in Run3 get increased. Before statistical analysis, it is expected that run-to-run variation can be inflated due to Run3. Also, W1 in Run1 may seriously impact the variance estimate

Table 1. Gate poly-silicon CDs (unit: nanometer)

(a)
N MOS

	Run1					Run2					Run3				
TEGs	W1	W2	W3	W4	W5	W1	W2	W3	W4	W5	W1	W2	W3	W4	W5
T	242.9	203.5	204.0	200.8	209.7	210.3	207.1	207.8	210.9	209.6	229.3	230.0	230.1	234.0	240.2
L	243.7	206.7	201.8	202.3	209.1	210.1	210.1	210.7	214.5	210.7	229.2	230.1	232.8	230.7	235.1
C	238.6	204.2	199.4	201.8	209.1	191.4	208.2	202.7	210.2	207.0	226.4	221.7	228.0	231.4	233.3
R	249.7	214.1	210.1	209.3	217.1	218.0	215.0	214.8	220.5	219.5	234.0	238.9	238.0	240.8	239.5
B	246.9	211.2	207.1	205.4	218.0	213.2	209.5	207.8	217.4	214.1	229.4	233.3	232.7	235.3	235.5

(b)
P MOS

	Run1					Run2					Run3				
TEGs	W1	W2	W3	W4	W5	W1	W2	W3	W4	W5	W1	W2	W3	W4	W5
T	245.7	205.8	208.7	210.1	212.9	214.0	213.1	210.2	221.6	217.8	239.3	236.0	238.8	243.1	242.2
L	248.5	211.2	208.2	205.5	219.8	215.1	211.0	211.6	217.8	210.2	234.6	239.8	238.5	237.8	238.3
C	246.3	211.1	205.4	201.4	212.4	193.3	207.1	208.9	213.2	212.0	230.0	232.3	233.2	238.3	237.5
R	247.7	216.9	215.1	212.8	216.0	224.0	215.7	215.8	224.8	221.9	243.0	241.1	239.0	244.5	247.7
B	254.9	214.7	209.3	208.4	216.2	219.1	215.0	212.9	223.4	220.0	236.2	241.4	239.9	240.1	242.5

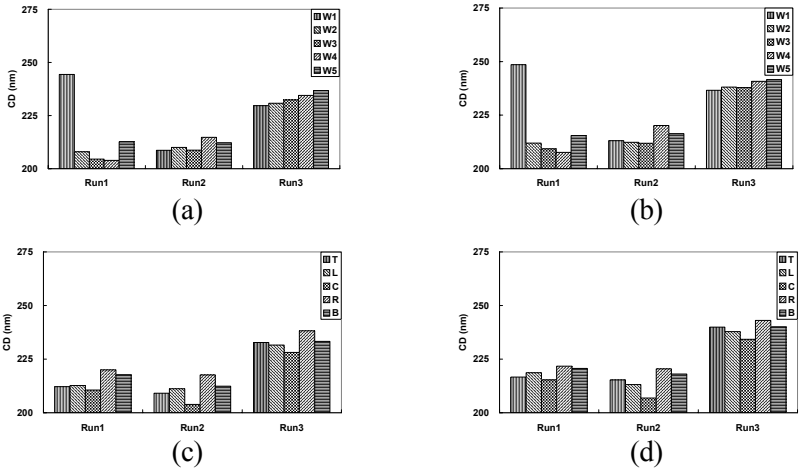

Figure 3. Sample CD means; (a) by wafers (N MOS); (b) by wafers (P MOS); (c) by TEGs (N MOS); and (d) by TEGs (P MOS).

for wafer-to-wafer variation of Run1.

<Table 2> summarizes statistical analyses regarding the hierarchical variance components associated with the random effects model in equation (2). The computer software Minitab™ is mainly used for analysing the experimental data. Panel (a) and (b) present analysis of variance (ANOVA) tables for N and P MOS case respectively, and each panel has four different ANOVA tables. On the whole, it is noticed that there are small *p*-values, and we may reject the null hypotheses of the two-stage nested design and the randomized complete block design. For illustration, results are explained on N MOS case only. The first ANOVA table of panel (a) summarizes results analyzed from the two-stage nested design using 75 CDs. The two rightmost columns of the table provide estimates of the hierarchical variance components and the expected mean squares respectively. The next three ANOVA tables of panel (a) correspond to the analyses on the three randomized complete block designs for Run1, 2 and 3 respectively. These three ANOVA tables have the same expected mean squares as Run1 does.

From the analysis on the two-stage nested design, the hierarchical variance components are estimated as follows; 1) for run-to-run variation, $\hat{\sigma}^2_{RUN} = 117.30$ is the largest among the three hierarchical variance component estimates; 2) for wafer-to-wafer variation, $\hat{\sigma}^2_{WAF} = 96.14$; and 3) for the random error component (i.e. within-wafer variation), $\hat{\sigma}^2_{\varepsilon} = 23.22$.

For the next three ANOVA tables associated with the randomized complete block design, Run1 has a distinguished behavior of variance estimates against Run2 and 3. With respect to Run1, the variance estimate for block-to-block variation (i.e. wafer-to-wafer variation), $\hat{\sigma}^2_{BLK} = 287.20$ is considerably larger than the variance estimate for the random error component, $\hat{\sigma}^2_{\varepsilon} = 2.04$ due to the impact of W1 in Run1. Meanwhile, Run2 and 3 show more stabilized wafer-to-wafer variation. Thus, we can see that these variance decompositions confirm the graphical interpretation on <Figure 3>.

In each run, a pooled estimate of the common variance within each of five fixed levels of factor *C* (i.e. TEGs) can be calculated as equation (10).

$$S^2_p = \frac{\sum_{k=1}^{K} (J-1)\, S^2_k}{\sum_{k=1}^{K} (J-1)} \tag{10}$$

where S^2_p is the pooled estimate, S^2_k is the sample variance in the *k*th level of factor *C*. As for Run1, $\widehat{\sigma^2_{BLK}} = 287.20$ and $\widehat{\sigma^2_{\varepsilon}} = 2.04$ decompose $S^2_p = 289.24$ mutually exclusively and collectively exhaustively.

3.2 Variance components estimation with the mixed model

Based on the mixed model, panel (a) and (b) in <Table 3> present ANOVA tables for N and P MOS case respectively. Because two cases can be explained in a similar manner, only N MOS case is set forth here. At panel (a) in <Table 3>, the sum of squares due to error at panel (a) in <Table 2> (i.e. $SS_E = 1393.49$) is decomposed into two components; 1) $SS_C = 1006.36$; and 2) $SS_E = 387.13$.

Table 2. ANOVA tables

(a)

N MOS

Variation type	Source of variation	Degrees of freedom	Sum of squares	Mean square	F_0	p-value	Variance component	Expected mean square
Run-to-run	A: Runs	2	6872.71	3436.36	6.82	0.011	117.30	$\sigma_\varepsilon^2 + K\sigma_{WAF}^2 + JK\sigma_{RUN}^2$
Wafer-to-wafer	B: Wafers (within runs)	12	6046.98	503.92	21.70	0.000	96.14	$\sigma_\varepsilon^2 + K\sigma_{WAF}^2$
Within-wafer	Error	60	1393.49	23.22			23.22	σ_ε^2
	Total	74	14313.18					
Run1	B: Blocks	4	5752.36	1438.09	703.57	0.000	287.20	$\sigma_\varepsilon^2 + K\sigma_{BLK}^2$
	C: TEGs	4	323.80	80.95	39.60	0.000		$\sigma_\varepsilon^2 + J\sum_{k=1}^{K} TEG_k^2/(K-1)$
	Error	16	32.70	2.04			2.04	σ_ε^2
	Total	24	6108.86					
Run2	B: Blocks	4	133.89	33.47	2.67	0.071	4.18	
	C: TEGs	4	493.95	123.49	9.84	0.000		
	Error	16	200.88	12.55			12.55	
	Total	24	828.72					
Run3	B: Blocks	4	160.72	40.18	8.23	0.001	7.06	
	C: TEGs	4	264.05	66.01	13.52	0.000		
	Error	16	78.10	4.88			4.88	
	Total	24	502.88					

(b)

P MOS

Variation type	Source of variation	Degrees of freedom	Sum of squares	Mean square	F_0	p-value	Variance component	Expected mean square
Run-to-run	A: Runs	2	8481.00	4240.50	8.29	0.005	149.16	$\sigma_\varepsilon^2 + K\sigma_{WAF}^2 + JK\sigma_{RUN}^2$
Wafer-to-wafer	B: Wafers (within runs)	12	6137.70	511.47	22.03	0.000	97.65	$\sigma_\varepsilon^2 + K\sigma_{WAF}^2$
Within-wafer	Error	60	1393.30	23.22			23.22	σ_ε^2
	Total	74	16012.00					
Run1	B: Blocks	4	5806.42	1451.61	160.12	0.000	288.50	$\sigma_\varepsilon^2 + K\sigma_{WAF}^2$
	C: TEGs	4	143.11	35.78	3.95	0.020		$\sigma_\varepsilon^2 + J\sum_{k=1}^{K} TEG_k^2/(K-1)$
	Error	16	145.05	9.07			9.06	σ_ε^2
	Total	24	6094.58					
Run2	B: Blocks	4	242.48	60.62	3.48	0.032	8.63	
	C: TEGs	4	540.12	135.03	7.74	0.001		
	Error	16	279.00	17.44			17.43	
	Total	24	1061.60					
Run3	B: Blocks	4	88.80	22.20	4.73	0.010	3.50	
	C: TEGs	4	211.03	52.75	11.25	0.000		
	Error	16	75.01	4.68			4.68	
	Total	24	374.85					

By separating the variation due to TEGs, within-wafer variation can be more precisely estimated as $\hat{\sigma}_{\varepsilon}^2 = 6.91$ compared to $\hat{\sigma}_{\varepsilon}^2 = 23.22$ of panel (a) in <Table 2>. On top of the estimation, wafer-level CD uniformity can be checked out considering the whole dataset. The small *p*-value associated with factor *C* indicates that CDs might not be patterned uniformly at wafer-level.

3.3 Wafer-level CD uniformity tests

In <Table 2> and <Table 3>, we can see that there is lack of wafer-level CD uniformity. If a wafer-level CD uniformity does not acquired, the equipment and materials in photolithography process could be scrutinized. For a more detailed analysis on the wafer-level CD uniformity according to die positions, Duncan's multiple range test is combined with the randomized complete block design. For each run, this test procedure needs an estimate of the standard error of sample CD mean for each TEG as equation (11).

$$S_{\overline{y}_{.k}} = \sqrt{\frac{\hat{\sigma}_{\varepsilon}^2}{J}} \tag{11}$$

where $S_{\overline{y}_{.k}}$ is the estimate of the standard error of sample CD mean for the *k*th level of factor *C* (i.e. TEGs), and $\hat{\sigma}_{\varepsilon}^2$ is the variance estimate for the random error component of the randomized complete block design. <Table 4> and <Table 5> show the results of Duncan's multiple range tests with the significance level α = 0.05 for comparing all pairs of means at different TEGs for N and P MOS case respectively. Results show that, for all three runs, there is CD non-uniformity and even a similar concentric CD pattern within wafers. That is, as a die locates farther from the center of wafer, CD gets larger as shown in <Table 6>. However, <Table 6> simply gives inequalities on sample CD means, not the statistically significant difference in sample CD means.

For instance, in the leftmost column of <Table 4>, $\hat{\sigma}_{\varepsilon}^2 = 2.04$ is used in calculating $S_{\overline{y}_{.k}} = 0.64$, and five sample CD means are $\overline{y}_{.C} = 210.62$, $\overline{y}_{.T} = 212.18$, $\overline{y}_{.L} = 212.72$, $\overline{y}_{.B} = 217.72$ and $\overline{y}_{.R} = 220.06$ according to TEGs. With four different least significant ranges (i.e. R_p for p = 2, 3, 4 and 5), the last ten lines of this column present comparisons. It is noticed that, for eight out of ten comparisons, the difference in sample CD means is larger than its corresponding R_p.

Table 3. ANOVA tables based on the mixed model

(a)

N MOS

Variation type	Source of variation	Degrees of freedom	Sum of squares	Mean square	F_0	*p*-value	Variance component	Expected mean square
Run-to-run	A: Runs	2	6872.71	3436.36	6.82	0.011	117.30	$\sigma_{\varepsilon}^2 + K\sigma_{WAF}^2 + JK\sigma_{RUN}^2$
Wafer-to-wafer	B: Wafers (within runs)	12	6046.98	503.91	72.89	0.000	99.40	$\sigma_{\varepsilon}^2 + K\sigma_{WAF}^2$
	C: TEGs	4	1006.36	251.59	36.39	0.000		$\sigma_{\varepsilon}^2 + IJ\sum_{k=1}^{K} TEG_k^2/(K-1)$
Within-wafer	Error	56	387.13	6.91			6.91	σ_{ε}^2
	Total	74	14313.18					

(b)

P MOS

Variation type	Source of variation	Degrees of freedom	Sum of squares	Mean square	F_0	*p*-value	Variance component	Expected mean square
Run-to-run	A: Runs	2	8480.98	4240.49	8.29	0.005	149.16	
Wafer-to-wafer	B: Wafers (within runs)	12	6137.71	511.48	46.51	0.000	100.10	
	C: TEGs	4	777.48	194.37	17.67	0.000		
Within-wafer	Error	56	615.84	11.00			11.00	
	Total	74	16012.01					

Table 4. Duncan's multiple range tests (N MOS)

N MOS		
Run1	Run2	Run3
$\overline{y_{.C}} = 210.62$	$\overline{y_{.C}} = 203.90$	$\overline{y_{.C}} = 228.16$
$\overline{y_{.T}} = 212.18$	$\overline{y_{.T}} = 209.14$	$\overline{y_{.L}} = 231.58$
$\overline{y_{.L}} = 212.72$	$\overline{y_{.L}} = 211.22$	$\overline{y_{.T}} = 232.72$
$\overline{y_{.B}} = 217.72$	$\overline{y_{.B}} = 212.40$	$\overline{y_{.B}} = 233.24$
$\overline{y_{.R}} = 220.06$	$\overline{y_{.R}} = 217.56$	$\overline{y_{.R}} = 238.24$
$S_{\overline{y_{.k}}} = \sqrt{2.04/5} = 0.64$	$S_{\overline{y_{.k}}} = \sqrt{12.55/5} = 1.58$	$S_{\overline{y_{.k}}} = \sqrt{4.88/5} = 0.99$
$R_2 = r_{0.05}(2,16)S_{\overline{y_{.k}}} = (3.00)(0.64) = 1.92$	$R_2 = r_{0.05}(2,16)S_{\overline{y_{.k}}} = (3.00)(1.58) = 4.75$	$R_2 = r_{0.05}(2,16)S_{\overline{y_{.k}}} = (3.00)(0.99) = 2.96$
$R_3 = r_{0.05}(3,16)S_{\overline{y_{.k}}} = (3.15)(0.64) = 2.01$	$R_3 = r_{0.05}(3,16)S_{\overline{y_{.k}}} = (3.15)(1.58) = 4.99$	$R_3 = r_{0.05}(3,16)S_{\overline{y_{.k}}} = (3.15)(0.99) = 3.11$
$R_4 = r_{0.05}(4,16)S_{\overline{y_{.k}}} = (3.23)(0.64) = 2.06$	$R_4 = r_{0.05}(4,16)S_{\overline{y_{.k}}} = (3.23)(1.58) = 5.12$	$R_4 = r_{0.05}(4,16)S_{\overline{y_{.k}}} = (3.23)(0.99) = 3.19$
$R_5 = r_{0.05}(5,16)S_{\overline{y_{.k}}} = (3.30)(0.64) = 2.11$	$R_5 = r_{0.05}(5,16)S_{\overline{y_{.k}}} = (3.30)(1.58) = 5.23$	$R_5 = r_{0.05}(5,16)S_{\overline{y_{.k}}} = (3.30)(0.99) = 3.26$
R vs. *C*: 9.44 > 2.11 (R_5)	*R* vs. *C*: 13.66 > 5.23 (R_5)	*R* vs. *C*: 10.08 > 3.26 (R_5)
R vs. *T*: 7.88 > 2.06 (R_4)	*R* vs. *T*: 8.42 > 5.12 (R_4)	*R* vs. *L*: 6.66 > 3.19 (R_4)
R vs. *L*: 7.34 > 2.01 (R_3)	*R* vs. *L*: 6.34 > 4.99 (R_3)	*R* vs. *T*: 5.52 > 3.11 (R_3)
R vs. *B*: 2.34 > 1.92 (R_2)	*R* vs. *B*: 5.16 > 4.75 (R_2)	*R* vs. *B*: 5.00 > 2.96 (R_2)
B vs. *C*: 7.10 > 2.06 (R_4)	*B* vs. *C*: 8.50 > 5.12 (R_4)	*B* vs. *C*: 5.08 > 3.19 (R_4)
B vs. *T*: 5.54 > 2.01 (R_3)	*B* vs. *T*: 3.26 < 4.99 (R_3)	*B* vs. *L*: 1.66 < 3.11 (R_3)
B vs. *L*: 5.00 > 1.92 (R_2)	*B* vs. *L*: 1.18 < 4.75 (R_2)	*B* vs. *T*: 0.52 < 2.96 (R_2)
L vs. *C*: 2.10 > 2.01 (R_3)	*L* vs. *C*: 7.32 > 4.99 (R_3)	*T* vs. *C*: 4.56 > 3.11 (R_3)
L vs. *T*: 0.54 < 1.92 (R_2)	*L* vs. *T*: 2.08 < 4.75 (R_2)	*T* vs. *L*: 1.14 < 2.96 (R_2)
T vs. *C*: 1.56 < 1.92 (R_2)	*T* vs. *C*: 5.24 > 4.75 (R_2)	*L* vs. *C*: 3.42 > 2.96 (R_2)

Table 5. Duncan's multiple range tests (P MOS)

P MOS		
Run1	Run2	Run3
$\overline{y_{.C}} = 215.32$	$\overline{y_{.C}} = 206.90$	$\overline{y_{.C}} = 234.26$
$\overline{y_{.T}} = 216.64$	$\overline{y_{.L}} = 213.14$	$\overline{y_{.L}} = 237.80$
$\overline{y_{.L}} = 218.64$	$\overline{y_{.T}} = 215.34$	$\overline{y_{.T}} = 239.88$
$\overline{y_{.B}} = 220.70$	$\overline{y_{.B}} = 218.08$	$\overline{y_{.B}} = 240.02$
$\overline{y_{.R}} = 221.70$	$\overline{y_{.R}} = 220.44$	$\overline{y_{.R}} = 243.06$
$S_{\overline{y_{.k}}} = \sqrt{9.07/5} = 1.35$	$S_{\overline{y_{.k}}} = \sqrt{17.44/5} = 1.87$	$S_{\overline{y_{.k}}} = \sqrt{4.68/5} = 0.97$
$R_2 = r_{0.05}(2,16)S_{\overline{y_{.k}}} = (3.00)(1.35) = 4.04$	$R_2 = r_{0.05}(2,16)S_{\overline{y_{.k}}} = (3.00)(1.87) = 5.60$	$R_2 = r_{0.05}(2,16)S_{\overline{y_{.k}}} = (3.00)(0.97) = 2.90$
$R_3 = r_{0.05}(3,16)S_{\overline{y_{.k}}} = (3.15)(1.35) = 4.24$	$R_3 = r_{0.05}(3,16)S_{\overline{y_{.k}}} = (3.15)(1.87) = 5.88$	$R_3 = r_{0.05}(3,16)S_{\overline{y_{.k}}} = (3.15)(0.97) = 3.05$
$R_4 = r_{0.05}(4,16)S_{\overline{y_{.k}}} = (3.23)(1.35) = 4.35$	$R_4 = r_{0.05}(4,16)S_{\overline{y_{.k}}} = (3.23)(1.87) = 6.03$	$R_4 = r_{0.05}(4,16)S_{\overline{y_{.k}}} = (3.23)(0.97) = 3.12$
$R_5 = r_{0.05}(5,16)S_{\overline{y_{.k}}} = (3.30)(1.35) = 4.44$	$R_5 = r_{0.05}(5,16)S_{\overline{y_{.k}}} = (3.30)(1.87) = 6.16$	$R_5 = r_{0.05}(5,16)S_{\overline{y_{.k}}} = (3.30)(0.97) = 3.19$
R vs. *C*: 6.38 > 4.44 (R_5)	*R* vs. *C*: 13.54 > 6.16 (R_5)	*R* vs. *C*: 8.80 > 3.19 (R_5)
R vs. *T*: 5.06 > 4.35 (R_4)	*R* vs. *L*: 7.30 > 6.03 (R_4)	*R* vs. *L*: 5.26 > 3.12 (R_4)
R vs. *L*: 3.06 < 4.24 (R_3)	*R* vs. *T*: 5.10 < 5.88 (R_3)	*R* vs. *T*: 3.18 > 3.05 (R_3)
R vs. *B*: 1.00 < 4.04 (R_2)	*R* vs. *B*: 2.36 < 5.60 (R_2)	*R* vs. *B*: 3.04 > 2.90 (R_2)
B vs. *C*: 5.38 > 4.35 (R_4)	*B* vs. *C*: 11.18 > 6.03 (R_4)	*B* vs. *C*: 5.76 > 3.12 (R_4)
B vs. *T*: 4.06 < 4.24 (R_3)	*B* vs. *L*: 4.94 < 5.88 (R_3)	*B* vs. *L*: 2.22 < 3.05 (R_3)
B vs. *L*: 2.06 < 4.04 (R_2)	*B* vs. *T*: 2.74 < 5.60 (R_2)	*B* vs. *T*: 0.14 < 2.90 (R_2)
L vs. *C*: 3.32 < 4.24 (R_3)	*T* vs. *C*: 8.44 > 5.88 (R_3)	*T* vs. *C*: 5.62 > 3.05 (R_3)
L vs. *T*: 2.00 < 4.04 (R_2)	*T* vs. *L*: 2.20 < 5.60 (R_2)	*T* vs. *L*: 2.08 < 2.90 (R_2)
T vs. *C*: 1.32 < 4.04 (R_2)	*L* vs. *C*: 6.24 > 5.60 (R_2)	*L* vs. *C*: 3.54 > 2.90 (R_2)

Table 6. Wafer-level concentric CD patterns according to TEGs

	N MOS	P MOS
Run 1	$C < T < L < B < R$	$C < T < L < B < R$
Run 2	$C < T < L < B < R$	$C < L < T < B < R$
Run 3	$C < L < T < B < R$	$C < L < T < B < R$

4. Conclusions and Further Work

Primarily, this paper presents a single framework regarding estimating the hierarchical variance components and testing the wafer-level uniformity on CD. A two-stage nested design is analyzed by the random effects and mixed model, and a randomized complete block design is applied to each subset from the whole dataset. Duncan's multiple range tests plus ANOVA analyses perform the wafer-level CD uniformity. With understanding of the statistical design, the analysis procedure can be illustrated as in < Figure 4 >.

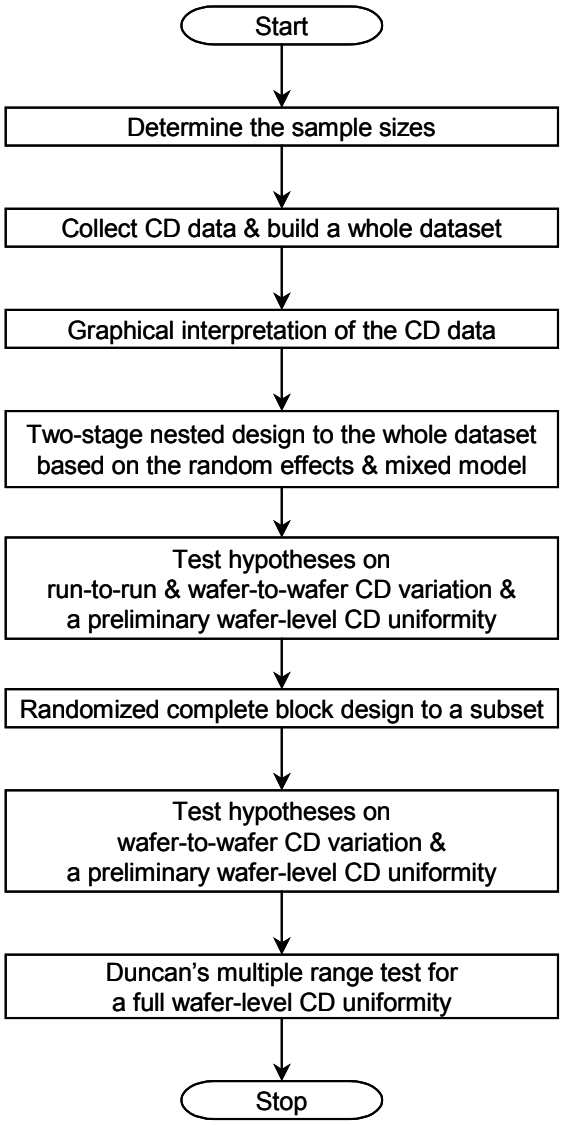

Figure 4. A flow-chart for the analysis procedure.

By the run-by-run uniformity test, it is confirmed that there is a concentric CD pattern, a type of wafer edge effects. In fabs, based on the results, so-called two-image masks procedure is adopted to diminish the pattern where narrower patterned masks are utilized for the edge region of wafers. Meanwhile, if the sampling budget is allowed, the experimental design needs to have additional number of runs not only for estimating run-to-run variation more precisely but also for determining appropriate mask patterns for this newly adopted procedure. For further work, empirical model building techniques like response surface methodologies can be considered for building a relationship between CDs and electrical test characteristics concerned.

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