The Memory Effects of a Carbon Nanotube Nanodevice

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To discover electrical properties of individual single wall nanotube(SWNT), a number of SWNT-based tubeFETs have been fabricated. The device consists of a single semiconducting SWNT on an insulating substrate, contacted at each end by metal electrodes. It presents high transconductances, and charge storage phenomenon, which is the operations of injecting electrons from the nanotube channel of a tubeFET into charge traps on the surface of the SiO_2 gate dielectric, thus shifting the threshold voltage. This phenomenon can be repeated many times, and maintained for the hundreds of seconds at room temperature. We will report this phenomenon as the memory effects of the SWNT, and attempt to use this property for the memory device.

Keywords : Carbon nanotube, Mmemory effects, SWNT, TubeFET, Electron beam lithography

1. INTORDUCTION

The last 20 years' hot topic has been the miniaturization of electronic, optical and electro-mechanical devices based on the integrated circuit technology. The successes of nanotechnologies have captured the imagination of the general public as well as the scientist and the engineer.

The electrical properties of carbon nanotubes (NTs), a class of macromolecules discovered almost a decade ago, may play a central role in future nanoelectronics[1]. Their unique structure makes them potentially useful as basic elements for generations of highly integrated circuits[2]. Single-walled carbon nanotubes may be wrapped by a metallic or graphene lattice. To discover the electrical properties of a SWNT, a number of SWNT-based electronic devices have been demonstrated, including single-electron transistors (SETs)[3], field-effect transistors (FETs)[4], and junction devices[5]. While the transport in NTs is responsible for the wide variety of electrical properties found so far[4], it is this structure on the other hand, which makes it very difficult to characterize the intrinsic transport properties of the SWNT. The problem is to perform a noninvasive measurement, which is essential to discover memory effects associated with the device structure.

The memory effects on SWNTs have been studied by several groups. The charging of the SWNT is induced on the SiO_2 surface (bottom layer). It can result in the formation of barriers in the tube, which is ideal for the investigation of a nano-memory device. In addition, Cui and co-workers[6] clearly demonstrated that ambipolar nanotube transistors may be created with exceptionally large transconductance. Their transistors can also function as single molecule memory cells that are stable for days at room temperature.

2. EXPERIMENT

The experimental procedures are shown in Fig. 1. The degenerately-doped silicon wafer with 500-1000nm of thermally grown SiO_2 is used. The first step is to depositing a catalyst metal that is prepared by mixing a fused Fe catalyst with ethanol on our substrate. The size range of the fused Fe particles are from 5-65nm. The second step is to grow SWNTs. Substrates coated with the catalyst are loaded into a thermal CVD with Ar and H_2 gases flowing through at rates of 600sccm and 400sccm. Once the furnace is heated up to 780℃ for 10minutes, a flow of 2sccm ethylene is admitted into the quartz tube.

Alignment markers were patterned on the substrate by using the electron-beam lithography. SWNTs are selected by their apparent height of 2 nm or less in the atomic force microscope(AFM) images and the coordinates of the SWNTs are registered with respect to alignment markers for the third step. The next steps are

to do the e-beam lithography and to deposit the metal electrode. The electron-beam lithography processing establishes Au(45nm)/Cr(5nm) electrical contacts to individual SWNT as shown in Fig. 3. The devices are measured by AFM to make sure whether they are contacted or not. At last measurements of the electrical properties of contacted devices were made by the stationary probe.

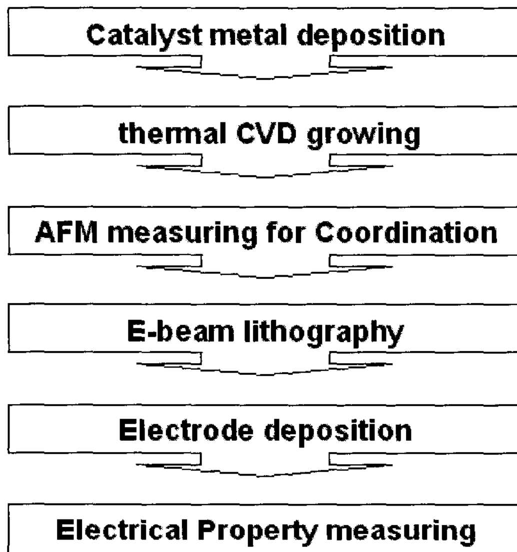


Fig. 1. Experimental procedures for SWNT tubeFETs.

3. RESULTS AND DISCUSSION

Figure 2. shows the AFM image and data of the individual SWNT which was grown at 780℃ by the thermal CVD. To measure the height, the length, and the coordination used for the electron beam lithography, measurements were carried out several times for one SWNT. The data present that the height and the length are 1.85±0.005nm and 7㎛, respectively. According to our previous experiments, the size should be sufficient to make tubeFET if the length is over 1㎛. It is possible to confirm that these are individual, not bundle, because the height is precisely uniformed throughout the tube. Any catalyst metals were not found around the tube and the end of the tube was curved. It seems the tube had grown vertically at the initial stage, and fallen down while growing. The catalyst had disappeared by then, and the tip of the tube functioned like the catalyst. It is good for analyzing the electrical properties when catalyst metals don't exist because it is free from the effects of them.

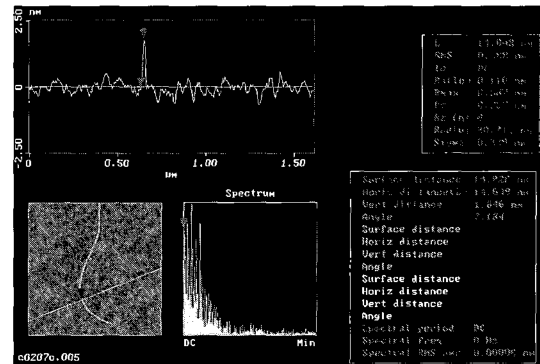
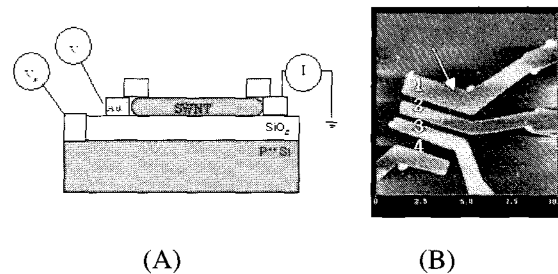


Fig. 2. AFM image and data of the individual SWNT which was grown at 780℃ by the thermal CVD.



(A) (B)

Fig. 3. (A) Schematic diagram of the SWNT tubeFET. (B) the AFM image of the SWNT tubeFET sample grown by the thermal CVD with the nanotube diameter of 1.1nm.

Figure 4 displays an I-V_{bias} curve for the sample in Fig 3. At V_{gate}=0, a small nonlinearity seems to be present in the I-V_{bias} curve. As the V_{bias} is increased to positive values, a pronounced gap-like nonlinearity develops around V_{bias}=0. The I-V_{bias} curve shows a resistance that saturates around 1MΩ. For the major part this resistance is due to the contact resistance between the tube and the electrodes. We thus obtain a controllable semiconductor-to-metal transition in a one-dimensional system[4].

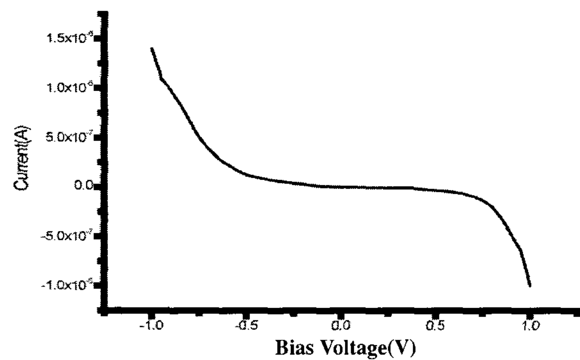


Fig. 4. Two probe I-V_{bias} curves, which was taken at room temperature and in atmospheric pressure, with applying the voltage to contact 2(source) and 3(drain).

Figure 5. shows the current-gate voltage (I-V_g) characteristics of the device connected to two Au/Cr electrodes separated by 0.6mm. The data was acquired at ambient conditions and the bias voltage of V=10mV. Fig. 5. indicates two different data sets, one acquired starting at –10V and the other beginning at a gate voltage of 10V. The threshold voltages are shifted with respect to each other: 2.5V for the curve starting at –10V("down" sweep) and 5.5V for the one starting at +10V("up" sweep). This phenomenon was first reported by Fuhrer and co-workers, and they suggested the use of these devices as electrically-programmable memories.[7] They thought this phenomenon could form the basis of a tubeFET to be used as a charge-storage memory device. The devices operate by injecting electrons from the nanotube channel of a tubeFET into charge traps on the surface of the SiO_2 gate dielectric, thus shifting the threshold voltage. These devices are fabricated from CVD-grown semiconducting nanotube, which are annealed in hydrogen atmosphere during nanotube growth. It seems to decrease charge trap density. The direction of the threshold voltage shift relative to the direction of the electric field can be used to determine the net sign of the trapped charges. This is because net negative charges are trapped in the bulk oxide and the majority of the traps are at near the electrode/SiO_2 interface. About the reason of the phenomena, we suggest the mechanism as shown in Fig. 6. The steps are that 1) the negative charges are moved to near the SiO_2 layer when the positive voltage is applied, and 2) the net negative charges are trapped and stay in the bulk oxide even though the applied voltage is removed. 3) The negarive charges are released and the positive charges move when the negative voltage is applied. 4) The net positive charges are trapped and stay in the bulk oxide even though the applied voltage is removed. We have tried to get some clear evidences of the mechanism.

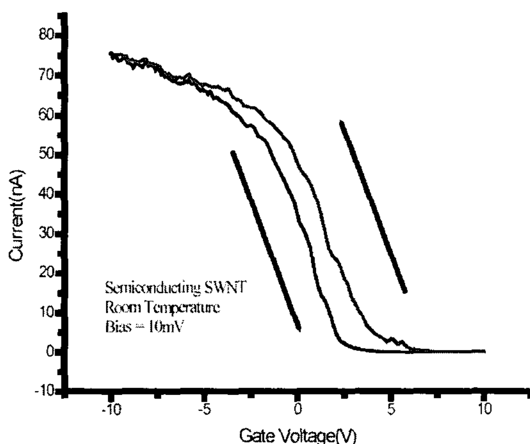


Fig. 5. The curves are current changes as function of gate voltage for a typical TubeFET device at room temperature with a source-drain bias of 10mV.

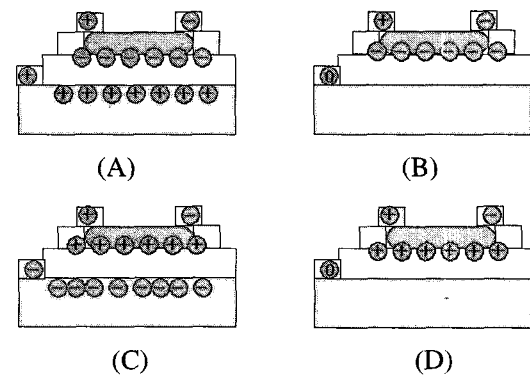


Fig. 6. The threshold voltage shift relative to the direction of the electric field means the net sign of the trapped charges. A) The negative charges are moved to near the SiO_2 layer when the positive voltage is applied. B) The net negative charges are trapped and stay in the bulk oxide even though the applied voltage is removed. C) The negative charges are released and the positive charges move. D) The net positive charges are trapped and stay in the bulk oxide even though the applied voltage is removed.

Figure 7. shows readout data from the memory device during a writing sequence. The device is biased at 10mV, and the current gate voltage is shown as a function of time. Each data bit is marked as "1"(high conductance) or "0" (low conductance) state. The output current is perfectly matched with the input gate voltage signal. Fig.4. means a SWNT can be applied as an erasable programmable memory and a SWNT device is a promising structure for a metal-oxide-semiconductor capacitor in a dynamic random access memory(DRAM) cell because it is not necessary to refresh it like the present DRAMs due to long charge lifetimes in the deep oxide traps.

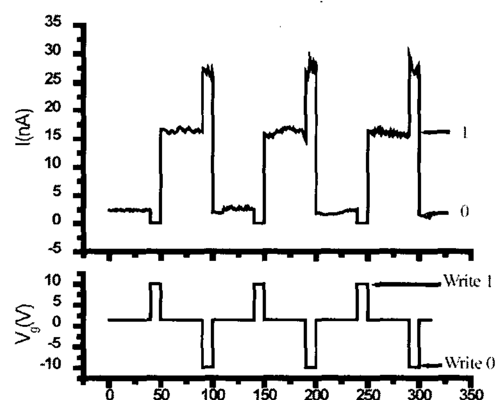


Fig. 7. Current was changed with gate voltage was done as a function of time during several read/write/read/erase cycles of the Tube FET memory.

4. CONCLUSION

We fabricated the SWNT tube FET and characterized the integration of the entire memory cell. The device shows semiconducting properties in I-V curve, and the significant shifts in threshold voltage, changing the gate voltage. This hysteresis seems due to trapped charges within the dielectric layer and each bit is stored in as few as one hundred electrons. It indicated that it should be possible to build-to-build nanotube-based single-electron memory elements [6]. Our experiments and new attempt suggest we are already at the heart of many proposed approaches to nano-electronics.

ACKNOWLEDGMENTS

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