6-18 GHz MMIC Drive and Power Amplifiers

Hong-Teuk Kim, Moon-Suk Jeon, Ki-Woong Chung, and Youngwoo Kwon

Abstract— **This paper presents MMIC drive and power amplifiers covering 6-18 GHz. For simple wideband impedance matching and less sensitivity to fabrication variation, modified distributed topologies are employed in the both amplifiers. Cascade amplifiers with a self-biasing circuit through feedback resistors are used as unit gain blocks in the drive amplifier, resulting in high gain, high stability, and compact chip size. Self impedance matching and high-pass, low-pass impedance matching networks are used in the power amplifier. In measured results, the drive amplifier showed good return losses (S_{11}, S_{22} < -10.5 dB), gain flatness (S_{21}= 16 ± 0.6 dB), and P_{1dB} > 22 dBm over 6-18 GHz. The power amplifier showed P_{1dB} > 28.8 dBm and P_{sat} ≈ 30.0 dBm with good small signal characteristics (S_{11} < -10 dB, S_{22} < -6 dB, and S_{21}= 18.5 ± 1.25 dB) over 6-18 GHz.**

Index Terms — **6-18 GHz MMIC amplifier, wideband amplifier, distributed amplifier.**

I. INTRODUCTION

Wideband microwave MMIC amplifiers are of interest to electronic warfare and countermeasures due to their small size, low cost, and reliability. Generally, these chips require high return loss (> 10 dB), good gain flatness and high output power over wideband frequencies. For meeting these goals, the feedback amplifier, distributed amplifier and lossy matching amplifier topologies have been usually employed [1]-[3].

In this work, wideband MMIC amplifiers have been designed using the modified distributed topologies in which wideband impedance matching is basically simple and consequently the sensitivity to fabrication process variation is low. In drive amplifier, a cascade amplifier with a self-biasing circuit through feedback resistors is used as an active unit cell, resulting in high stability and high gain in distributed amplifier. In power amplifier, the distributed amplifying unit cell considering high output power is first designed and then wideband impedance matching with high-pass, low-pass network is used at input and output ports. Moreover, simple self impedance matching network is also employed at inter-stage.

Wire bonds, input/output SMA connections, and power combiners increase loss as frequency goes up in an amplifier module. Therefore, the gain and output power of MMIC amplifiers are designed to be gradually increased with frequency. These chips were made using a 4-mil thickness GaAs substrate and TRW 0.15-μm PHEMT process.

II. DRIVE AMPLIFIER

Fig. 1 shows the schematic of the proposed active unit cell in distributed drive amplifier. This active unit cell is a cascade amplifier with a self-biasing circuit through feedback resistors. For increasing the cutoff frequency of gate line as well as gain and output power of a distributed amplifier, a gate width 200-μm PHEMT and a gate width 480-μm PHEMT are used at input and output stages, respectively. The drain current of 200 μm PHEMT is supplied through the parallel feedback resistor of 187 Ω and the gate voltage of 480 μm PHEMT is self-biased by the series feedback resistor of

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Manuscript received January 2, 2002; revised June 12, 2002.

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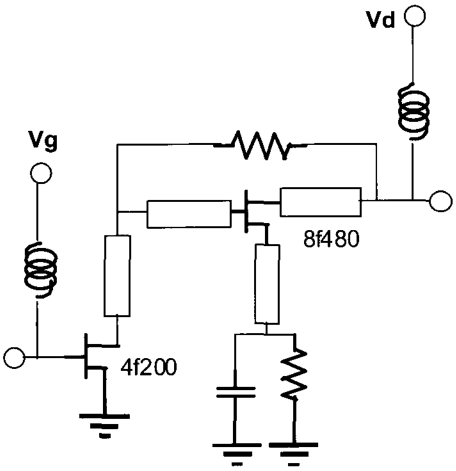


Fig. 1. Schematic of the proposed cascade active unit cell in distributed drive amplifier.

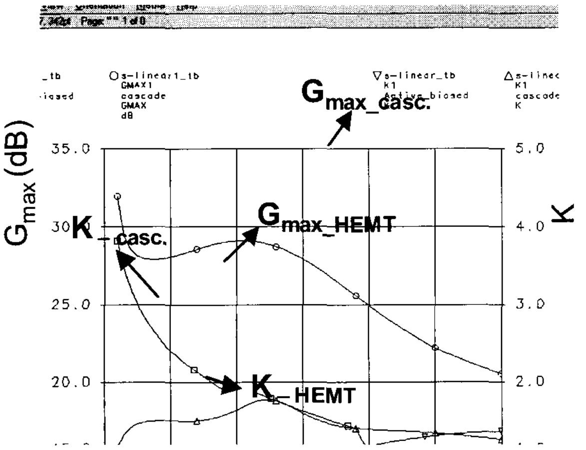


Fig. 2. Maximum available gains(MAG) and stability factors (K) of single 480-μm PHEMT and cascade active unit cell of drive amplifier.

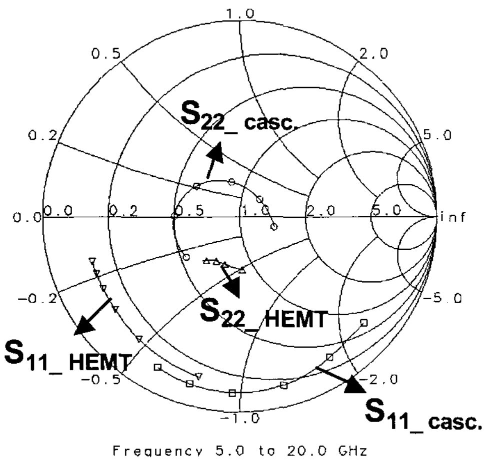
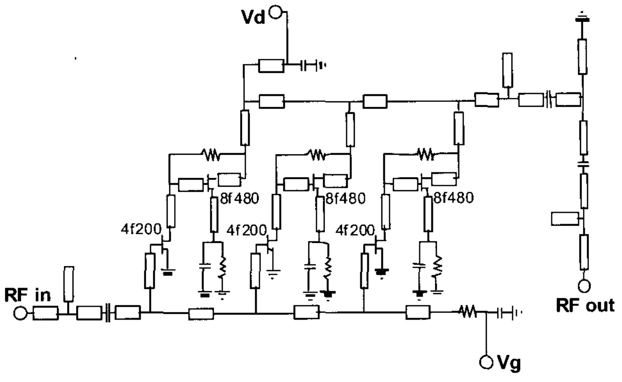
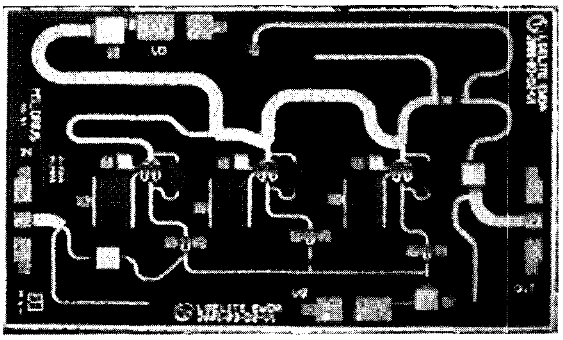


Fig. 3. Simulated S_{11} and of S_{22} of single 480-μm PHEMT and cascade active unit cell of drive amplifier.



(a)



(b)

Fig. 4. (a) Schematic and (b) photograph of 3-section distributed drive amplifier (2.9mmX1.9mm).

53 Ω at source. These feedback resistor values were determined for high stability and high gain in distributed amplifier. Moreover, the P_{1dB} output power was also considered to be more than 22 dBm at the amplifier. The conventional drain termination resistor was eliminated for improving output power in this distributed amplifier topology. Fig. 2 shows the maximum available gains (MAG) and stability factors (K) of single 480-μm PHEMT and the proposed cascade active unit cell described above, respectively. The performances of MAG and K of the cascaded active unit cell are better than those of 480 μm PHEMT. The MAG is more than 25 dB at 5-20 GHz and the K is larger than 1 over all frequency ranges. These results clearly indicate that the proposed cascade active unit cell can be well used for high gain with high stability in a wideband distributed amplifier. The simulated S_{11} data of Fig. 3 show that the input gate capacitance of the cascade active unit cell is less than that of single 480-μm PHEMT, increasing the higher cutoff frequency of gate line in distributed amplifier. Fig. 4 shows schematic and photograph of a 3-

section distributed drive amplifier. This amplifier consists of one stage, results in simple impedance matching for good gain flatness as well as high gain. Moreover, the self-biasing circuit reduces chip size as much as 2.9 mm x 1.9 mm.

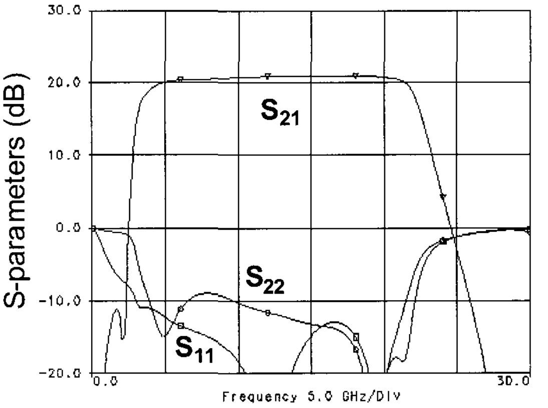


Fig. 5. Simulated small signal s-parameters of drive amplifier.

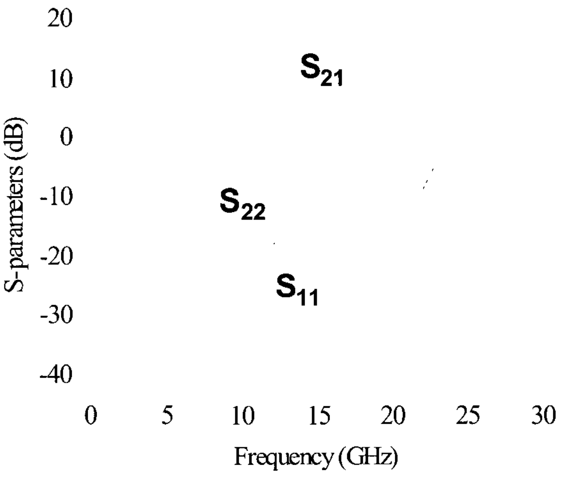


Fig. 6. Measured small signal s-parameters of drive amplifier.

Fig.5 shows the simulated small signal s-parameters of the drive amplifier. S_{11} is less than -12 dB and S_{22} less than −9 dB over 5-22 GHz. And also the small signal gain is 20 ± 0.5 dB in the same frequency range. The applied bias is V_g= -0.55 V, V_d= 8 V, and I_d= 290 mA. Fig.6 shows the measured small signal s-parameters of the drive amplifier. At bias of V_g= -0.55 V, V_d=8 V, and I_d=300 mA, S_{11} and S_{22} are less than −10.5 dB, and S_{21} is 16 ± 0.6 dB over 5-21 GHz. As shown in Fig.7, P_{1dB} is more than 22.0 dBm over 6-18 GHz. It is expected that the difference of small signal gain between simulation and measurement is mainly due to the used model error and transconductance variation of PHEMT in fabrication process.

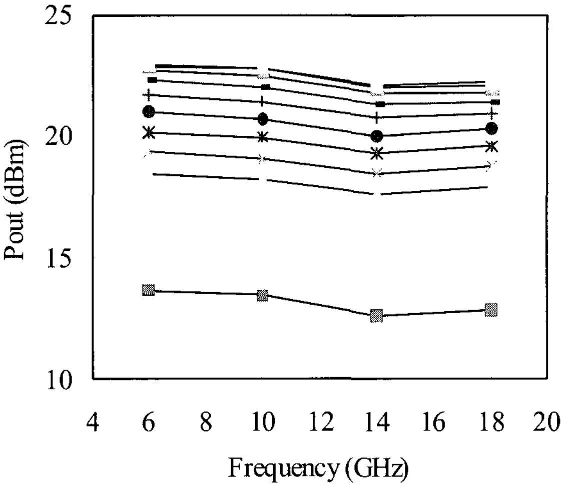


Fig. 7. Measured output power verse frequency when input power is swept in drive amplifier.

III. POWER AMPLIFIER

Fig. 8 shows the schematic of the distributed active unit cell in power amplifier. The gate termination resistor of 10 Ω was connected at gate line but drain termination resistor was eliminated at drain line for high output power in this distributed amplifier topology. The low gate termination resistor of 10 Ω was determined for increasing the cutoff frequency of low-pass type gate line. Using the series capacitor (3.5 pF) at gate of PHEMT also results in higher cutoff frequency of gate line because of the reduced total shunt capacitance of gate line. Considering higher loss of amplifier module at high frequency, the frequency-dependent gain and output power of this distributed active unit cell were optimally designed by controlling the phase matching of gate and drain line, length of the drain bias line as a short-circuited shunt stub, and the additional gate series capacitor. Load pull simulation was employed for maximum output power of the distributed active unit cell in determining the parameters described above. Gate bias is applied through resistor of 250 Ω.

Fig. 9 shows the maximum available gains (MAG) and stability factors (K) of single 480-μm PHEMT and the distributed active unit cell of power amplifier, respectively. In the distributed active unit cell, the MAG

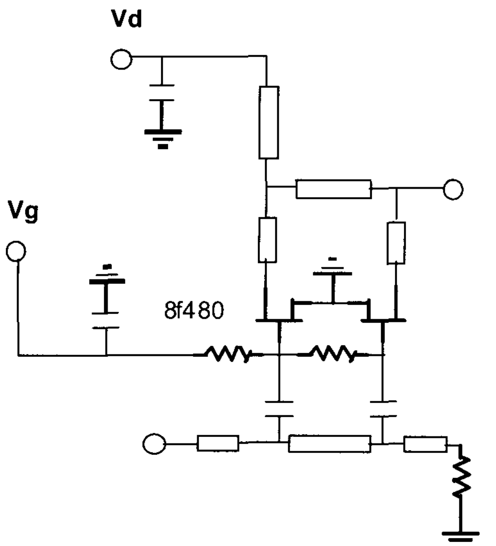


Fig. 8. Schematic of the distributed active unit cell in power amplifier.

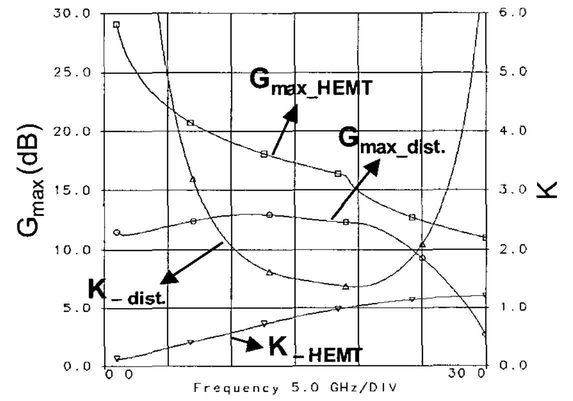


Fig. 9. Maximum available gains (MAG) and stability factors (K) of single 480-μm PHEMT and distributed active unit cell of power amplifier.

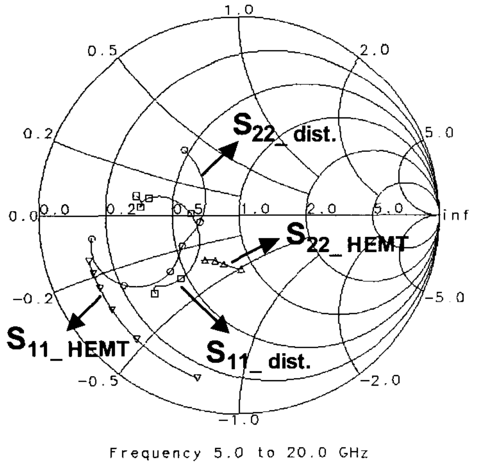
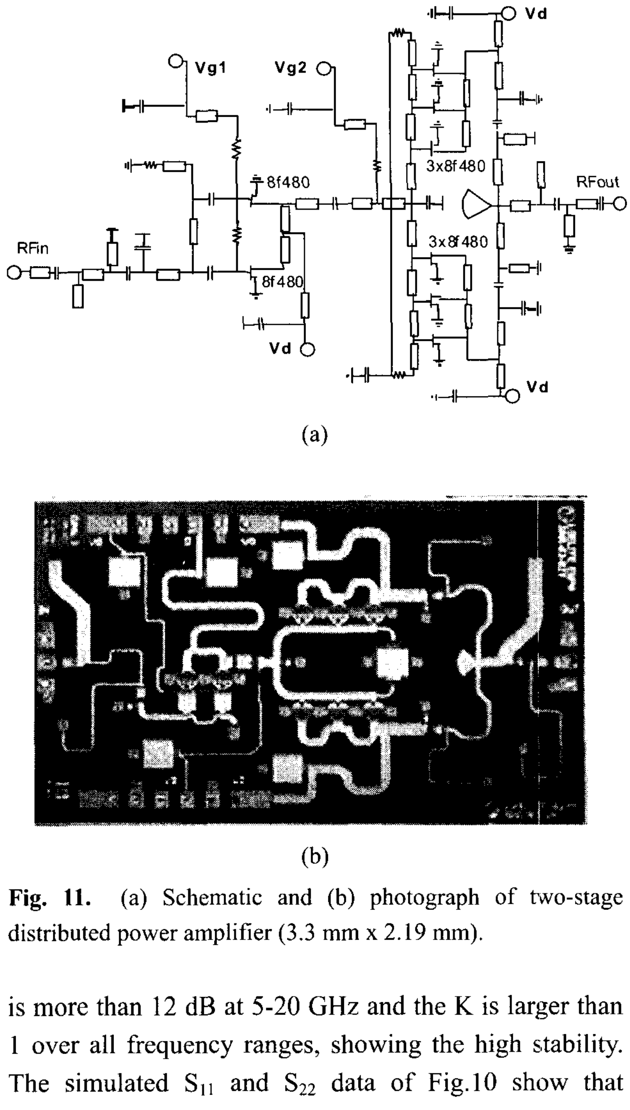


Fig. 10. Simulated S_{11} and S_{22} of single 480-μm PHEMT and distributed active unit cell of power amplifier.



(a)

(b)

Fig. 11. (a) Schematic and (b) photograph of two-stage distributed power amplifier (3.3 mm x 2.19 mm).

is more than 12 dB at 5-20 GHz and the K is larger than 1 over all frequency ranges, showing the high stability. The simulated S_{11} and S_{22} data of Fig.10 show that cascading the distributed active unit cells through only an additional short transmission line is able to make a conjugate impedance matching at inter-stage simultaneously. This results in a self impedance matching at inter-stage and also reduces the chip size in a multi-stage amplifier. And thereby the sensitivity to process variation is lower and also gain flatness is improved. Fig. 11 shows the schematic and photograph of the two-stage distributed power amplifier. Total gate widths of PHEMT are 2 x 480 μm at 1st stage and 6 x 480 μm at 2nd stage, respectively. The self impedance matching was realized through a series capacitor and a short transmission line at inter-stage. High-pass, low-pass networks were employed at input and output stages for compact wideband impedance matching networks in the power amplifier. The chip size is 3.3 mm x 2.19 mm.

Fig.12 shows the simulated small signal s-parameters of the 2-stage power amplifier. Both S_{11} and S_{22} are less

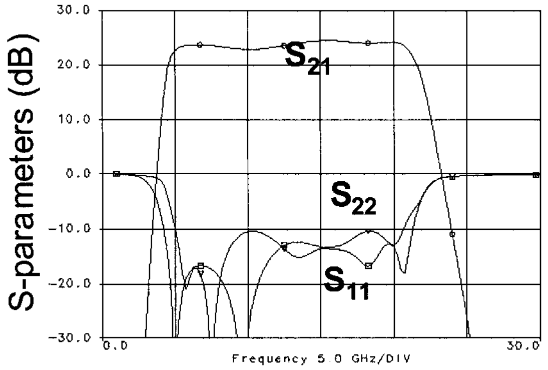


Fig. 12. Simulated small signal s-parameters of power amplifier.

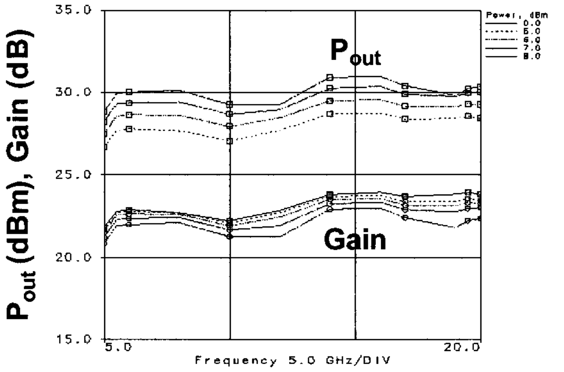


Fig. 13. Simulated output power verse frequency when input power is swept in power amplifier.

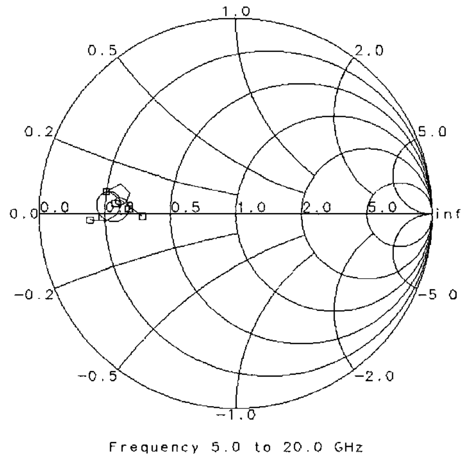


Fig. 14. Simulated load impedance seen by output of distributed active unit cell (3 x 480 μm PHEMTs) in power stage at 5-20 GHz.

than –10 dB over 5-20 GHz. The small signal gain is 22 ± 0.85 dB in the same frequency range. The bias is V_g= -0.5 V, V_d= 4.5 V, and I_d= 640 mA. The simulated output power verse frequency is shown in Fig.13. The P_{1dB} is more than 29 dBm over 6-18 GHz. Fig.14 shows the simulated load impedance seen by output of the distributed active unit cell (3 x 480 μm PHEMTs) in power stage. The wideband load impedance around 11 + j1.5 Ω is well achieved using the high-pass and loss-pass networks over 6-18 GHz. Fig.15 shows the measured small signal s-parameters of the power amplifier. Bias condition was selected for maximum P_{1dB} over 6-18 GHz. At bias of V_{gs1}= -0.3 V, V_{gs2}= -0.8 V, V_{ds}= 5.5 V, and I_d=280 mA, S_{11} is less than –10 dB and S_{22} is less than –6 dB over 6-18 GHz. S_{21} is 18.5 ± 1.25 dB. Fig.16 shows the measured power gain according to output power at 6 -18 GHz. P_{1dB} is more than 28.8 dBm and P_{sat} is about 30.0 dBm over 6-18 GHz. The correspondent power gain is 18.5 ± 1.45 dB up to P_{1dB}. Fig.17 shows the measured output power verse frequency when the input power is swept in power amplifier. As shown in Fig.16 and 17, the gain and maximum output power of the power amplifier gradually increase as frequency goes up. This helps to compensate the high frequency loss at a power amplifier module. The power added efficiency has been measured under CW condition. As shown in Fig.18, the PAE at P_{1dB} is between 19 % and 23 % over 6-18 GHz and compare very well with other best works [3]-[4].

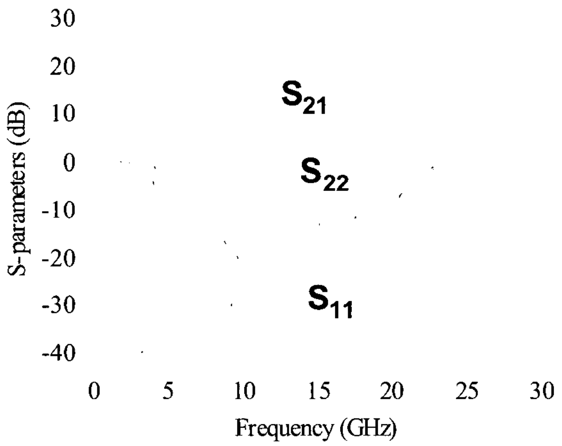


Fig. 15. Measured small signal s-parameters of power amplifier.

IV. CONCLUSINS

We have reported on the design and performance of drive and power MMIC amplifiers covering 6-18 GHz. Modified distributed topologies are employed in the both

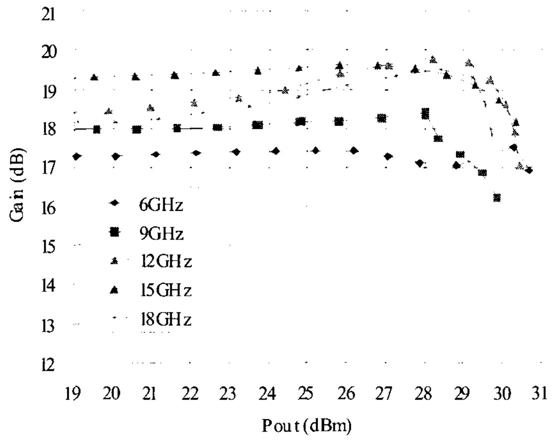


Fig. 16. Measured large signal gain verse output power at 6 - 18 GHz.

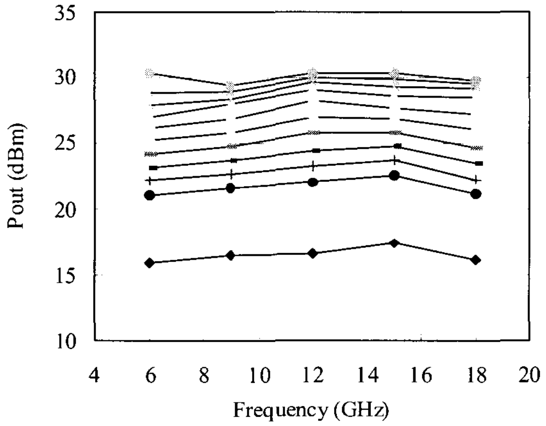


Fig. 17. Measured output power verse frequency when the input power is swept in power amplifier.

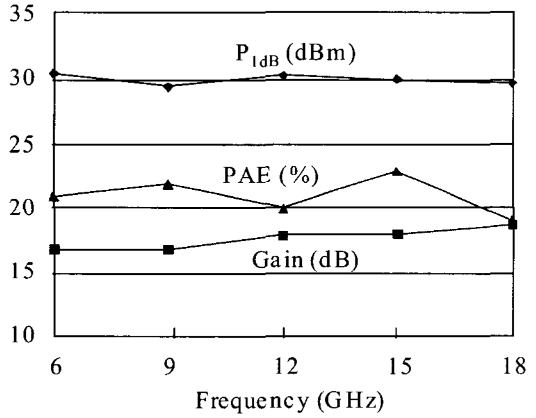


Fig. 18. Measured P_{1dB} and PAE at P_{1dB} verse frequency.

amplifiers, in which self-biasing and self-matching networks result in high stability, simple impedance matching, and small chip size. The drive amplifier with self-basing resistors showed good return losses (S_{11} , S_{22} < -10.5 dB), gain flatness (S_{21}= 16 ± 0.6 dB), and P_{1dB} > 22 dBm at 6-18 GHz. The power amplifier with self impedance matching and high-pass, low-pass impedance matching networks achieved the P_{1dB} >28.8 dBm and P_{sat} ≈ 30.0 dBm with good small signal characteristics (S_{11} < -10 dB, S_{22} < -6 dB, and S_{21}= 18.5 ± 1.25 dB) over 6-18 GHz. The PAE at P_{1dB} of power amplifier is between 19 % and 23 % over 6-18 GHz and compares very well with other best previously reported results.

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Youngwoo Kwon was born in Korea, in 1965. He received the B.S. degree in electronics engineering at Seoul National University in 1988, and the M.S. and Ph.D. degrees in electrical engineering from The University of Michigan, Ann Arbor, in 1990 and 1994, respectively. From 1994 to 1996, he was with Rockwell Science Center, where he was involved in the development of various millimeter-wave monolithic integrated circuits based on HEMT's and HBT's. In 1996, he joined the faculty of School of Electrical Engineering, Seoul National University, His current research activites include the design of MMIC's for mobile communication and millimeter-wave systems, large-signal modeling of microwave transistors, application of micromachining techniques to millimeter-wave systems, nonlinear noise analysis of MMIC 's and millimeter-wave power combining.

Moon-Suk Jeon received the M.S. degree in electronics engineering at Seoul National University in 2002. He is currently working for WAVICS Co. Ltd. His current research is MMIC power amplifier design with high efficient and high linearity.

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