Fabrication of Micro-inductor and Capacior For RF MEMS Applications

Bek-Hee Cho, Jae-Ho Lee, Young-Ho Bae, Chan-Sub Cho, and Jong-Hyun Lee

Abstract— **In this paper, we present the fabrication of tunable capacitors and 3-dimensional inductors. This work was related to fabricated 3-dimensional device for need of micro device in developing new intelligence age. This device was fabricated by electroplating used electroplating PR and high-vacuum evaporation of metal. Fabricated micro-inductor is consisted of air-bridge on electroplating rod and electroplated core. Micro-capacitor is consisted of thin metal membrane and electroplated core. Electroplating material is used Cu metal solvent. Air-gap between metal-layers function as almost perfect isolation layer. The most advantage of our micro-inductor and micro-capacitor compared to present device is a possibility that can fabricate on RF MEMS(microelectro-mechanical systems) application with high performance and various function. In this paper, we present the fabrication of tunable capacitors and 3-dimensional inductors. This work was related to fabricated 3-dimensional device for need of micro-device in developing new intelligence age. This device was fabricated by electroplating used electroplating PR and high-vacuum evaporation of metal. Fabricated micro-inductor is consisted of air-bridge on electroplating rod and electroplated core. Micro-capacitor is consisted of thin metal membrane and electroplated core. Electroplating material is used Cu metal solvent. Air-gap between metal-layers function as almost perfect isolation layer. The most advantage of our micro-inductor and micro-capacitor compared to present device is a possibility that can fabricate on RF MEMS application with high performance and various functions.**

Index Terms — **RF MEMS, Inductor, Capacitor.**

I. INTRODUCTION

Nowadays RF active and passive devices have been developed. Using these devices, satellite communication, mobile phone, data communication, local area network and satellite broadcasting etc. have been grown rapidly. For these applications, present devices tend to be minimized, low-powered and low-cost. Also standard passive devices, resistor, capacitor and inductor are tried to integrate. [1][2] Resistor of these passive devices is succeeded to integrate already. But RF application inductor and capacitor have many problems to integrate. So many researchers are studying in these devices. It is effect that micro-inductor is fabricated 3-dimensionally for its hysterisis. If inductor is integrated, inductor is able to include in one-chip without extra-interface. It is important that it is realized desired inductance and Q-factor for integration and one-chip packaging of inductor. Because present inductor is fabricated by individual packaging, it is had defect that interface problem, low efficiency and high cost. [3][4] In case of capacitor, conventional capacitor has been made use of capacitance variation with respect to air-gap variation using PN structure, MOS structure etc. But these capacitance

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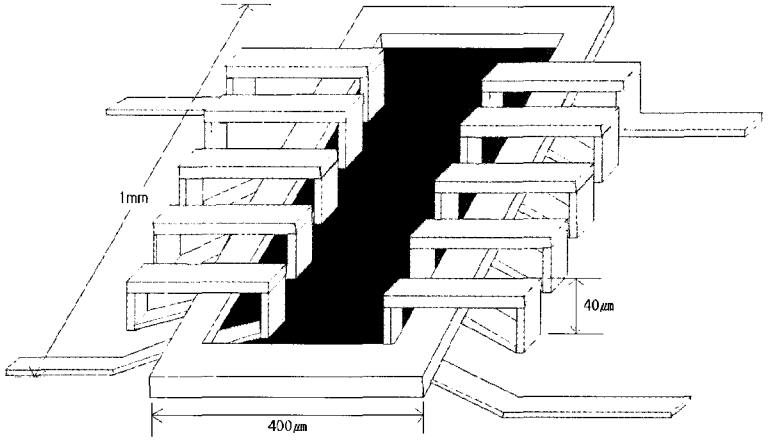

Fig. 1. Designed micro-inductor.

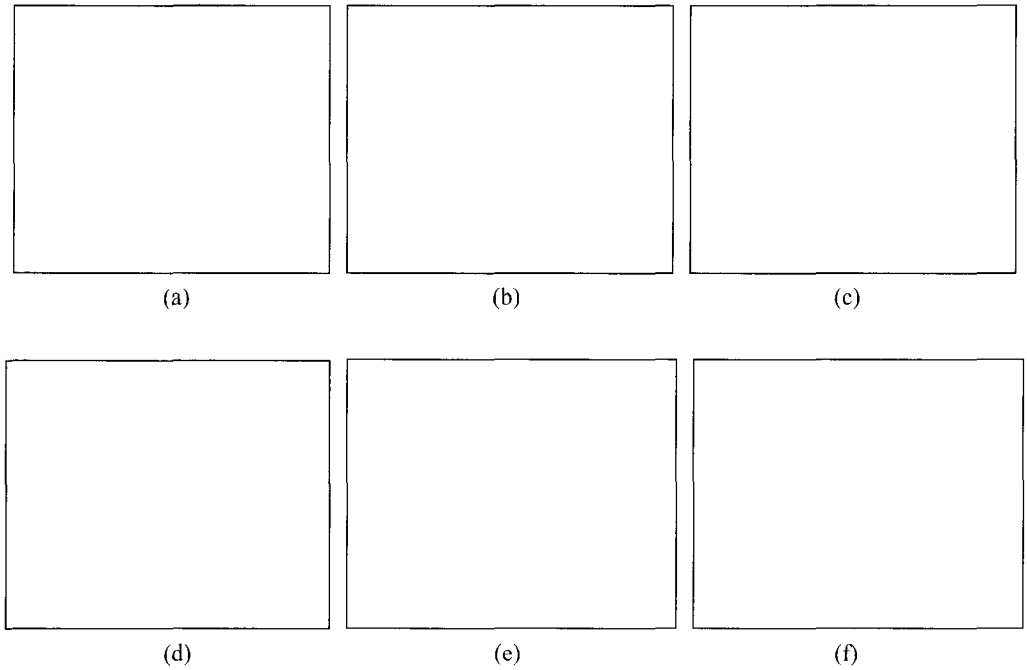

Fig. 2. The mask layout of 3-Dimensional micro-inductor (a) Basic metal line define (b) 1st electroplating define (c) Core insertion define (d) 2nd electroplating define (e) Air-bridge define (f) Basic metal line removal define.

variations are required very high driving voltage and are controlled difficultly. So conventional capacitor is applied to limited electrical area. In particular, conventional capacitor isn't able to apply in accordance with a few MHz to a few GHz. Parallel-plate capacitor using metal thin film is effectively for RF region applications. [5][6]

For solving problems of above representation, in this paper, 3-dimensional inductor and variable capacitor is fabricated using MEMS technology. In point of 3-dimensional structure, insulating-developed solenoid inductor is fabricated with air-gap between metal lines. After metal evaporating on silicon wafer Cu metal layer is formed using Cu electroplating. For efficiency of inductor core is inserted and finally using air-bridge forming method micro-inductor is fabricated. Also using MEMS technology and Cu electroplating with low-resistivity variable capacitor is fabricated with CPW(coplanar waveguide) for RF communication network. Signal line of CPW is used to lower electrode of capacitor and upper electrode of capacitor with Cu electroplating is made. So applied voltage between

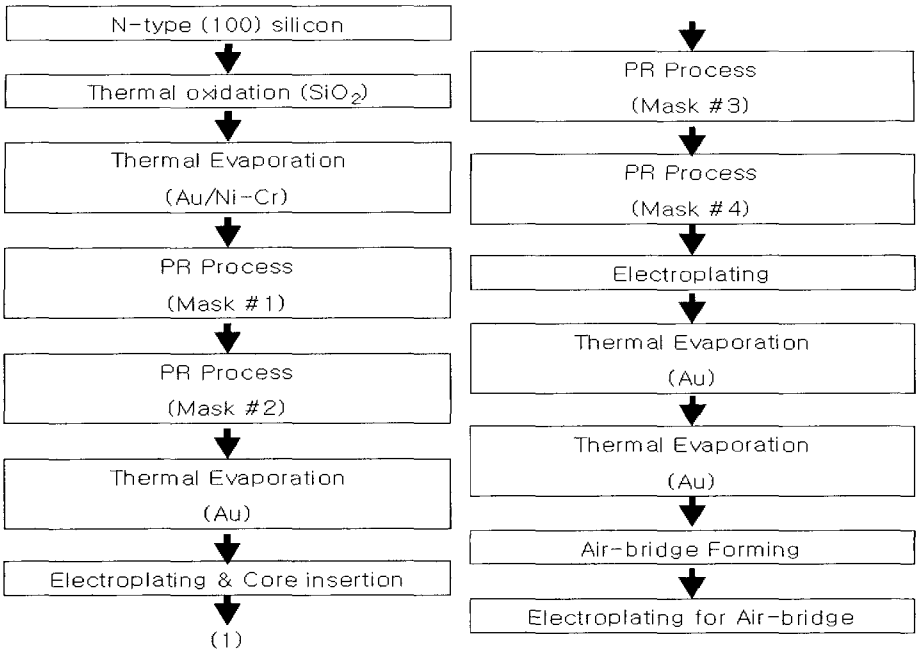

Fig. 3. The fabrication flow chart of micro-inductor.

electrodes is affected displacement of upper electrode. An according with its displacement, distance of electrodes and capacitance is varied. Thus, capacitance of variable capacitor is tested and analyzed with respect to applied voltage.

II. Design and Experiment of Proposed Devices

A. *Micro-inductor*

Fig. 1 is proposed inductor shape for desired characteristics. It has 50 μm width of bottom metal line, 30 μm width of metal bridge, 20 μm height of electroplating post for reinforcement of physical strength. Fig. 2 is the mask layout of 3-dimensional micro-inductor and include basic metal line define (2-a), 1st electroplating define (2-b), core insertion define (2-c), 2nd electroplating define (2-d), air-bridge define (2-e), basic metal line removal define (2-f). it is designed that height of micro-inductor has 40 μm height when be fabricated. Metal line between inductor devices for Cu electroplating is removed in final process and gap between metal layers is consist of air-gap for insulating-development. Fig. 3 is the drawing of fabrication flow chart of 3-dimensional micro-inductor and Fig. 4 is the drawing of cubic fabrication process. First N-type (100) silicon wafer is oxidized due to develop insulating between device and silicon substrate. Insulating between device and silicon substrate is very important for performance of device. After initial cleaning silicon wafer, Ni-Cr and Au are evaporated on front side of silicon wafer with In-situ method. With this silicon wafer, PR spin coating is done, UV light is exposed and Au/Ni-Cr is etched. Using electroplating PR, area which will be electroplated is defined and 20 μm height of Cu film is shaped by Cu electroplating. And then Au film is evaporated again for core forming. For obtaining thick core metal, electroplating is performed again. Repeatedly Cu electroplating is performed and Au air-bridge film is evaporated. Cu electroplating is performed again for reinforcement of physical strength of air-bridge. Because the rate of expansion of metal film on PR is different to that of PR, it is easy to crack when thermal evaporating. For solve this thermal problem, it must be get rid of humidity of PR. It is required additional mask that remove inserted metal lines because of metal lines for electroplating. In this process, because height of device is over 40 μm, thickness of PR is over 40 μm for one spin-coating process. So UV light expose is taken very

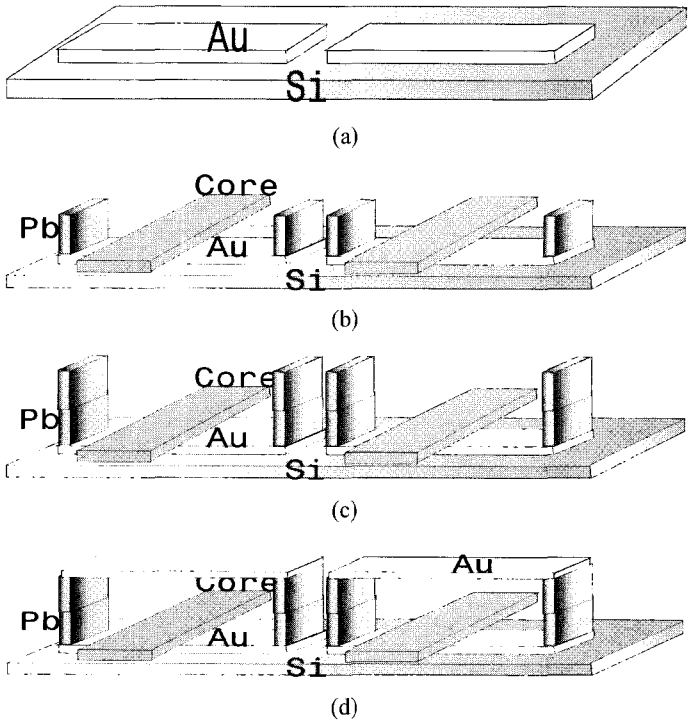

Fig. 4. The cubic fabrication process of micro-inductor. (a) Basic metal line Fab. (b) 1st electroplating & Core Fab. (c) 2nd electroplating. (d) Air-bridge Fab.

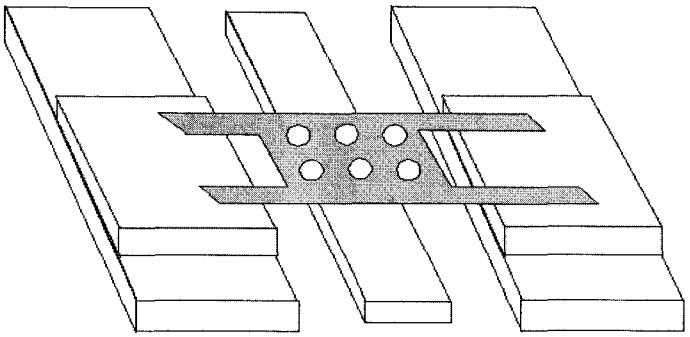

Fig. 5. Proposed variable capacitor.

long time and in this paper we take 300 seconds for UV light expose with electroplating PR. As result of above process 3-dimensional micro-inductor is fabricated. At final process PR is removed for air-gap between metal lines.

B. *Micro-capacitor*

Fig. 5 is the designed variable capacitor that is proposed in this paper. And designed variable capacitor has 4 beam of 30 μm × 95 μm area and 1 membrane of 200 μm ×200 μm area. Membrane, as say above, is behaved like upper electrode and CPW is behaved like lower electrode for MMIC applications. Also designed capacitor has 200 μm × 700 μm signal line, 400 μm × 700 μm ground line and 50 μm distance between signal line and ground line. Fig. 6 is the mask layout for fabrication of variable capacitor and include basic metal line define (6-a), PR process define for 1st Cu electroplating (6-b), Cr removal define between signal line and ground line (6-c), Si_3N_4/Au pattering define for maximum capacitance (6-d), 2nd Cu electroplating define for making of air-gap between upper electrode and lower electrode (6-e), Au metal layer define for Cu

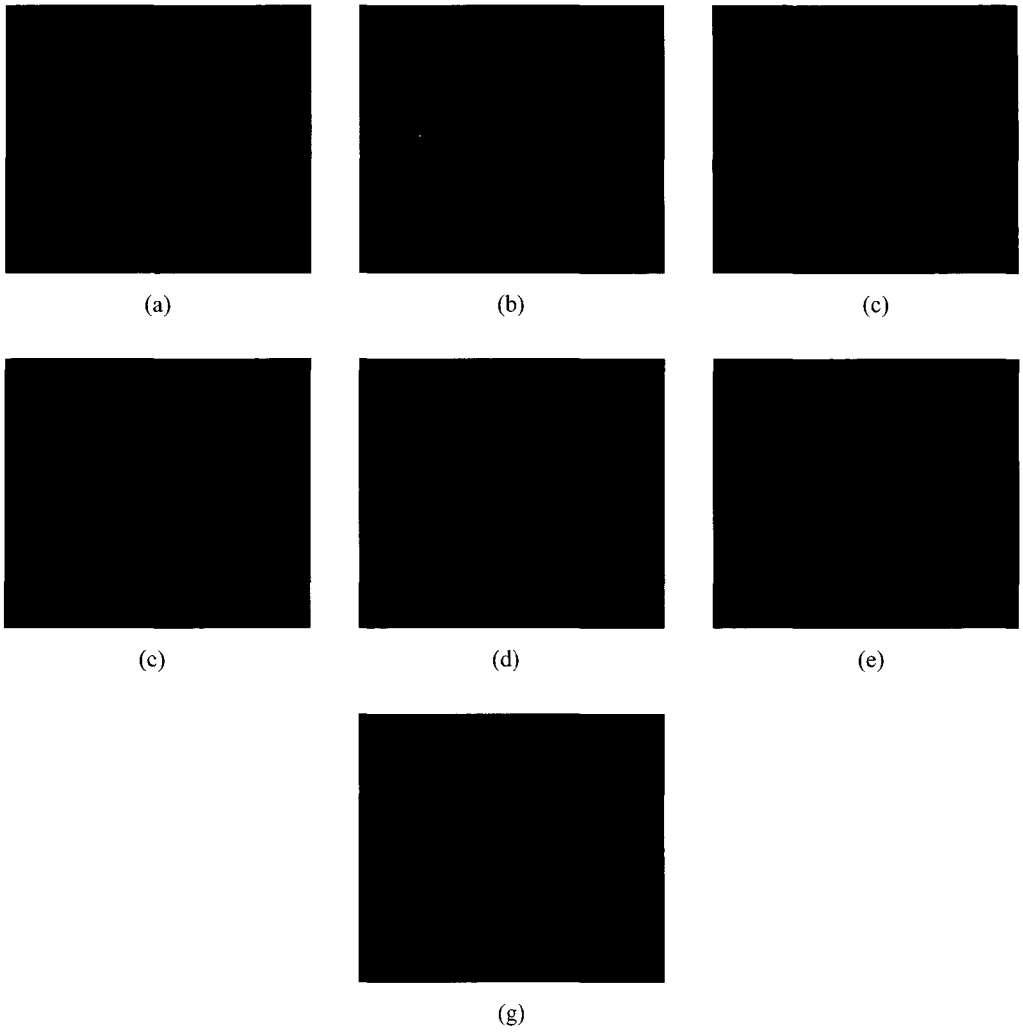

Fig. 6. The mask layout of variable capacitor (a) Basic metal line define (b) 1st electroplating define (c) The removal of Cr between electrode (d) Si_3N_4/Au pattern define (e) 2nd electroplating define (f) Au metal layer define (g) 3rd electroplating define.

electroplating of upper electrode (6-f), 3rd Cu electroplating (6-g). Fig. 7 represent the fabrication flow chart of variable capacitor and Figure 8 represent the fabrication process of variable capacitor in side-view. It is used that Corning 1737 glass substrate has 500 μm thickness for insulating characteristics and lowering substrate loss. After initial cleaning of Corning 1737 glass substrate, glass substrate is evaporated Cr with 400 Å thickness and Au with 1300 Å thickness in In-situ. After Lower electrode is formed by lithography method and Au selective removal, lower electrode is defined by AZ 1512 PR lithography. 1.5 μm Cu electroplating layer is obtained by that during 450 seconds current of 5 mA is flowed to sample in copper sulfate solvent. Cr film on substrate between signal line and ground line is removed selectively for preventing of needless electroplating. After Si_3N_4 with 3500 Å thickness is deposited by PECVD instrument for preventing of electric short between upper electrode and lower electrode, Au with 3500 Å thickness is evaporated by thermal evaporator and then Au film is removed by Au etchant. Area which Cu electroplating will be performed is defined for air-gap of capacitance variation using electroplating PR and 2 μm Cu electroplating post is formed by that during 300 seconds current of 5 mA is flowed to sample in copper sulfate solvent. Au film is deposited by thermal evaporator. And 0.5 μm Cu electroplating film is performed on Au film with 120 seconds. After 3rd Cu electroplating, PR is removed for air-gap between metal layers. Finally

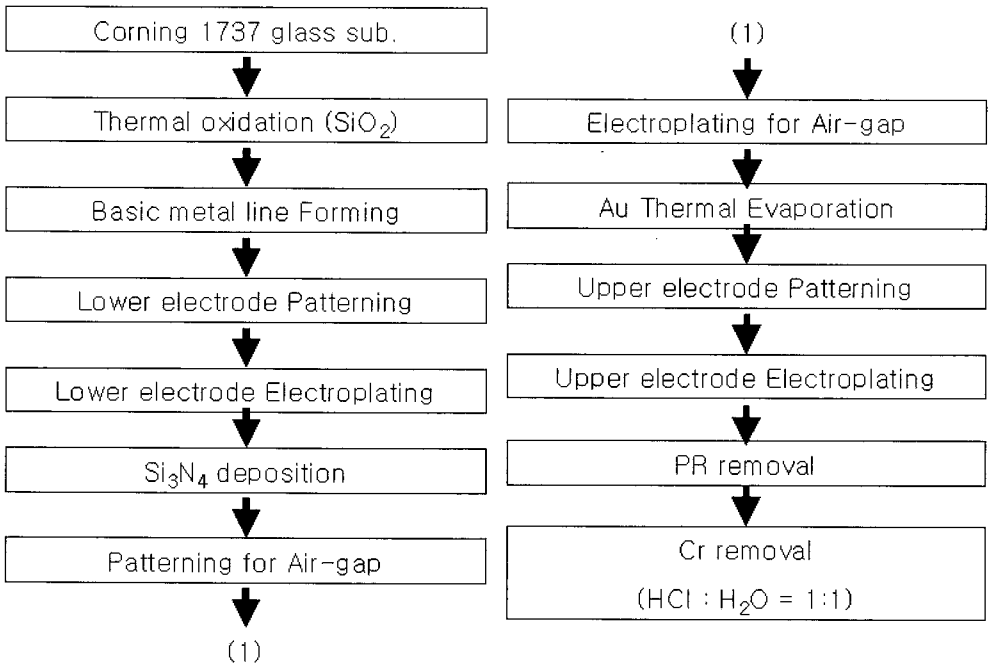

Fig. 7. The fabrication flow chart of variable capacitor.

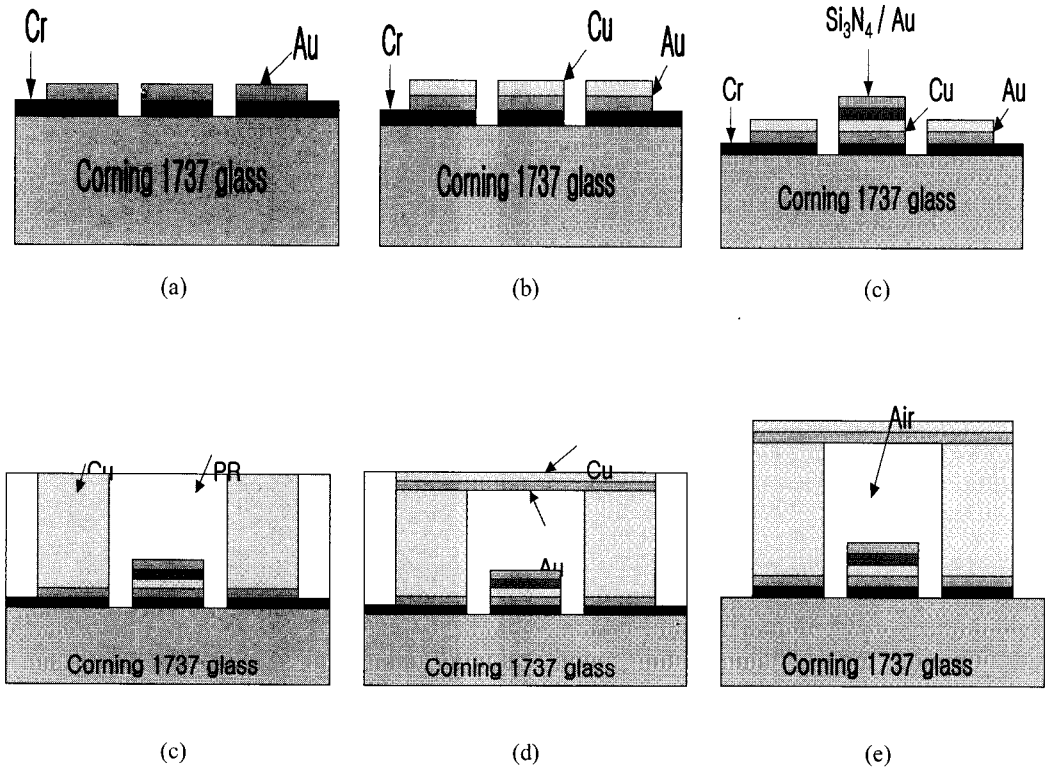

Fig. 8. The fabrication process of variable capacitor (a) Basic metal line Fab. (b) 1st electroplating & Cr removal (c) Si_3N_4/Au evaporation (d) 2nd electroplating (e) 3rd electroplating (f) PR removal.

through the above processing, variable capacitor is fabricated.

III. Expriment Result

A. *SEM analysis of proposed devices*

Fig. 9, 10 and 11 represent unit process of fabrication of 3-dimensional micro-inductor. Fig. 9 is SEM photography after UV exposure with electroplating PR. Height of electroplating PR is 20 times height of general PR. Thus electroplating PR is required to control aspect ratio. In this paper, aspect ratio of PR is 5. Fig. 10 and 11 represent SEM photography of air-bridge. It is performed Cu electroplating 5 μm in figure 10, 1 μm in Fig. 11 respectively for reinforcement of physical strength of air-bridge. An air-bridge of figure 10 and 11 has 400 μm length with air-gap between metal layers. Fig. 12 is SEM photography of unit process of core insertion and core has a 400 μm × 1000 μm area. Figure 13 is SEM photography of fabricated 3-dimensional micro-inductor. Fig. 14 present SEM photography of variable capacitor in view of front side and Variable capacitor has four beam of 30 μm × 95 μm area and upper electrode of 200 μm × 200 μm area.

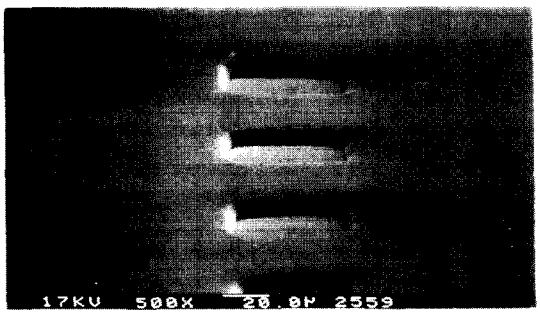

Fig. 9. The SEM photograph after exposure of electroplating PR.

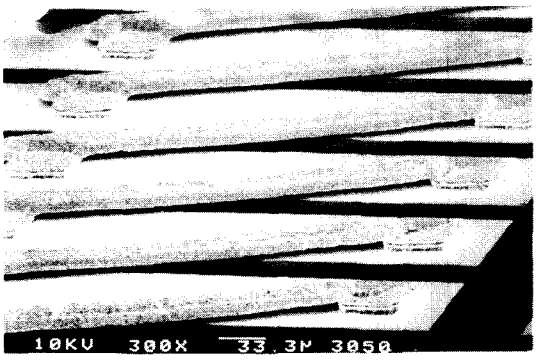

Fig. 10. The SEM photograph after fabrication of air-bridge.

Fig. 11. The SEM photograph after fabrication of Cu thin film.

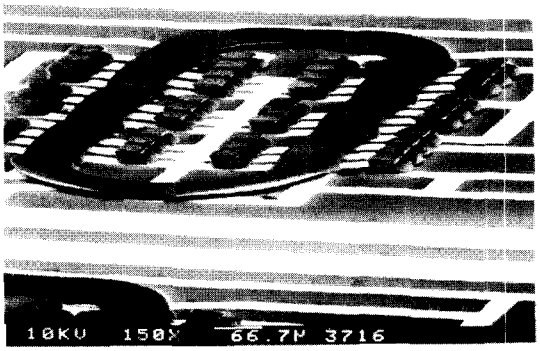

Fig. 12. The SEM photograph of fabricated core.

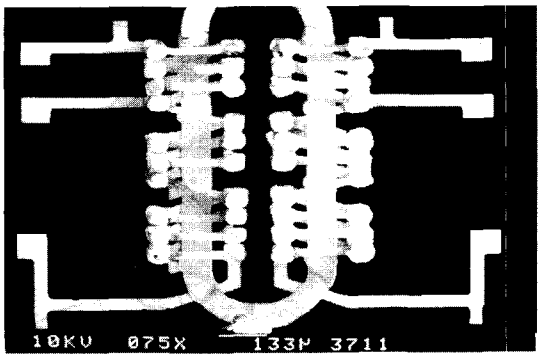

Fig. 13. The SEM photograph of 3-dimensional micro-inductor

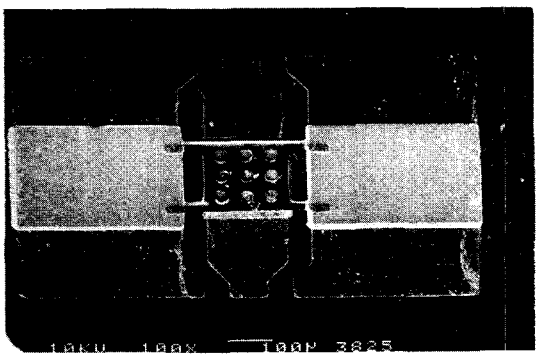

Fig. 14. The SEM photograph of fabricated variable capacitor.

B. *Electric characteristics of proposed devices*

For analyze characteristics of fabricated 3-dimensional micro-inductor, it is used HP4194A impedance/gain-phase analyzer. Gain and phase shift of micro-inductor is tested with variation of 10Hz to 100MHz frequency. Fig. 15 represent SEM photograph of tested micro-inductor with HP4194A impedance/gain-phase analyzer. For test of capacitance of variable capacitor with respect to applied voltage, it is used HP4280A C-V instrument. Fig. 16 represent drawing of capacitance varications with respect to applied voltage and represent calculated value and measured value respectively. Measured capacitance is changed between 1.367 pF~2.245 pF when voltage apply 0 V~42 V and change ratio of capacitance is shown by 64.2%.

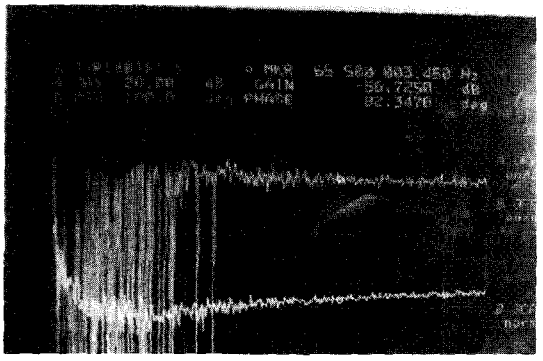

Fig. 15. View of HP4194A impedance/gain-phase analyzer in testing.

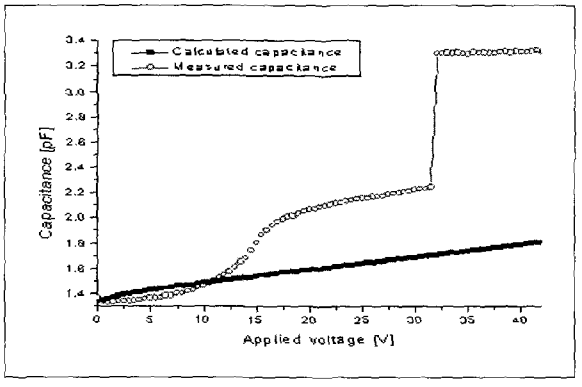

Fig. 16. The measured capacitance with respect to voltage.

IV. Conclusion

In this paper, it is proposed that method of fabrication of 3-dimensional micro-inductor and variable capacitor using MEMS technology and Cu electroplating technique. Micro-inductor and variable capacitor are fabricated on N-type silicon wafer and Corning 1737 glass substrate respectively. Two devices are made with repeated general lithography, Cu electroplating and metal evaporating process. First we established relation between Cu electroplating time and Cu electroplating current and perform an experiment of electroplating PR with UV exposure time. The proposed inductor has 1 mm width, 1 mm length and 30 μm height. Moreover proposed capacitor has 200 μm × 700 μm signal line, 400 μm × 700 μm ground line and 50 μm distance between lines. It is used that HP4194A impedance/gain-phase analyzer and oscilloscope for measurement of micro-inductor. And it is obtained voltage gain and phase shift of micro-inductor in test. Besides fabricated variable capacitor is measured with HP 4280A C-V instrument. When voltage between electrodes of capacitor change 0 V ~ 42 V, capacitance of capacitor has 1.367 pF~2.245 pF change ratio.

Now we are researching an experiment that fabricate both inductor and capacitor on one substrate with development of RF MEMS application resonator, filter etc.

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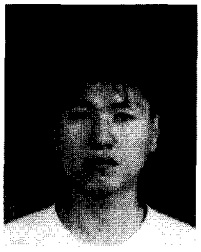

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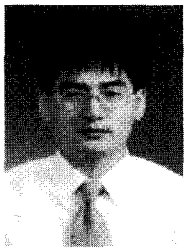

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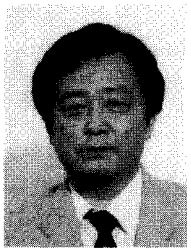

Jong-Hyun Lee was born in Taegu, Korea on 1949. He attended Kyungpook National University (KNU) where he received the Bachelor and the Master of Engineering in Electronics in 1972, 1976, respectively. He was awarded his **Docteur d'Ingenieur** in electronics from ENSERG-INP, Grenoble, France, in 1981. He joined the School of Electronic & Electrical Engineering at KNU, in 1982, where he taught courses in semiconductor physics, electronic devices, integrated circuits fabrication process, and electronic materials. Between 1994 and 1997 he has served as director of the school, and he is now professor.