A Simple and Analytical Design Approach for Input Power Matched On-chip CMOS LNA

Tae Wook Kim and Kwyro Lee

Abstract— **A simple and analytical design approach for input power matched CMOS RF LNA circuits and their scaling for lower power consumption, is introduced. In spite of the simplicity of our expressions, it gives excellent agreement with numerical simulation results using commercial CAD tools for several circuit examples performed at 2.4GHz using 0.18μm CMOS technology. These simple and analytical results are extremely useful in that they can provide enough insights not only for designing any CMOS LNA circuits, but also for characterizing and diagnosing them whether being prototyped or manufactured.**

Index Terms — **Low Noise Amplifier, Low Power CMOS RF Amplifier, Noise Figure, Input Power Matching, Source Degeneration.**

I. INTRODUCTION

Low noise amplifier (LNA) is an important building block in RF communication system. Noise figure (NF) of LNA dominates the sensitivity of whole receiver system[1]. Since modern communication system demands more and more stringent requirement of NF and higher degree of integration [2]-[6], NF optimization of fully integrated on-chip LNA where the quality and size of integrated inductor are very limited, is an important issue nowadays.

In LNA design, input power matching is necessary not only for obtaining higher gain, but for reducing signal distortion due to reflection. In all common source type FET(CSFET) circuits including MESFET and MOSFET, it is well known, however, that it is hard to match both gain and NF simultaneously. Therefore there are two approaches in LNA design, i.e. either input power matching is traded off after NF minimization or vice versa. CSFET with input noise matching is the most popularly used circuit topology for the former case [3]. As far as the authors know there are two ways for the latter case. One is to use source degeneration inductor [4]-[6] and the other is to use various negative feedback [7]. The former gives excellent NF but less gain, and vice versa for the latter. In source degeneration LNA (SDLNA), simultaneous matching can be achieved by resistive input impedance effectively provided by inductor degeneration and by input matching inductor which cancels out capacitive impedance of CSFET.

In most of LNA circuits, therefore, inductor loss is one of the major contributors to the total noise figure as well as the gain. This is especially true for on-chip inductor where its quality factor is quite lower than that of an external inductor. When external high quality inductor is available, CSFET with smaller transistor width whose large impedance can be cancelled by larger input matching inductor is favorable because it provides large input voltage boosting without generating large thermal noise from the parasitic resistance in the matching inductor. Note, in this case, that it can effectively suppress channel thermal noise down, which is the major CMOS transistor noise source. But in on-chip LNA circuits, larger inductor leads to larger series resistance that inevitably increases NF by input resistive loss. Thus there exists optimum transistor width.

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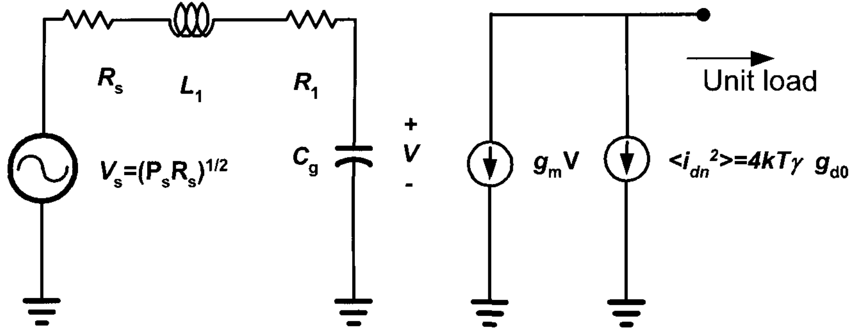

Fig. 1. Simplified equivalent circuit of CSLNA.

Because there are many circuit parameters involved in LNA design, its optimization is very complicated and thus routinely done using computer simulation. However, analytical design is always plausible, because it gives much more insight not only for circuit design at least in the first design targeting, but for the characterization and diagnosis for the prototyping and manufacturing circuits.

In this paper, we propose simple, analytical and systematic design approaches for on-chip CMOS LNA circuits. In Sec. II, we analytically derive noise sources, noise matching and minimum noise figure for CSFET and compare our formula with others developed earlier. These are then extended to SDLNA in Sec. III. In Sec. II, contrary to the Sec. II where NF optimization is firstly done, then gain is traded off, we start from input power matching using SDLNA and then minimize NF as much as possible in Sec. III. Section II introduces simple noise model for CSFET LNA (CSLNA) and then treats analytical transistor width optimization leading to NF minimum for given inductor quality factor. Section III studies analytical NF minimization approach for input power matched SDLNA, then, we extend this approach for lower power consumption in Section IV. Analytical approaches will also be compared with computer simulation using Agilent ADS CAD tool in Sec. IV, followed by conclusion.

II. Analytical NF Optimization Methods for ON-Chip CSLNA

Fig. 1 shows simplified equivalent circuit of CSLNA, where R_s is the source impedance, 50 Ω in most RF systems, R_l the parasitic series resistance of input matching on-chip inductor (L_l), C_g the gate capacitance of CSFET. Here drain channel current noise, $<i_{dn}^2>$, is due to the thermal noise generated by the carriers in the channel region [6], where k is the Boltzmann's constant and T is the absolute temperature. Here g_{d0} is the transistor output conductance when $V_{ds}=0$ [9] and γ is a constant. The value of γ is 2/3 in classical limit and may need to be replaced by larger value in short channel devices[10].

In Fig. 1, all other FET noise sources such as induced gate noise are ignored. Our recent unpublished work shows that drain noise dominates overall NF. Moreover, gate poly resistance is neglected because there are many ways to reduce it by layout techniques [11]. Substrate loss is also ignored because it can be reduced by such technique as bonding pad shielding [12].

The signal power delivered to the unit load, S, then, is given by,

$$S=\left| V_S \times \frac{jX_g}{R_S+R_1+j(X_1-X_g)} \times g_m \right|^2$$
$$=P_sR_S \times \frac{g_m{}^2 X_g{}^2}{(R_s+R_1)^2+(X_1-X_g)^2}. \quad (1)$$

Where , X_l and X_g are given by ωL_l and $1/\omega C_g$. Note that eq.(1) has maximum when $X_l=X_g$, and then it is proportional to $X_g^2/(R_s+R_l)^2$. In this case, input voltage is boosted by the input matching network. The higher the input matching quality factor in the input matching circuitry, the more signal power is delivered to load.

On the other hand, the noise power delivered to the unit load, N, is given by

$$N = 4kT(R_s + R_1)\times\frac{g_m^{\ 2}X_g^{\ 2}}{(R_s + R_1)^2 + (X_1 - X_g)^2} + 4kT\gamma g_{d0} \tag{2}$$

Combining eq. (1) and eq. (2) gives the following noise-to-signal power ratio,

$$\frac{N}{S} = \frac{4kT}{P_s}\times(1+\frac{R_1}{R_s}) + \frac{4kT\gamma}{P_s R_S} \times\frac{(R_S + R_1)^2 + (X_1 - X_g)^2}{g_m^{\ 2}X_g^{\ 2}}\times g_{d0} \tag{3}$$

Then, NF, can be calculated as follows from eq. (3),

$$\begin{aligned} NF &= \frac{N}{S}\times\frac{P_s}{4kT} \\ &= (1+\frac{R_1}{R_s}) + \gamma\frac{(R_S + R_1)^2 + (X_1 - X_g)^2}{g_m^{\ 2}X_g^{\ 2}}\times\frac{g_{d0}}{R_s} \\ &= 1 + \frac{R_1}{R_s} + \gamma f^2 \frac{(R_S + R_1)^2 + (X_1 - X_g)^2}{f_T^{\ 2}}\times\frac{g_{d0}}{R_s} \end{aligned} \tag{4}$$

In eq. (4), we replaced transistor equivalent circuit parameters, g_m and X_g, by unit short-circuited current cutoff frequency, f_T, using following definition,

$$\frac{f_T}{f} = g_m X_g \tag{5}$$

Clearly eq. (4) has minimum firstly when,

$$X_1 = X_g \tag{6}$$

Eq. (6) means that the reactance of the input capacitance(C_g) of transistor is exactly cancelled by that of the input matching inductor (L_l). In addition, CSLNA has global minimum NF when,

$$R_s = \sqrt{R_1^{\ 2} + \frac{R_1}{\gamma g_{d0}}\times\frac{f_T^{\ 2}}{f^2}} \tag{7}$$

The minimum NF, then, given by

$$NF_{\min} = 1 + \frac{\gamma f^2}{f_T^{\ 2}} g_{d0}(2R_1 + \sqrt{R_1^{\ 2} + \frac{R_1}{\gamma g_{d0}}\times\frac{f_T^{\ 2}}{f^2}}) \tag{8}$$

There are two interesting cases in the low frequency ($f \rightarrow 0$) limit.

i) When R_s cannot be matched as in eq. (7) because of small f, NF_{min} is approaching $1+ R_l/R_s$ (see eq. (4)). This is exactly the low frequency limit NF for CSLNA [9].

ii) When R_s is matched according to eq. (7), NF_{min} of eq. (8) is given by $1 + kf/f_T\sqrt{\gamma R_1 g_{d0}}$. Note that this is very close to Fukui model which was empirically proposed for MESFET [14].

Eq. (8) has many important implications for CSLNA. Firstly, it emphasizes that LNA should be operated in low V_{GS}-V_T regime, where g_{d0}/f_T^2 which is proportional to g_{d0}/g_m^2, is minimized. Secondly, as we can see in eq. (4), noise figure increases as the parasitic resistance of input matching inductor (R_l) increases and decreases as the value of g_{d0} decreases. It will be shown in following consideration that R_l is inversely proportional to input transistor width (W) while g_{d0} is proportional to W. Therefore there exists optimum input transistor width, which can analytically be found as below.

To find out optimum width of input transistor, let us first denote,

$$\gamma g_{d0} f^2/f_T^2 = g_{FET} W. \tag{9}$$

Typical value of g_{FET} at 2.4GHz for 0.18μm CMOS is $g_{FET} = 3.5\times10^{-3}(\Omega^{-1}mm^{-1})$ where, γ is assumed 1, $f_T/f \approx 10$, and $g_{d0} \approx 0.35S\ (\Omega^{-1})$ at $V_{GT}=0.2$V. Writing $C_g=C_{g0}W$ and $C_{g0}=1.75(pF/mm)$ which are typical for 0.18μm CMOS, the parasitic resistance R_l for the NF matching inductor satisfying eq. (6), can be represented by input transistor width (W) as follows,

$$R_1 \approx \frac{\omega L_1}{Q_L} = \frac{1}{Q_L}\times\frac{1}{\omega C_g} = \frac{R_0}{W} \tag{10}$$

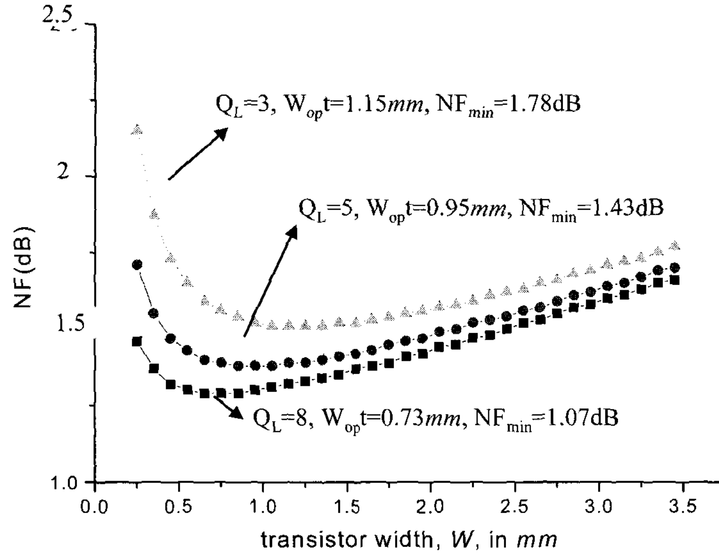

Fig. 2. Noise figure vs. input transistor width with various Q_L

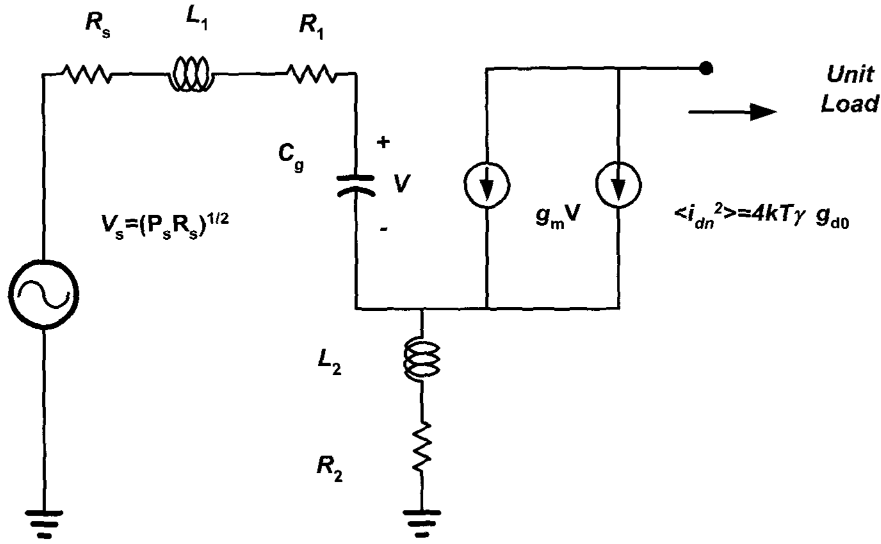

Fig. 3. Simplified equivalent circuit of SDLNA

Here Q_L is the on-chip inductor quality factor and

$$R_0=1/(\omega\ C_{g0}Q_L) \tag{11}$$

Typical values for 0.18μ m CMOS are of R_0= 4.7Ω - *mm* for Q_L= 8. Inserting eq. (9) and eq. (10) into eq. (4) leads to,

$$NF = 1+\frac{R_0}{R_sW}+g_{FET}R_sW \times\left(1+\frac{2R_0}{R_sW}+\frac{R_0^2}{R_s^2}\times\frac{1}{W^2}\right) \tag{12}$$

The last term in the parenthesis of eq. (12) is much smaller than others, then, eq. (12) reduces to the following simple eq. (13),

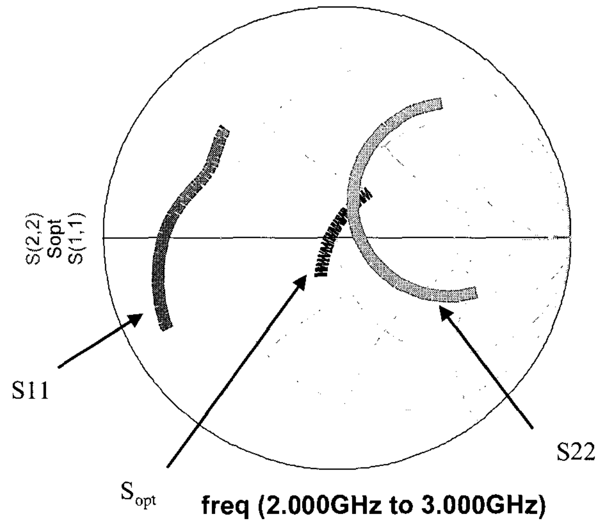

Fig. 4. S-parameter simulation result of NF matched CSLNA (W=730μ m)

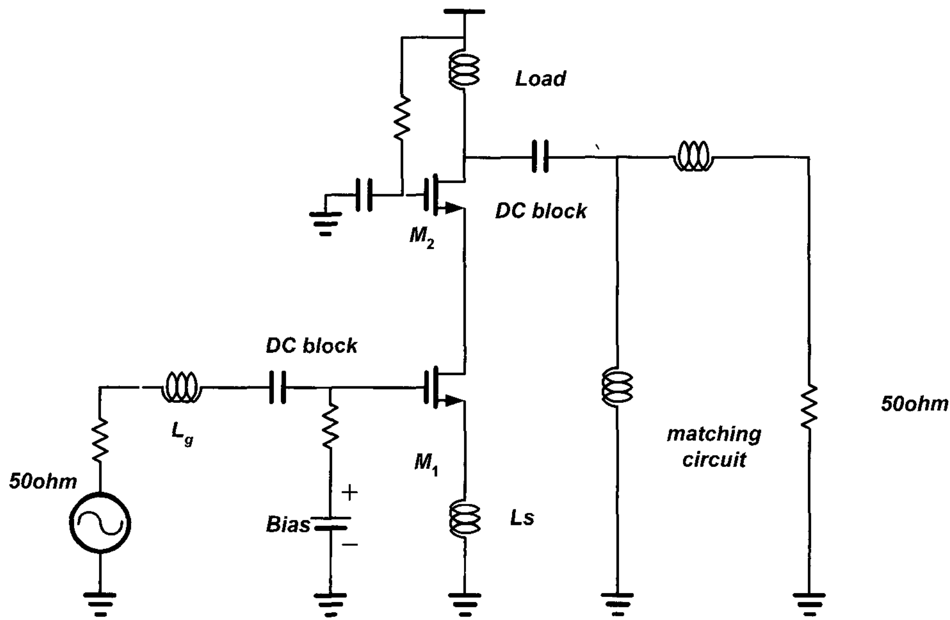

Fig. 5. Complete SDLNA circuit schematic.

$$NF \approx 1 + 2g_{FET}R_0 + \frac{R_0}{R_s} \cdot \frac{1}{W} + g_{FET}R_sW \tag{13}$$

Note that eq. (13) has a term proportional to W and another to $1/W$, therefore it has a minimum value. This is clearly shown in Fig.2, where NF vs. W for 0.18μ m NMOS CSLNA is shown. As expected, higher Q_L, allows us to use smaller transistor width, leading to lower NF. It is easy to show that eq.(13) has minimum value at W_{opt} given by,

$$W_{opt} = \left(\frac{1}{g_{FET}R_s} \times \frac{R_0}{R_s} \right)^{1/2} \tag{14}$$

The corresponding NF_{min} is then given as

$$NF_{\min} = 1 + 2g_{FET}R_0 + \frac{2R_0}{R_s W_{opt}} \quad (15)$$

Equations (14) and (15) are very simple and analytical enough to provide physical insight not only into all types of CMOS LNA circuit designs but also into the characterization and diagnosis of the experimental measured data from fabricated circuits. From 0.18μm CMOS process where the state-of-the-art inductor Q_L of 8 is available, for example, we obtain NF_{min}= 1.28=1.07dB with optimum transistor size of 730μ m at 15mA power consumption.

III. Analytical Design Approach of Input Power Matched SDLNA

In Sec. II, we carried out NF optimization procedure for CSLNA. However, CSLNA can not provide noise figure matching and gain matching simultaneously as was discussed in Introduction. This is also seen in Fig. 4, which shows ADS simulated s-parameter plots for the CSLNA whose optimum width is found analytically as in Sec. II. Fig. 5 shows SDLNA circuit schematic for ADS simulation. Cascode configuration is adopted here for all types of LNA including CSLNA and SDLNA studied in this paper, not only for higher gain but also isolation between input and output. Although cascode transistor (M_2) can increase total NF, it is neglected in our calculation because it has minor effect [5]. In this simulation infinitely high quality choke inductor is assumed and input and output matching inductor quality factor are assumed to be 8. The BSIM3 version 3.2 NMOSFET model was used in this simulation with BSIM3 version 3.2 thermal noise and 1/f noise models. As can be seen in Fig. 4, noise optimum point (S_{opt}) is at 50 Ω, but gain optimum (S11) point is far away from it. It shows that, even though the reactance of the input capacitance is canceled by that of the input matching inductor, additional resistive input impedance is needed for maximum signal power transfer to the LNA input from 50 Ω source.

As introduced earlier, SDLNA is one of the most popularly used methods for this. Fig. 3 shows simplified equivalent circuit for SDLNA, where it is well known that SDLNA provides additional resistive input impedance $\omega_T L_2$ in addition to R_I[6]. Here ω_T is the angular cutoff frequency given by $2\pi f_T$.

Even though the resistive impedance of $\omega_T L_2$ is noiseless, it reduces gain, therefore eq. (1) should be changed as follows, assuming input impedance matching, i.e., $X_I=X_g$ and $R_s=R_I+ \omega_T L_2$.

$$S_{SDLNA} = P_s \times \frac{g_m^2 X_g^2}{4R_s} \quad (16)$$

The noise power, N_{SDLNA}, can similarly be derived as,

$$N_{SDLNA} = 4kT(R_s + R_1) \times \frac{g_m^2 X_g^2}{4R_s^2} + 4kT\gamma g_{d0} \frac{(R_s + R_1)^2}{4R_s^2} \quad (17)$$

Therefore NF of SDLNA is given by,

$$NF_{SDLNA} \approx 1 + 2g_{FET}R_0 + \frac{R_0}{R_s} \cdot \frac{1}{W} + g_{FET}R_s W \quad (18)$$

Note that eq. (18) is exactly the same as eq. (13). This is quite reasonable because L_2 is noiseless and R_2 is negligibly small.

Table 1 compares ADS simulation results for CSLNA and SDLNA optimization results using ADS simulator. Note that SDLNA gives identical NF as CSLNA but much better input matching. Here W=730 μm, is chosen as the optimum FET width for both CSLNA and SDLNA. L_2 is chosen at 0.3nH, which provides resistive input impedance of $\omega_T L_2$=43.6 Ω. This together with R_I= 6.3 Ω leads impedance matching to R_s= 50 Ω.

Fig. 6 clearly shows both NF and input power matching can easily be obtained in SDLNA which was optimized using our design approach developed earlier. $W_{opt,SDLNA}$ is same as W_{opt} of CSLNA and simulation result in

Table 1 shows that both CSLNA and SDLNA have identical NF of 1.05dB. This means that SDLNA is very effective in providing simultaneous power and noise matching with its NF_{min} basically the same as CSLNA.

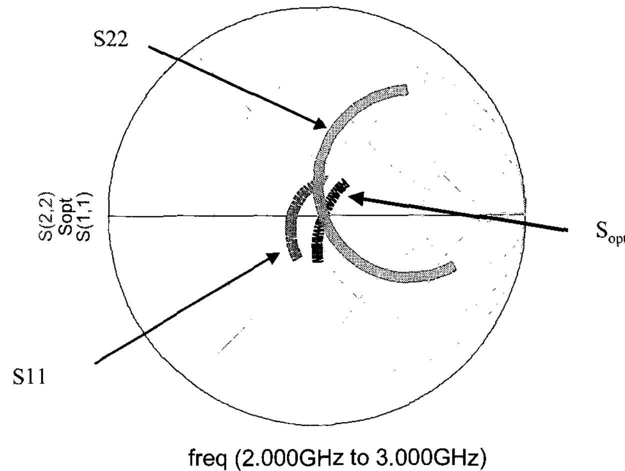

Fig. 6. ADS computer simulated s-parameter plot for NF and input power matched SDLNA (W=730μ m) that was optimized analytically following the approach developed in this section.

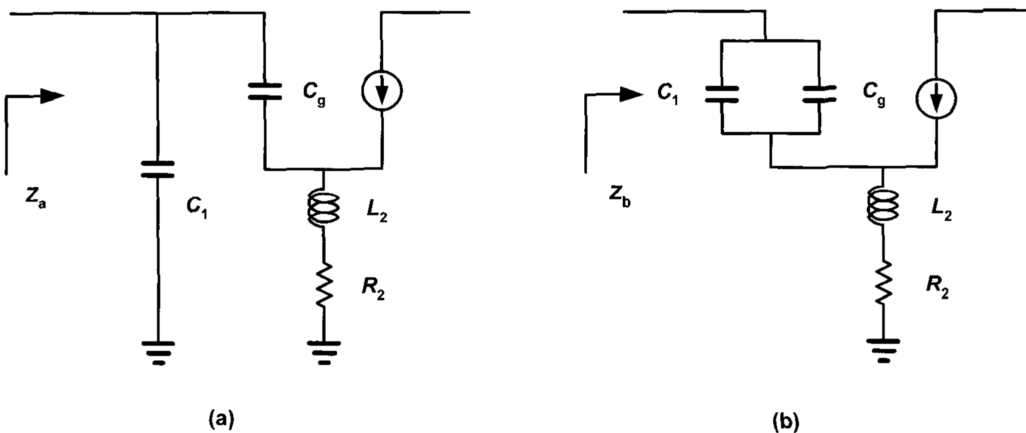

Fig. 7. Two ways to add capacitive admittance to the SDLNA. (a) is conventional L-matching circuit and (b) is proposed recently [4].

IV. MOSFET SIZE SCALING FOR LOW POWER APPLICATION

In Sec. II and III, we assumed that there is no limit in power consumption, i.e., no limit in gate width of CSFET. As a result, we obtained about 15mA current consumption at gate drive voltage of 0.2V with 730μ m gate width as an optimum design example for 0.18μ m CMOS technology. There are, however, many cases where smaller current consumption is absolutely mandatory, where NF should be traded-off for smaller power consumption.

As can be seen previous sections, the impedance of the input matching inductor should always be determined in the range of 50-150 Ω. This is true for any 50 Ω system because about 1-3 times voltage boosting in input matching system is desirable in any LNA. Larger inductor size, although it gives bigger voltage boosting, is not preferable because it inevitably increases NF through bigger R_l. This implies that capacitive reactance of the input circuit should also be in the same range. There are two ways to keep this reactance value at low current consumption. One is to to use the same CSFET found optimally in Sec. II and III but to operate it at lower gate drive. Another is to use smaller with CSFET

Table 1. ADS simulated s-parameters for the circuits shown in Table 1. Here NF_{min} is the minimum NF from the circuits obtainable when inputs are noise matched.

@ 2.4GHz, 1.8V	NF_{min}	NF_{act}	S11	S22	S21	S_{opt}	Current
CSLNA (730µ m)	1.05dB	1.05dB	-3.4dB	-20.4dB	24.5dB	-22.82dB	15mA
SDLNA (730µ m)	1.05dB	1.05dB	-19.1dB	-20.1dB	21.4dB	-19dB	15mA
SDLNA (260µ m)	1.46dB	1.5dB	-19dB	-20dB	20dB	-18dB	5.44mA
SDLNA (160µ m)	1.9dB	2dB	-21dB	-20dB	13dB	-16.5dB	1.54mA

Table 2. Components value and performance for three SDLNA examples designed by analytical methods proposed in this paper. The current is the drain DC bias current at gate drive of V_{GS}-V_T = 0.2V.

α	0	1	1.8
W_{opt}	730 µm	260 µm	160 µm
C_g	1.27pH	0.46pF	0.28pF
C_1	0pF	0.46pF	0.5pF
L_1	3nH	4.66nH	5.4nH
R_1	6.3 Ω	8.8 Ω	10.26 Ω
L_2	0.4nH	1nH	2.15nH
NF_{min}	1.07dB	1.46dB	1.76dB
***Current* at V_{GS}-V_t=0.2V**	15mA	5.5mA	3.3 mA

and add capacitive admittance to the input circuit. The former, although its design is simple and straightforward as discussed in Sec. II and III, is impractical because not only transistor f_T becomes low but it is hard to reproducibly bias MOSFET operating in near threshold regime. Thus it is more practical to scale the transistor width with constant gate drive voltage.

There are two ways to add capacitive admittance to the input circuit of SDLNA as show in Fig. 7.

Fig. 7(a), is one of the most widely used so-called L-match LNA topologies. Fig. 7 (b) is another method proposed very recently [5]. From an elementary circuit analysis, it can be shown that both are quite equivalent. Since, however, circuit analysis of (b) is much simpler than that of (a), we choose (b) for studying low power SDLNA in this paper. Furthermore, (b) is preferable because the value of L_2 leading to 50 Ω input matching is smaller than that of in (a).

The input impedance of Fig. 7 (b) is calculated as,

$$Z_b = \frac{1}{j\omega(C_g + C_1)} + \frac{g_m}{C_g + C_1} L_2 + j\omega L_2 \tag{19}$$

Following the same analysis as in Sec. III, we can conclude the following.

Reactive matching for noise requires,

$$\omega(L_1 + L_2) = \frac{1}{\omega(C_1 + C_g)} \tag{20}$$

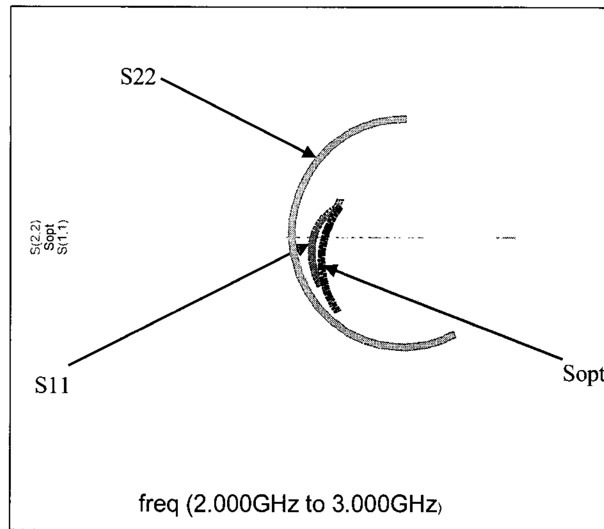

Fig. 8. ADS calculated S11 and S_{opt} plots for the scaled SDLNA (W=260μm) whose components values are designed analytically as in Table 2.

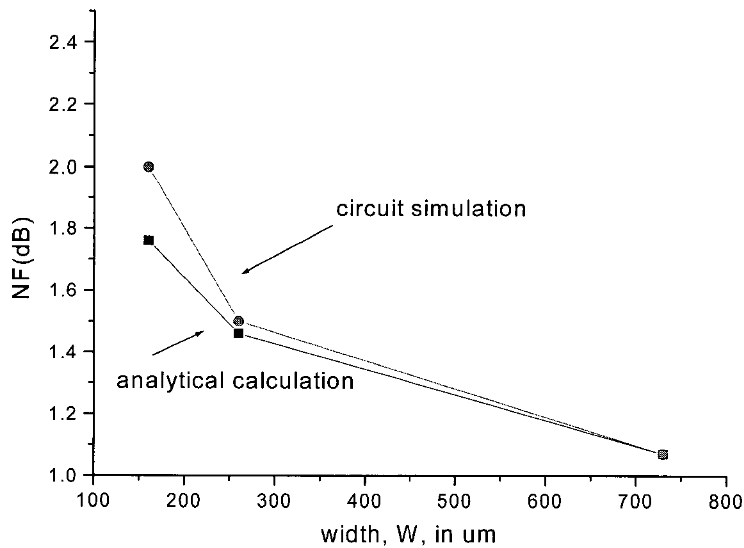

Fig. 9. Analytically calculated NF and ADS simulated NF_{act} comparison for three SDLNA designs which were optimized analytically as in Table 1.

In addition, input power matching requires,

$$R_s = \omega_T' L_2 + R_1 + R_2 = \omega_T' L_2 + \frac{\omega L_1 + \omega L_2}{Q_L} \quad (21)$$

$$\omega_T' = \frac{g_m}{C_1 + C_g} \quad (22)$$

Here ω_T' is defined as the effective cutoff frequency of CSFET where C_l is added to C_g. Note that the C_l effectively reduces cutoff frequency of CSFET. The corresponding NF can then be expressed as

$$NF = 1 + \frac{1}{R_s} \cdot \frac{1}{Q_L \omega (C_1 + C_g)} + \gamma g_{d0} R_s \cdot \frac{\omega^2 (C_1 + C_g)^2}{g_m^2} \cdot \left(1 + \frac{1}{R_s Q_L \omega (C_1 + C_g)}\right)^2 \quad (23)$$

Now if we let,

$$C_1=\alpha\, C_g, \tag{24}$$

and using eq. (9), eq. (23) reduces to,

$$NF = 1 + \frac{1}{R_s Q_L (1+\alpha)\omega C_{g0} W} + R_s g_{FET} W (1+\alpha)^2 \left(1 + \frac{1}{R_s Q_L} \cdot \frac{1}{(1+\alpha)\omega C_{g0} W}\right)^2 \tag{25}$$

Comparing eq. (25) with eq. (17), we see that adding C_1 effectively increases Q_L by a factor of (1+α) and does g_{FET} by $(1+\alpha)^2$. Last term in second parenthesis can be neglected and applying elementary mathematical principle, The optimum transistor width is then obtained by

$$W_{opt} = \frac{W_{opt0}}{(1+\alpha)^{3/2}} \tag{26}$$

Here W_{opt0} is the optimum transistor width at α =0 which was found in Sec. II and III (see eq. (14)). The corresponding NF_{min} is given by

$$NF_{\min} = 1 + \frac{2(1+\alpha)^{1/2}}{R_s Q_L \omega C_{g0} W_{opt0}} + \frac{2 g_{FET}(1+\alpha)}{Q_L \omega C_{g0}} \tag{27}$$

Note that equations (24), (26) and (27) are parametric ones in α .

Table 2 shows three transistor size scaling examples for 0.18μm CMOS technology. First column contains components values and performance of unscaled SDLNA(α =0), second and third columns show two examples (α =1 and α =1.8) of scaled down SDLNA for lower power consumption. Note that L_1 is calculated from eq. (6) and L_2 is calculated from following equation,

$$L_s = \frac{\dfrac{50-R_g}{2\pi f_T}}{(\alpha+1)^2} \tag{28}$$

Fig. 8 shows S11 and S_{opt} plots for scaled SDLNA with W=260 μm using analytically designed components values as listed in Table 2. It demonstrates that both input power and noise are well matched to 50 Ω at 2.4GHz.

Table 1 summarizes simulation results for the three SDLNA shown in Table 2. NF_{min} means lowest obtainable noise figure obtained by ADS simulator at the given bias, transistor size and matching components, NF_{act} stands for actual noise figure calculated by ADS for the circuits listed in Table 2, which were optimized analytically following proposed approaches. Table 1 shows that our transistor scaling theory performs well and demonstrates the accuracy of our approaches. Fig. 9 compares analytically calculated and ADS simulated NF_{act} results, which also shows good agreement. The above results demonstrate the accuracy and usefulness of our analytic design approaches, which provide enough insight not only for the initial design targeting which then can be optimized further by CAD tools but for characterizing and diagnosing fabricated prototypes as well as circuits being manufactured.

V. CONCLUSION

We introduced several simple and analytical design approaches for input power matched CMOS RF LNA circuits and their transistor width scaling for lower power consumption. In spite of the simplicity of our expressions, they give excellent agreement with numerical simulation results using commercial CAD tools for several circuit examples performed at 2.4GHz using 0.18μm CMOS technology. These simple and analytical results are extremely useful in that they can provide enough insights not only for first design targeting which they can be optimized further using CAD tools, but also for characterizing and diagnosing them being prototyped as well as manufactured.

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REFERENCES

[1] B.Razabi, *RF microelectronics*, Prentice Hall, 1998.
[2] F. Svelto, S. Deantoni, G. Montagna and R. castello, "Implementation of a CMOS LNA plus Mixer for GPS Applications with No External Components", IEEE Transaction on VLSI systems, vol.9, No. 1, Feb, 2001.
[3] Beom-Kyu Ko, "Circuit Design Techniques of Monolithic Microwave Low Noise Amplifiers", Ph.D thesis, Korea Advanced Institute of Science and Technology, 1997
[4] Derek K. Shaeffer and Thomas Lee, "A 1.5V 1.5-GHz CMOS low noise amplifier," IEEE J. Solid-State Circuits, vol. 32, pp. 745-759, Mar. 1997.
[5] Pietro Andreani and Henrik Sjoland, "Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier," IEEE Transaction on Circuit and Systems, vol. 48, No.0, Sep. 2001.
[6] E. Abou-Allam, J. J. Nibset, M. C. Malierpaard, "Low-Voltage 1.9-GHz Front-End Receiver in 0.5 um CMOS Technology," IEEE J. Solid-State Circuits, vol. 36, pp. 1434-1452, Oct. 2001.
[7] Beom-Kyu Ko and Kwyro Lee, "A New Simultaneous Noise and Input Power Matching Technique fro Monolithic LNA's using Cascode Feedback," " IEEE Transaction on Microwave Theory and Techniques, vol. 45, No. 9 Sep. 1997.
[8] T. Manku, "Microwave CMOS – Device Physics and Design," IEEE J. Solid-State Circuits, vol. 34, pp. 277-285, Mar. 1999.
[9] A. Van der Ziel, Noise in Solid State Devices and Circuits. New York: Wiley, 1986.
[10] A. A. Abidi, "High-Frequency Noise Measurement on FETs with Small Dimensions," IEEE Trans. Electron Devices, vol. 33, Nov. 1986
[11] B. Razabi. et al., "Impact of Distributed Gate Resistance on the Performance of MOS Devices," IEEE Trans. Circuits and Systems I., vol. 41, pp. 750-754, Nov., 1994.
[12] G. Hayashi, et al., "A 9mW 900MHz CMOS LNA with Mesh Arrayed MOSFETs", IEEE Symposium on VLSI Circuits Digest of Technical Papers., pp 84-85, 1998.
[13] F. Gatta, et al., "A 2-dB Noise Figure 900-MHz Differential CMOS LNA", IEEE J. Solid-State Circuits, vol. 36. No. 10, pp. 1444-1452.
[14] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's", IEEE Trans. Electron Devices, vol. ED-26 pp. 1032-1037, 1979.

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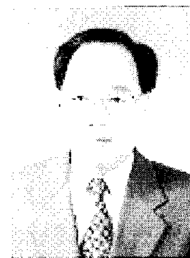

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