SiGe HBT 공정을 이용한 2 GHz Down Conversion MMIC Mixer 개발

2 GHz Down Conversion MMIC Mixer using SiGe HBT Foundry

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요 약

본 논문에서는 ㈜타키오닉스의 SiGe HBT 공정을 이용하여 double balanced Gilbert cell down conversion MMIC mixer를 구현한 결과를 제시하고, 이를 통해 RFIC 설계용 SiGe HBT 파운드리의 정확성과 신뢰성을 평가하였다. 제작된 Mixer는 3 V 동작 전압에서 10 mA의 전류를 소모하며, 2 GHz의 주파수 대역에서 17 dB의 Conversion Gain과 9.8 dB NF, −4.2 dBm Output 1 dB Compression Point, −27 dBc의 RF-IF Isolation의 특성을 나타내었으며 우수한 50 Ω 입. 출력 정합 특성을 갖는다. 시뮬레이션 결과와 측정결과는 거의 유사한 특성을 가지며, 이를 통해 SiGe HBT 모델 라이브러리의 정확성과 공정의 재현성을 검증할 수 있었다.

Abstract

In this paper, a double balanced gilbert cell MMIC mixer was realized in Tachyonics SiGe HBT technology. The fabricated mixer has 17 dB conversion gain, 9.8 dB noise figure, −4.2 dBm output 1 dB compression point, −27 dBc RF to IF isolation, and the good input, output matching characteristics. It draws 10 mA from a 3 V supply. The simulation and the measured results are closer to each other, which confirms accuracy of the model library and reliability of the process.

Key words : SiGe, Double, Balanced, Gilbert-Cell, MMIC, Mixer

Ⅰ. Introduction

The advance in satellite and IT technology has popularized the wireless communication system, and with the variety of user groups and large communication traffic, the frequency applied is getting higher. This paper presents the design and test results of down conversion MMIC mixer developed using Tachyonics SiGe HBT process, used on 2 GHz frequency for the receiver stage on a pcs and cellular phone. This process is highly cost efficient.

Ⅱ. Design and Layout of Active Down Conversion Mixer

The internal block diagram for the mixer is as shown in Fig. 1. The output IF frequency 250 MHz is obtained as the difference between input RF signal

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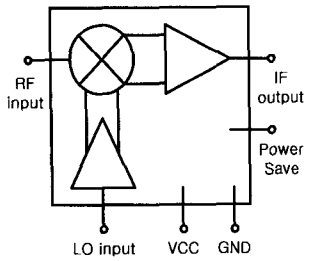

그림 1. 내부 블록 다이아그램
Fig. 1. Internal block diagram.

frequency 2.0 GHz and LO frequency 1.75 GHz.

The voltage supplied to the circuit is dc 3.0 V and the basic size of the applied transistor is the same as the Tachyonics SiGe HBT library 1×8 npn transistor. The schematic in Fig. 2 shows the active double balanced gilbert mixer used in this paper. Q1, Q2 are the differential amplifier driver stage, which amplifies the RF signal, and reduces the noise from Q3, Q4, Q5, Q6 switching quad. If the conversion gain of the mixer is too high, the input IP3 can be saturated, so we used a emitter degeneration resistor between the emitter coupled pair Q1 and Q2 to enhance the linearity and lower the conversion gain.

The local amplifier in Fig. 3 is similar to a differential amplifier. When the input local power grows higher in the gilbert-cell mixer, transistor Q1, Q2, Q3, Q4, Q5, Q6 in figure 2 saturates and the

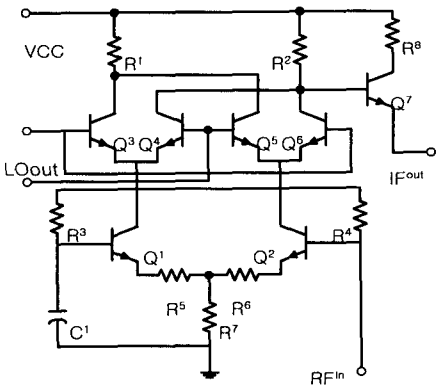

그림 2. 더블 밸런스 길버트 주파수 변환기
Fig. 2. Double Balanced Gilbert Mixer.

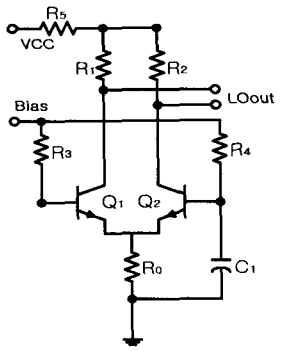

그림 3. 로컬 증폭기
Fig. 3. Local amplifier.

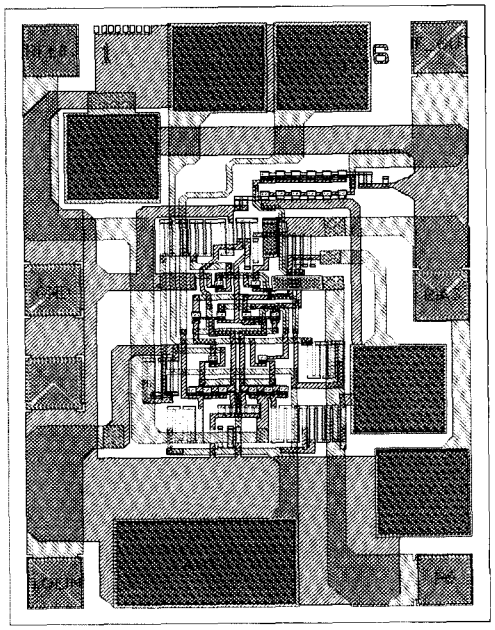

그림 4. 주파수 변환기 IC 내부 회로
Fig. 4. Mixer layout.

linearity of the mixer falls. So considering the mixer gain and linearity, a local amplifier was used to keep the input level of the local power under −10 dBm.

Fig. 4 is the layout of the designed mixer. The metal line was miter bended to minimize the discontinuity. To minimize the effects of bonding wire, we maximized the ground availability and used several bonding wires. The size of the chip is 1.28×0.81[mm^2]. The transistor and resistors were

placed considering the symmetry of the circuit. Also, to ground the vcc reliably, a RF short capacitor was used inside the chip. The placement and routing was done, with the same conditions of the basic transistor for the parallel connection of the transistors. The resistor variance was minimized by the layout of resistors, where the resistor pattern length is 5 squares longer compared to the area. A dummy resistor was added to the resistor that determines the bias, so that the resistor value could be changed in the future by changing the metal mask.

Ⅲ. Simulation and Measurement Results

Fig. 5 is an evaluation board for the designed chip using FR4 substrate of εr=4.8 and 0.8 mm thickness. The mixer chip was tested in the form of COB(Chip On Board) type. The PCB size was 30x30[mm^2] and the wire bonding was made using a gold wire of 1mil diameter.

The designed 2.0 GHz mixer was evaluated using a network analyzer(HP8510C), spectrum analyzer (HP8563E, E4407B, E4405B), noise figure meter (HP8970B), signal generator(HP83623B, HP8664A, ESG-D3000A). The conversion gain of the 2.0 GHz mixer is shown in the "One Tone test result" in Fig. 7. The gain is slightly higher than 17.0 dB for the input power of −40 dBm, and the simulation results shows about 18.4 dB. The measured conver sion gain of the mixer is about 1.4 dB lower compared to the simulation. However, considering the loss of PCB, the effects of the boding inductance, and the loss of the measurement equipments, the difference is not too much. As the RF input power increases from −50 to −10 dBm, the conversion gain is nearly constant upto −25 dm.

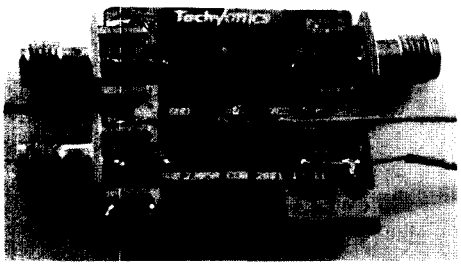

그림 5. 측정용 시제품
Fig. 5. Test JIG.

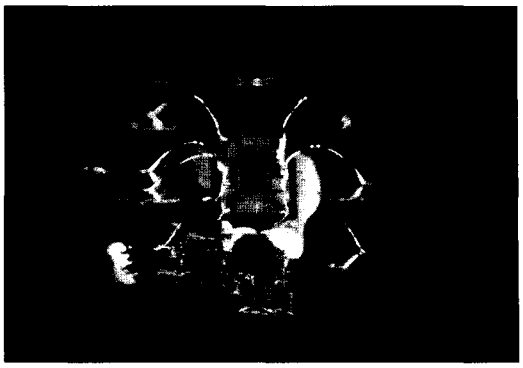

그림 6. COB PCB 확대
Fig. 6. Zoom in COB PCB.

The measurement of the noise figure of the mixer was done using HP8970B noise figure meter. The measured result was 9.8 dB which is slightly better than 10 dB estimated by the simulation. Fig. 8 shows simulation and measured results of "Two Tone test," where the input RF power is swept from −50 to −10 dBm. Measured IIP3 is −10 dBm and the linearity of the designed mixer seems to be very good. Fig. 9 shows the simulation and measured results of the RF to IF isolation, 22 dBc and 27 dBc

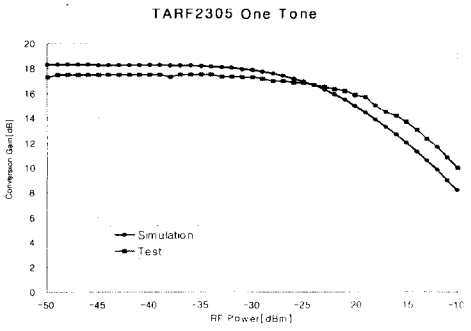

그림 7. 원톤 측정 결과
Fig. 7. One Tone test result.

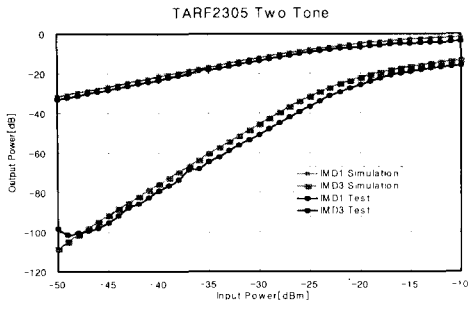

그림 8. 투톤 측정 결과
Fig. 8. Two Tone test result.

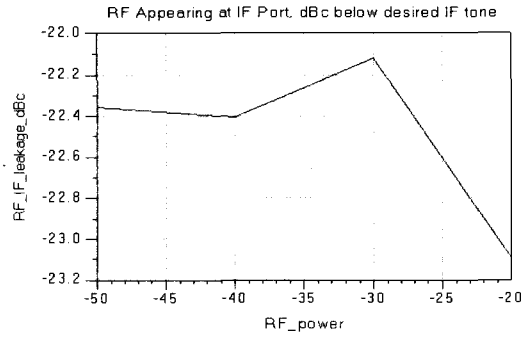

그림 9. RF-IF신호 아이솔레이션 시뮬레이션
Fig. 9. RF-IF isolation simulation.

표 1. 시뮬레이션값 vs 측정값 비교표
Table 1. Simulation vs Test results.

Parameter		Sim	Target	Test	Unit	Condition
Overall	RF Freq.	2.0	2.0	2.0	GHz	RF=−40 dBm
	IF Freq.	250	250	250	MHz	
	LO Freq.	1.75	1.75	1.75	GHz	
Mixer	CG	18.4	17.0	17.0	dB	IF=250 MHz
	Output P1 dB	−3.2	−5.0	−4.2	dBm	
	Input IP3	−13.0	−11.0	−11.0	dBm	
	NF	10.0	13.0	9.8	dB	SSB
	LO Level	−10.0	−10.0	−10.0	dBm	
	RF to IF	−22	−25	−27	dBc	
Power	Voltage	3.0	3.0	3.0	V	
	Current	11.2	12.0	10.1	mA	

respectively. Table 1 summaries the main features of the designed mixer comparing the simulation and the measurement results with the initial design targets. In most cases, the test results were a little short of the simulation results, but were better than the target specification in most categories.

Ⅳ. Conclusion

The 2 GHz active double balanced down conversion MMIC mixer designed in this paper is an essential part used in the receiving stage of a wireless communication system. The fabricated chip using SiGe HBT process with a 40 GHz f_T shows the performance of 17 dB conversion gain, −4.2 dBm output P1 dB, −11 dBm IIP3, 9.8 dB noise figure, 27 dBc RF to IF Isolation. The current consumption is 10 mA with 3 V supply. The chip size is 1.28×0.81[mm^2], but has the possibility of shrinkage. The designed down conversion mixer is made from a double metal process and has excellent frequency characteristics and linearity. Through the design, fabrication and evaluation procedures, we were able to verify the accuracy and excellency of Tachyonics SiGe RF Library. We can also expect to find a definite solution for RF MMIC Foundry Service.

References

[1] Behzard Razavi, *Rf Microelectronics*, Prentice Hall PTR, pp. 182-200, 1998.

[2] Barrie Gilbert, Rupert Baines, "Fundamentals of Active Mixer", *Applied Microwave & Wireless*, Winter 1995, pp. 10-27, 1995.

[3] David M. Pozar, *Microwave Engineering*, 2nd Edition, pp. 574-576, 1998.

[4] Guillermo Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, 2nd Edition, Prentice Hall PRT, pp. 362-364, 1997.

[5] Keng Leong Fong, Robert G Meyer, "Analog

And Signal Processing", *IEEE Transaction On Circuits And System-II*, vol. 46, no. 3, pp. 231-239, March 1999.

[6] Alan B Greben, *Bipolar And Mos Analog Integrated Circuit Design*, John Wiley & Sons.

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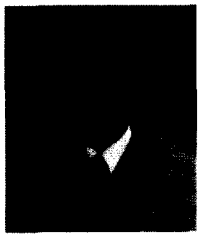

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