韓國電磁波學會論文誌 第13卷 第6號 2002年 7月 論文 2002-13-6-06

Applications of Triple Controlled Type DDFS-driven PLL Frequency Synthesizer to Broadband Wireless Systems

3중조절 DDFS 구동 PLL 주파수 합성기의 광대역 무선 통신시스템에 응용

Heung-Gyoon Ryu · Byeong-Rok An

유 흥 균 · 안 병 록

Abstract

In this paper, a triple controlled type DDFS-driven PLL frequency synthesizer with reduced complexity is used to show its applications for broadband wireless communication systems by frequency synthesis control. Since the proposed DDFS-driven PLL synthesizer is very simplified to use only phase accumulator in DDFS, it improves the switching speed and power consumption than the conventional DDFS-driven PLL frequency synthesizer. It is appropriate for applications with requirements of broadband, low-power consumption and high switching speed, since the proposed synthesizer can cover a wide range of frequency bands by the triple frequency control parameters. Method and results of frequency control parameters assignment are shown for the several frequency bands applications such as GSM, IMT-2000, Bluetooth and PCS system.

요 약

본 논문에서는, 구조를 간략히 한 3중 조절형의 DDFS 구동PLL 주파수 합성기를 이용하여 주파수 합성 조절법에 의한 광대역 무선통신시스템으로의 응용을 연구하였다. 제안된 DDFS 구동PLL 주파수 합성기는 DDFS에서 위상누적기만을 이용하는 매우 단순화된 구조이므로, 기존 DDFS 구동PLL 주파수 합성기의 경우보다 스위칭 속도가 높으며, 전력소모를 개선시킨다. 그리고 이 제안된 3중 조절형 주파수 합성기는 3가지 주파수 조절 파라미터를 이용하여 넓은 대역의 주파수 범위의 동작이 가능하므로, 광대역 저전력 고속 특성을 갖는 응용에 적합하다. 주파수 조절 파라미터 할당 방법과 그의 결과를 제시하였으며, GSM, IMT-2000, Bluetooth 및 PCS 시스템, 등여러 주파수 대역에 응용하는 경우를 보였다.

Key words : Triple Frequency Control, Triple Controlled Type, DDFS, PLL, DDFS-Driven PLL, Frequency Synthesizer

Ⅰ. Introduction

Even though DDFS(direct digital frequency synthesizer) has a performance of exquisite step size, fast switching time and good spurious performance [1], it has a disadvantage that needs the waveform shaping in a DDFS-driven PLL(phase locked loop) frequency synthesizer. In such a system, DDFS must provide PLL with accurate reference digital clock. However, since conventional DDFS output is a kind

충북대학교 전자공학과 및 컴퓨터정보통신연구소(Dept. of Electronic Engineering, and Research Institute of Computer, Information & Communication, Chungbuk National University)

· 논 문 번 호 : 20020219-021

· 수정완료일자 : 2002년 5월 2일

of sinusoidal analog signal, the digitizing process is necessary and its non-ideal effects are occurred in DDFS-driven PLL frequency synthesizer.

In the literatures, there have been many researches on frequency synthesis with high quality factors such as fast switching speed, low power consumption, low phase-noise, low spurious level, and so on [2]~[7]. In [2], authors presented the reduced complexity design method of DDFS for reducing the switching time and power consumption in DDFS-driven PLL frequency synthesizer. As compared with conventional DDFS-driven PLL synthesizer using the general DDFS structure, it has many advantages. Fast switching speed is obtained by removing other circuits except the phase accumulator(PA) in DDFS. It is quite true because the period of MSB(most significant bit) of PA output is equal to that of wanted DDFS output. Furthermore, since an output of PA is a digital clock signal, it is not necessary to digitize the DDFS output, contrary to the conventional scheme using a waveform shaper such as a hard limiter or Schmitt trigger. Therefore, the favorable performances can be obtained with lower power consumption. In [3], authors have also shown that the proposed scheme in [2] is applicable to triple controlled type DDFS-driven PLL frequency synthesizer, which was proposed in [4]. Since the triple controlled type PLL frequency synthesizer can work by controlling the triple control parameters within the frequency band supported by VCO (voltage-controlled oscillator), applications of simplified DDFS-driven PLL synthesizer are appropriate for various mobile communications systems.

In this paper, we introduce a triple controlled type DDFS-driven PLL frequency synthesizer with reduced. The assignment steps of triple frequency control parameters are proposed for the applications to various frequency bands. Finally, the assignment results of frequency control are presented for the digital wireless communication systems such as GSM(group special mobile), IMT(international mobile telecommunications)-2000, Bluetooth, and Korean PCS(personal communications service) system.

Ⅱ. Triple Controlled Type DDFS-Driven PLL Synthesizer with Reduced Complexity

In Fig. 1, the simplified triple controlled type DDFS-driven PLL frequency synthesizer is shown. This frequency synthesizer generates the desired frequency with low spurious level by controlling the three control parameters of K, R and [3], [4]. In the conventional DDFS, since the output is an analog signal, the digitizing process is necessary to provide the digital type phase detector with a reference clock.

As shown in Fig. 1, the PA has an input word K of M-bit. Among PA output bits, the first and second MSBs (most significant bits) are usually used to control the phase of 90° and of 180° output signal, respectively. Notice that the first MSB has the same period as the DDFS output signal. In other words,

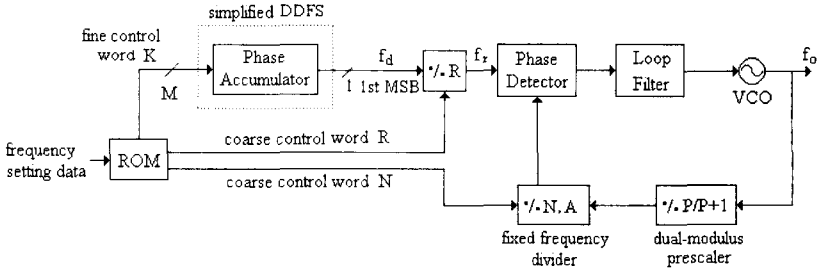

Fig. 1. Triple controlled type synthesizer with reduced complexity.

the first MSB and the DDFS output have the same frequency. Therefore, there is no necessity for doing waveform shaping the DDFS output signal in DDFS-driven PLL synthesizer. In addition, removing the other circuits except PA in DDFS significantly reduces the circuit complexity. That is, it is proven that the first MSB is quite appropriate to provide the digital reference clock for DDFS-driven PLL synthesizer.

There are many advantages from using only the first MSB for the reference clock. First, the waveform shaping process is not necessary. Hence, it is not affected by the waveform shaping. Second, power-consumption is lowered from sine-ROM (read-only memory) of look-up table, DAC(digital-to-analog converter) and waveform shaper. Therefore, power consumption in DDFS can be minimized without additional efforts. Finally, switching speed, which is one of the important quality factors in frequency synthesizer, can be considerably improved from the delay time reduction in the above circuits.

Ⅲ. Assignment Steps of Triple Control Parameter

In a DDFS, the input of the accumulator is the frequency control word, K, which is a kind of fine control word. Then, the output frequency of DDFS, f_d, is changed by variation of input control word. The relationship between the output frequency and the input word is represented by [1]

$$f_d = \frac{f_{CLK} K}{2^N} \tag{1}$$

where f_{CLK} is the clock frequency. Hence, the input frequency of phase detector is

$$f_r = f_d / R \tag{2}$$

Then, the output frequency of PLL is

$$f_o = f_r (NP + A) \tag{3}$$

where P is the fixed division ratio of dual-modulus prescaler. In Eq. (3), N and A are frequency division ratios of main and swallow counters in a fixed frequency divider, respectively. In this fixed frequency divider, N and A are used to cover the entire frequency range and the single channel spacing, respectively.

The frequency resolution of synthesizer is determined by f_{CLK} and R. This resolution represents the channel spacing of a specific system. Since frequency band and channel spacing are different according to the wireless applications of communications systems, these values should be variable to each system. Also, the other two control parameters of K and N are pre-determined and stored in ROM to cover the desired frequency band.

From the above passage, steps for parameter assignments are summarized as follows:

Step 1. K, f_{CLK} and R are set to determine the frequency resolution or channel spacing.

Step 2. Control parameter, N, is the predetermined and stored value to cover the entire frequency band of each desired application.

Step 3. A is increased by +1 up to 16. After A is increased up to 16, N is increased by +1 and A is set to 1 to represent the next channel.

Ⅳ. Frequency Allocations for Various Mobile Applications

In the previous section, assignment steps for parameter setting are described to satisfy the channel spacing and cover the entire frequency band of specific system. In this section, we will show setting methods of the above parameters for the triple controlled type DDFS-driven PLL frequency synthesizer to operate effectively in various mobile applications. In this paper, it is assumed that maximum values of K, N, R and A are fixed as 15, 511, 127 and 16, respectively.

Table 1. Parameters for PCS.

K	f_d [MHz]	R	f_r[MHz]		N	A	f_0 [GHz]
2	31.25	25	1.25	RL	87	8	1.75
					87	32	1.78
8	125	50		FL	91	15	1.84
					91	39	1.87

Table 2. Parameters for GSM.

K	f_d [MHz]	R	f_r [MHz]		N	A	f_0 [MHz]
1	4	20	0.2	RL	278	2	890
2	8	40			285	15	915
4	16	80		FL	292	3	935
8	32	160			299	3	960

4-1 Korean PCS

- FL (forward link): 1.84~1.87 GHz
- RL (reverse link): 1.75~1.78 GHz
- Channel spacing: Δf=1.25 MHz
- f_{CLK}=1 GHz, P=16

Table 1 shows parameter setting for forward and reverse links of Korean PCS. In this system, the forward and reverse links use 24 channels with channel spacing of 1.25 MHz, respectively. For example, let us consider a reverse link. In this case, R and K are first set to 2 and 25 or 8 and 50, respectively, so that $f_r = \Delta f$. Next, division ratios of the fixed frequency divider, N and A, are appropriately set to 87 to obtain the first channel of the desired frequency band, e.g. 1.75 GHz. After K, R, and N are determined according to step 1 and step 2, all channels with Δf=1.25 MHz between 1.75 and 1.78 GHz can be obtained by increasing A by +1 according to step 3. These procedures can also be applied in a forward link.

4-2 GSM

- FL (forward link): 935~960 MHz
- RL (reverse link): 890~915 MHz
- Channel spacing: $=\Delta f$=0.2 MHz
- f_{CLK} = 0.256 GHz, P=16

Parameter setting for forward and reverse links of GSM is shown in Table 2. In this system, both forward and reverse links use 125 channels of Δf= 0.2 MHz. All procedure is similar to the case of PCS. In this system, a different clock frequency is used for adjusting f_r=0.2 MHz., Since the channel spacing is smaller than Korean PCS, it needs very large frequency division ratios, as compared with Korean PCS system.

4-3 IMT-2000

- FL (forward link): 2.110~2.200 GHz
- RL (reverse link): 1.885~2.025 GHz
- Channel spacing: Δf=5 MHz
- f_{CLK}=1 GHz, P=16

Table 3 shows parameter setting for both direction links of IMT-2000 system. Forward and reverse links have 18 and 28 channels of Δf=5 MHz, respectively. In this case, since the channel spacing and channel bandwidth are very larger than Korean PCS and GSM, smaller division ratios should be used.

4-4 Bluetooth

- channel bandwidth: 2.402~2.480 GHz
- Channel spacing: Δf=1 MHz
- f_{CLK}=256 MHz, P=16

Bluetooth uses the ISM(industry, science and

Table 3. Parameters for IMT-2000.

K	f_d [MHz]	R	f_r [MHz]		N	A	f_0 [GHz]
8	125	25	5	RL	23	9	1.885
					25	5	2.025
				FL	26	6	2.110
					29	8	2.200

Table 4. Parameters for Bluetooth.

K	f_d [MHz]	R	fr [MHz]	N	A	f_0 [GHz]
1	4	4	1	150	2	2.402
2	8	8				
4	16	16		154	16	2.480
8	32	32				

medical) band between 2.402 and 2.480 GHz. Table 4 shows parameter setting for Bluetooth system. Similar to the case of GSM system, we can generate all required frequency in Bluetooth system by selecting various values of K, R and N. However, since both channel spacing and channel bandwidth of Bluetooth system are larger than those of GSM, it is possible to use smaller division ratios.

V. Simulations and Results

The presented circuit of Fig. 1 is simulated to evaluate its performance. Simulations are performed in HSPICE and MOSFET with gate length of 0.24 μ m is used. In the DDFS, the input word, K, consists of 6-bit. Fig. 2 shows simulation result of the transfer characteristic of the designed VCO. This VCO is a kind of ring oscillators. There is a nonlinearity in the respect of total curve. However, since each different part of the curve is used according to the mobile applications, piecewise linear portion is utilized so that nonlinearity shown in total curve is not a problem within the specific application frequency band. Therefore, this designed VCO for triple controlled type DDFS-driven PLL frequency synthesizer of Fig. 1 can cover the above four mobile frequency bands with high quality factors of low power-consumption and fast switching speed.

Finally, let's see how well the simplified DDFS can operate to drive the PLL in Fig. 1. Fig. 3 shows the transient response of PLL loop filter when K=15, N=8, R=64 and A=1, i.e. f_0=4.724 MHz. As shown Fig. 3, since the simplified DDFS provides the

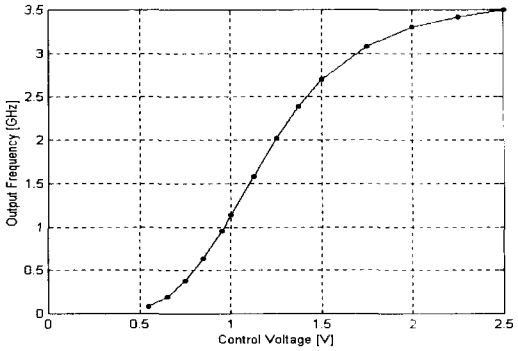

Fig. 2. Transfer characteristic of VCO.

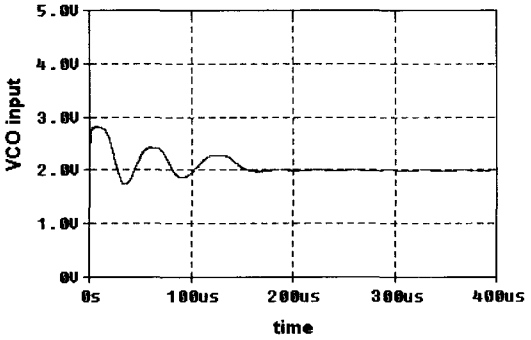

Fig. 3. Settling process of loop filter output.

digital reference clock to the PLL, the PLL is settled down into the stable region within 0.15ms. Hence, the simplified DDFS is very appropriate for the triple controlled type DDFS-driven PLL frequency synthesizer.

VI. Conclusion

In this paper, assignment method of triple frequency control parameters in the simplified DDFS-driven PLL synthesizer is proposed for the various mobile applications such as European GSM, IMT-2000, Bluetooth and Korean PCS system.

Frequency allocation method is the three steps in section 3 and these steps are applicable to all systems. The assignment results of frequency control parameters are presented for the digital mobile communication systems as Table 1 ~ 4. When the

channel spacing and bandwidth become smaller, it is good for division ratios to increase and more parameters should be changed. By using this proposed method, it is shown that triple controlled type simplified DDFS-driven PLL frequency synthesizer can be applied to cover the broad frequency. In addition, it provides high quality factors, such as fast switching speed and low power-consumption.

Consequently, it is possible not only to cover four kinds of wireless communication frequency band between 800 MHz and 2.5 GHz by using the proposed triple controlled type DDFS-driven PLL synthesizer with one VCO but also to have high quality factors.

References

[1] B-G. Goldberg, *Digital Techniques in Frequency Synthesis*, McGraw-Hill, 1996.

[2] H. G. Ryu, Y. Y. Kim, H. M. Yu and S. B. Ryu, "Design of DDFS-driven PLL Frequency Synthe sizer with Reduced Complexity", *IEEE Transactions on Consumer Electronics*, vol. 47, no. 1, Feb. 2001.

[3] H. G. Ryu, Y. Y. Kim and H. M. Yu, "Reduced Complexity Design for Triple-Tunable Frequency Synthesizer", *IEE Electronics Letters*, to be published.

[4] K. Tajima, Y. Imai, Y. Kanagawa, and K. Itoh, "A 5 to 10 GHz Low Spurious Triple Tuned Type PLL Synthesizer Driven by Frequency Converted DDS Unit", *IEEE MTTS International*, vol. 3, pp. 1217-1220, 1997.

[5] T. Saba, D. K. Park and S. Mori, "Fast Acquisition PLL Frequency Synthesizer with Improved N-Stage Cycle Swallower", *IEEE ISSSTA* '94, vol. 2, pp. 352-356, 1994.

[6] Y. Sumi, S. Obote, N. Kitai, H. Ishii and R. Furuhashi, "PLL Synthesizer with Multi-Programmable Divider and Multi-Phase Detector", *IEEE Transactions on Consumer Electronics*, vol. 45, no. 3, pp. 950-955, August 1999.

[7] D. Wulich, " Fast Frequency Synthesis by PLL Using a Continuous Phase Divider", *Proceedings of the IEEE*, vol. 76, no. 1, pp. 85-86, January 1988.

유 흥 균

1988년~현재: 충북대학교 전자공학과 정교수

[주 관심분야] 디지털 통신 공학, 이동 통신 시스템, 통신 회로 설계 및 통신 신호 처리

안 병 록

1987년 2월: 부경대학교 전기공학과 (공학사)

1993년 8월: 충북대학교 전자공학과 (공학석사)

1998년~2001년: 충북대학교 전자공학과 박사수료

현재: 주식회사 우신전기기술사 사무소 대표