Design of a Series Voltage Sag Compensation System in Transmission Line

Hyen Young Choi*, Yang Mo Kim*, Gyo Sung Lee*, Se Ho Oh* and Jung Gyun Park*

Abstract - When power consumption increases, power supply must be efficient and reliable for good power quality. The studies on compensation system of power quality are processing actively. Voltage sag among of factors for power quality is generally PI dual control that voltage sag compensation is used. But this control is no more available since of 120[kHz] ripple rejection. So we proposed the control algorithm using PID control in 3-phase unbalanced power system and the series voltage compensator, when voltage sag occurs.

Keywords: voltage sag, PI control, PID control, voltage sag compensation, PQ (power quality)

1. Introduction

With the progress of industry, widespread digital computers and electronic equipment become all the more sensitive to transients, voltage sags, harmonics, momentary interruptions, and so forth. If these matters computers and electronic equipment will malfunction and these power quality (PQ) events lead to increased costs for industry. When an industrial process is interrupted or shut down as a result of a PQ event, the process outage will be much longer than the duration of the PQ events itself. Especially, voltage sags are the most important problem of the PQ events. NPL(National Power Laboratory) of the U.S.A. presented a measured report at 235 areas of the U.S.A. and Canada from 1990 to 1995. According to that report, voltage sags constitute 87[%] of PQ events. Other events are typically rare, accounting for an additional 13[%] of all PQ events. But we have no advanced theory about the effect of voltage sags [1].

In the distribution line, some lines are connected to the bus in parallel. So a single line fault causes the voltage to drop to almost zero at the fault position. This zero voltage then turns into an event of a certain magnitude and duration at the interface between the adjacent line and the bus. That magnitude is smaller than normal voltage but is greater than zero. According to the NPL survey, voltage drops of 60[%] nominal voltage are most often the case with voltage sags. Voltage sags are typically caused by fault conditions. Voltage sags may also be caused by motor stating. These are usually three-phase symmetrical sags of shallower depth and longer duration, which affect only the local area. Statistical data have shown that most faults are single-line-to-ground (SLG) faults.

A few years ago, these voltage sags had little effect on the system. But in cases of industrial processes using computer systems, sensitive communication systems, medical equipment and accurate electrical equipment, short-duration voltage sags can lead to the fatal results. So voltage sags have been called the most important concern affecting most industrial and commercial customers, and several studies been conducted and developments have been made.

With the progress of power electronics, voltage sag compensation systems using power conversion equipment have been actively studied. Voltage uninterruptible power supply (UPS) systems are representative. UPS systems compensate not only for voltage sags, but also for voltage swells and harmonics, so the performance is excellent. But UPS systems require extensive maintenance and repair and are not economical in power distribution systems. Recent studies have focused on a dynamic voltage restorer (DVR) that injects voltage to compensate for voltage sags in series with a distribution feeder. Because the object of the DVR is just voltage sag compensation, the DVR has an economic advantage over the UPS system and has excellent dynamic characteristics [2][3]. Control efficiency of the DVR is determined by.

1. compensation magnitude limit,
2. reduction of steady-state errors,
3. source voltage with phase synchronous.

Previous studies of voltage compensation proposed an algorithm to control DC values using the d-q synchronous rotating frame of 3-phase voltage source. This method allows easy control of the system because d-q

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transformation allows to reduce a three-phase system to an equivalent two-phase system plus the zero-sequence component. But symmetrical parts of the 3-phase unbalanced voltage source during voltage sags are detected by vector calculation or the filter. So the control structure is complex [4].

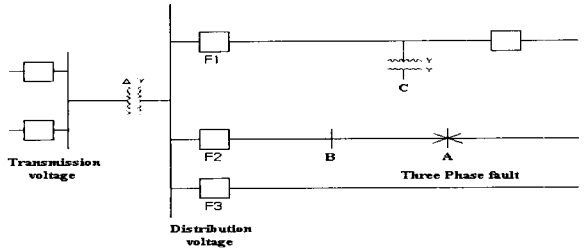
This paper combined the basic theory and control algorithm with simulation and results for compensation voltage sag. It compared the compensation between PID control and PI double control. Considering dynamic characteristics as important points in the system, we proposed a compensation using PID control.

2. Voltage Sags

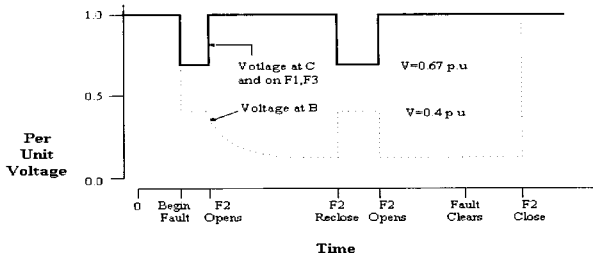
The sudden reduction of the voltage is a short duration reduction in rms voltage caused by faults on the transmission or distribution system. There is a difference between the the IEEE and IEC standards description of the voltage sags. The IEC standard describes voltage dip as a sudden reduction of the voltage at a point in the electrical system, followed by a voltage recovery after a short period of time, from 0.5 cycle to a few seconds. The amplitude of a voltage sag is defined as the difference between the voltage during the sag and the nominal voltage of the system and is expressed as a percentage of the nominal voltage. The IEEE standard 1159-1195 describes voltage sag as a decrease of between 0.1 to 0.9[pu] in rms voltage at the power frequency for the duration of 0.5 cycle to 1 minute. Especially voltage sag with a duration time of 8.3[ms] to 0.5[s] is called instantaneous sag. The voltage sag lasts until the fault is cleared by a protective device therefore, the duration of the sag is determined by the fault-clearing time of the protection system adopted. The magnitude of the voltage sag is mainly determined by the impedance between the faulted bus and the load.

In transmission or distribution systems, more frequent problems are faults on the transmission system or faults on the bus. In these cases, voltage sags appear before the customers during the fault-duration time.

When the fault occurs on the distribution system, voltage sag appears on the bus by influence of the fault. A distribution voltage is shown in Fig. 1.



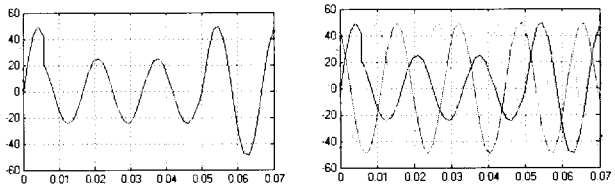
(a) 3-phase fault at distribution system



(b) Effect about others phase by fault

Fig. 1 Distribution voltage caused by fault

If the fault happens on the transmission system, the fault line is separated from the source to prevent energy leakage and the total time for the fault detection and operation of the braker is about 3~6 cycles. The magnitude and duration time of the voltage sag are different according to the fault position.



(a) (b)

Fig. 2 Voltage sag by SLG fault

Fig. 2 shows voltage sag 50[%] of default reduced by SLG fault. Voltage sag versus duration time is shown in Table 1. 50[%] of voltage sags correspond to voltage sags down to 20[%] of the nominal line voltage, 60[%] of voltage sags last for less than 5 ~ 6 cycles, and 80[%] last for less than 0.2[s].

Table 1 Voltage sag duration time

Category	Duration time	Magnitude
Instantaneous	0.5~30 cycles	0.1~0.9 pu
Momentary	30 cycles~3s	0.1~0.9 pu
Temporary	3s~1min	0.1~0.9 pu

In this paper, we proposes a high-quality, accuracy voltage sag compensator having a characteristic of the DVR.

During normal operation, the proposed high-quality accuracy voltage compensator, SAGCOM supplies the load with sources of electricity. When voltage sag is detected, the voltage source inverter injects a voltage in series with the line to compensate for the sag.

The voltage sag compensator is shown in Fig. 3. The voltage generated from the inverter is injected by the transformer in series to compensate for the decrease in supply voltage. SAGCOM must compensate for voltage sag within 0.2[s], compensation for voltage sag of less than 60[%] nominal voltage and voltage injection that is

synchronized with supply voltage are conditions that must be satisfied.

3. Unbalanced Power System

As a matter of fact, most voltage sags are generated by SLG faults. Under fault conditions, the power system turns into a 3-phase unbalanced voltage. Eq. (1) demonstrates the relationship between 3-phase unbalanced voltages and zero, positive, and negative sequence components.

E_{an}, E_{bn}, E_{cn} is respectively phasor voltage of 3-phase voltage, and E_0, E_p, and E_n means zero, positive, and negative sequence components, respectively.

$$\begin{bmatrix} E_{an} \\ E_{bn} \\ E_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}\begin{bmatrix} E_o \\ E_p \\ E_n \end{bmatrix} \quad (1)$$

where $a = e^{j\frac{2\pi}{3}}$ and the unbalanced 3-phase voltage can be represented by Eq. (2).

$$\begin{bmatrix} e_{an}(t) \\ e_{bn}(t) \\ e_{cn}(t) \end{bmatrix} = V_{mp}\begin{bmatrix} \cos(wt+\alpha_p) \\ \cos(wt+\alpha_p-\frac{2}{3}\pi) \\ \cos(wt+\alpha_p+\frac{2}{3}\pi) \end{bmatrix} + V_{mn}\begin{bmatrix} \cos(wt+\alpha_n) \\ \cos(wt+\alpha_n+\frac{2}{3}\pi) \\ \cos(wt+\alpha_n-\frac{2}{3}\pi) \end{bmatrix} + V_{mo}\begin{bmatrix} \cos(wt+\alpha_0) \\ \cos(wt+\alpha_o) \\ \cos(wt+\alpha_o) \end{bmatrix} \quad (2)$$

Using d-q transformation matrix of Eq. (3), Eq. (2) is transformed into Eq. (4), which represents the d-q axis variables on the synchronous rotating frame[5].

e_d^e , e_q^e : d-q axis on the synchronous frame

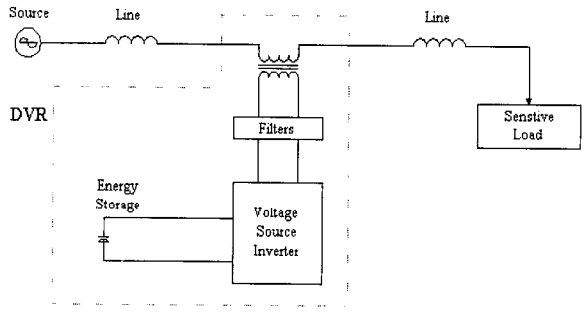


Fig. 3 Voltage sag compensator

$$T = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (3)$$

$$e_d^e = \frac{2}{3}(e_a - \frac{e_b}{2} - \frac{e_c}{2})\cos\theta + \frac{1}{\sqrt{3}}(e_b - e_c)\sin\theta$$
$$e_q^e = \frac{2}{3}(e_a - \frac{e_b}{2} - \frac{e_c}{2})\sin\theta - \frac{1}{\sqrt{3}}(e_b - e_c)\cos\theta \quad (4)$$

If Eq. (4) changes into the expression of Eq. (2), the d-q expression of the unbalanced 3-phase voltage can be shown in Eq. (5).

$$e_d^e = e_p\cos\psi_p + e_n\cos(2\omega t+\psi_n)$$
$$e_q^e = -e_p\sin\psi_p + e_n\sin(2\omega t+\psi_n) \quad (5)$$

where subscripts p, and n represent the positive, and negative sequence component respectively and subscripts d and q mean the d-q axis component.

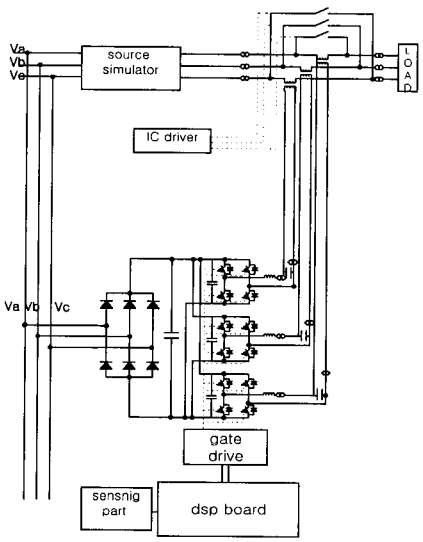


Fig. 4 Overall configuration of SAGCOM

4. The System Modeling of SAGCOM

SAGCOM is connected with the distribution system in series and, after detecting the voltage sag, compensates for the decrease in supply voltage. The system configuration to compensate for unbalanced load voltage is shown in Fig. 4.

Compensation voltage that is generated by 3 single-phase inverters is injected by a series transformer through the LC filter after the process of single-phase bipolar PWM switching.

For system modeling of the SAGCOM controller, the SAGCOM is divided into 2 parts, the voltage source part

and inverter part, and each part is transformed by d-q transformation. Because the load current of the voltage source part is equal to the current injected by the series transformer, the overall configuration of SAGCOM is made by unification of the 2 parts. Since the voltage sag occurs in steady state of the system, system modeling is possible without considering the load.

Before modeling the inverter part, the source voltage conditions are expressed as

$$\begin{aligned} V_{Ia}+ V_{Ib}+ V_{Ic}&\neq 0 \\ i_{Ia}+ i_{Ib}+ i_{Ic}&= 0 \end{aligned} \tag{6}$$

The switching function is defined as

$$\begin{aligned} S_a,\ S_b,\ S_c &= 1 \qquad upper - on \\ S_a,\ S_b,\ S_c &= 0 \qquad lower - on \end{aligned} \tag{7}$$

and the capacitor voltage of the DC link is defined as

$$C_{dc} \cdot \frac{d\,V_{dc}}{dt} = S_a\, i_{ca}+ S_b\, i_{cb}+ S_c\, i_{cc} \tag{8}$$

The state equation of capacitor voltage of the LC filter can be expressed as Eq. (9) ~ (11) and the expression of inverter output current on the d-q axis is described as Eq.(12), (13).

$$C_f \cdot \frac{d\,V_{Ia}}{dt} = i_{ca}- i_{Ia} \tag{9}$$

$$C_f \cdot \frac{d\,V_{Ib}}{dt} = i_{cb}- i_{Ib} \tag{10}$$

$$C_f \cdot \frac{d\,V_{Ic}}{dt} = i_{cc}- i_{Ic} \tag{11}$$

$$i_{cd}- i_{Id} = C_f \cdot \frac{d\,V_{Id}}{dt} + wC_f\, V_{Iq} \tag{12}$$

$$i_{cq}- i_{Iq} = C_f \cdot \frac{d\,V_{Iq}}{dt} - wC_f\, V_{Id} \tag{13}$$

where ω represents the angular velocity of source frequency, and C_{dc} is the capacitance of dc link capacitor. Before modeling of the inverter output voltage, the loss component of the inverter, R_f has to be considered. The expression of the inverter output voltage on the d-q axis is described as Eq.(14), (15).

$$V_{cd}- V_{Id} = L_f \cdot \frac{d\,i_{cd}}{dt} + wL_f\, i_{cq}+ R_f\, i_{cd} \tag{14}$$

$$V_{cq}- V_{Iq} = L_f \cdot \frac{d\,i_{cq}}{dt} - wL_f\, i_{cd}+ R_f\, i_{cq} \tag{15}$$

C_f, L_f : capacitor and inductor of LC filter

i_c, V_c : current and voltage at inverter

i_I, V_I : current and voltage at the transmission

It is possible to control the SAGCOM with system model and compensation of the decrease in supply voltage can be done. After detecting the supply voltage and load current, compensation is possible using a high speed controller. Since the controller always detect the load current, the voltage sag compensation efficiency is improved.

5. Algorithm for Control

It was already proposed the controller that the control loops of an outer voltage for the voltage from capacitors both ends of output voltage and of an inner current for the current from have the double controller. A very useful PI control method was used in the system and IP control was used in parallel to support the PI control, because of a limited output of the controller. Fig. 5 shows a block diagram of the proposed PI double controller [6], [7].

From Eq.(12)~(13), the transfer function of the voltage controller by PI regulator becomes

$$\begin{aligned} \frac{V_{cd}}{V_{cd}^*} &= \frac{K_{vpd}\, s+ K_{vid}}{C_f s^2+ K_{vpd}\, s+ K_{vid}} \\ \frac{V_{cq}}{V_{cq}^*} &= \frac{K_{vpq}\, s+ K_{viq}}{C_f s^2+ K_{vpq}\, s+ K_{viq}} \end{aligned} \tag{16}$$

Meanwhile, the transfer function of the current controller is derived as

$$\begin{aligned} \frac{I_{od}}{I_{od}^*} &= \frac{K_{cpd}\, s+ K_{cid}}{L_f s^2+ (K_{cpd}+ R_f)\, s+ K_{cid}} \\ \frac{I_{oq}}{I_{oq}^*} &= \frac{K_{cpq}\, s+ K_{ciq}}{L_f s^2+ (K_{cpq}+ R_f)\, s+ K_{ciq}} \end{aligned} \tag{17}$$

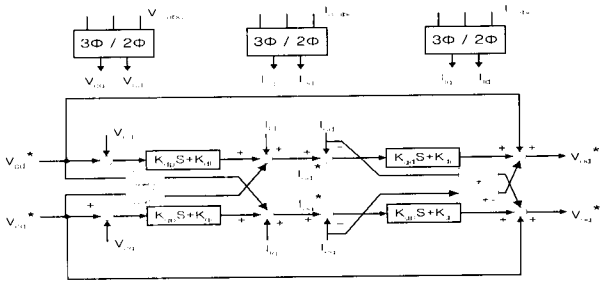
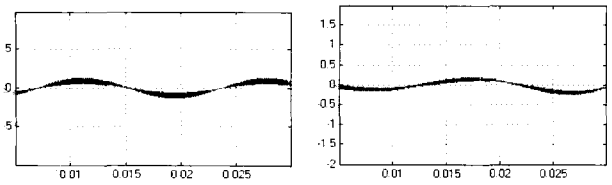
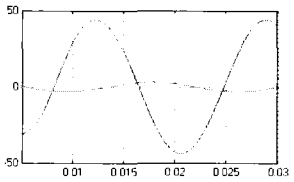


Fig. 5 Block diagram of proposed controller



(a) d component (b) q component



(c) Inverter output voltage

Fig. 6 Characteristics by the 2nd order harmonic

where K_{vp}, K_{vi}, K_{cp}, and K_{ci} are the gain of the PI regulator and L_f, C_f are the inductance and capacitance of the LC filter, respectively. Those are the voltage and current components of the LC filter for controlling the voltage component of inverter.

The d-q transformation of 3-phase unbalanced voltage is shown in Eq.(5). The d-q components of unbalanced voltage are composed of the dc component with constant value and 2nd order harmonic. That is, under the d-q synchronous rotating frame, d-q components of 3-phase unbalanced voltage have a ripple voltage of 120[Hz].

If the 2nd order harmonic exists, even though the decrease in supply voltage is compensated for, the 2nd order harmonic is not removed. So compensation doesn't go well. The waveform of the d-q components of the unbalanced voltage and inverter output voltage are shown in Fig 6.

Since the balances among the positive, negative, and zero sequence components are broken, a negative component or positive component causes a ripple voltage of 120[Hz].

Hence, positive and negative components have to be compensated for and 2nd order ripple voltage must be removed. The ripple voltage of 120[Hz] can be removed by 2 types of filters, delay equalizer and notch filter.

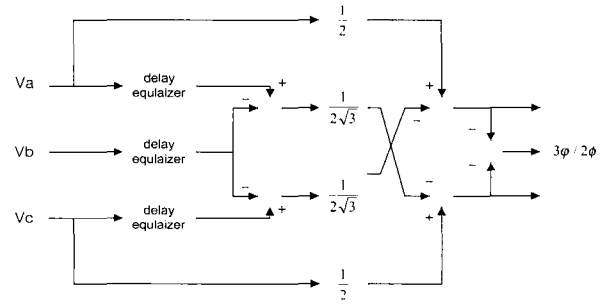
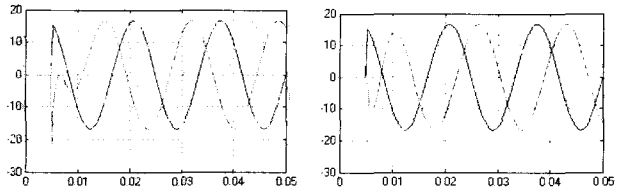


Fig. 7 Delay equalizer



(a) (b)

Fig. 8 Positive and negative component of being divided by delay equalizer

Strictly speaking, positive and negative components are divided by the delay equalizer to prevent which used phase delay without changing amplitude ripple voltage.

A block diagram of the delay equalizer is shown in Fig. 7. The transfer function of the delay equalizer is shown in Eq.(18).

$$N(s)=\frac{s^2-a_1 s+a_0}{s^2-a_1 s+a_0} \tag{18}$$

Positive and negative components that are divided by delay equalizer are shown in Fig. 8.

In case the delay equalizer is used, d-q components have a DC value. The d-q expression that is filtered by delay equalizer is shown in Fig. 9

Another method to remove the ripple voltage is the notch filter, which removes, only ripple voltage. A block diagram for removing the ripple voltage of d-q components is shown in Fig. 10.

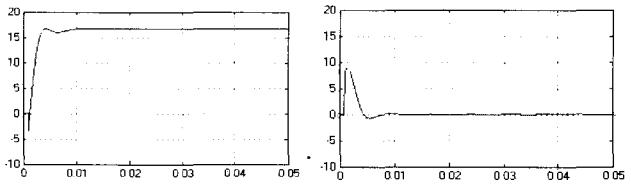
The transfer function of the notch filter is defined as

$$N(s)=\frac{s^2+W_e^2}{s^2+W_e/Qs+We^2} \tag{19}$$

d axis components are shown in Fig. 11.

The waveform of (a) is the case in which no notch filter is used. The ripple voltage of 120[Hz] exists. When the notch filter is used, the ripple voltage is removed. So the d axis component becomes zero.

Simulation is conducted to verify the compensation performance. The delay equalizer is used, and the SAGCOM controller has a double control loop, which is constructed with a voltage controller and a current controller.



(a) d component (b) q component

Fig. 9 the d-q components filtered by the delay equalizer

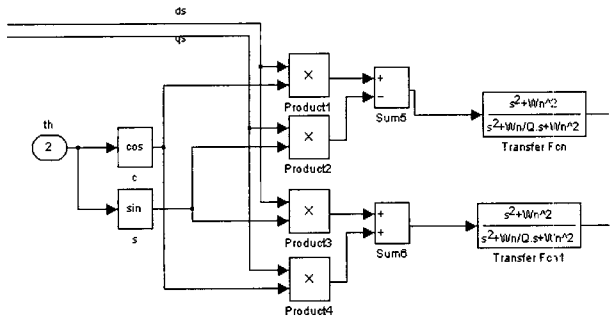


Fig. 10 Notch filter block of d-q component

Two types of controllers, an analog controller and a digital controller, are constructed. In real system, digital controller is adopted in simulation because SAGCOM uses that. For changing the analog controller into digital controller, transfer function of PI controller[8][9].

$$\frac{V_o(s)}{V_i(s)} = K_p + \frac{K_i}{s} \tag{20}$$

backward Euler method is applied. If 's' replaces with $\frac{z-1}{Tz}$, Eq.(20) is changed into Eq.(21).

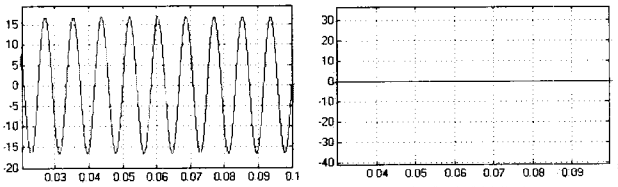
$$\frac{V_o(z)}{V_i(z)} = (K_p + K_i \frac{Tz}{z-1}) = \frac{(K_p + K_i T)z - K_p}{z-1} \tag{21}$$

The PI controller that is changed by Z transformation is shown in Eq.(22)

$$\frac{V_o(z)}{V_i(z)} = \frac{(K_p + K_i T)z - K_p}{z-1} \tag{22}$$

The unbalanced voltage is divided into positive, negative, and zero sequence components, and control of 5 variables (that is, d, q components of positive and negative components in addition to zero sequence components) is achieved.

Conventional PI control is impossible in unbalanced power systems. When an SLG fault occurs, and supply voltage becomes unbalanced, the filter that removes ripple voltage of 120[Hz] is necessary for d-q transformation control and the control of 5 variables must be performed. In the case of the PI double control of unbalanced power system using d-q transformation, such condition is uneffective.



(a) without notch filter (b) with notch filter

Fig. 11 d axis component

Using differential control for reducing steady-state error of the PI controller, proposed PID controller has a good transient response and improves system stability.

The PID controller that is supplied in compensation system uses direct control of the 3-phase without d-q transformation. Because the proposed PID controller adopts a discrete-time control method, Z transformation is used.

$$G(s) = K_d S + K_p + \frac{K_i}{S} \tag{23}$$

Eq.(23) is changed into Eq.(24) by the forward Euler method.

$$G(z) = \frac{K_d z^2 + (K_p T - 2K_d)z + (K_i T^2 - K_p T + 1)}{zT - T} \tag{24}$$

The transfer function being applied to the system is the capacitor voltage component, which can be expressed as

$$Vc(s) = \frac{\frac{1}{C_f}}{(L_f s + R_f) + \frac{1}{C_f}} Vs(s) \tag{25}$$

As expected, Eq.(25) is changed into Eq. (26) using z-transformation.

$$N(z) = \frac{T}{L_f C_f (z-1)^2 / T + R_f C_f (z-1) + T} \tag{26}$$

Eq.(27) is obtained from Eq.(24), (26) using the pole-zero cancellation method.

$$Y(z) = N(z)G(z) = \frac{TW_c}{(z-1)} \tag{27}$$

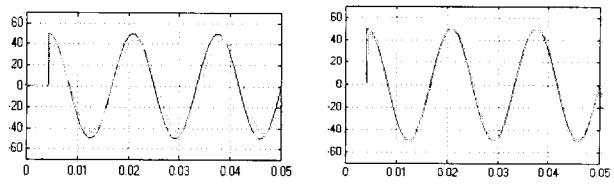
So the each control gain can be obtained. The control gain of transfer function that is obtained by the backward Euler method agrees with the control gain by forward Euler method.

To estimate the compensation characteristics, simulation was done using MATLAB Simulink based on the calculated parameters.

Table 2 shows the parameters used for the simulation.

Table 2 Simulation parameter

parameter	value
Source voltage	50[v]
Frequency	60[Hz]
Sampling time	100[us]
Load(R-L)	24[Ω]
Cf(filter)	40[μF]
Lf(filter)	6e-4[mH]



(a) PI dual control (b) PID control

Fig. 12 Between PI dual and PID control comparison

Tow control method was simulated with the reference as the same condition that voltage sag occurred at 4.3[ms]. PI dual control method at Fig 12. (a) appeared to make a signigicant difference over 5[%] of steady-state errors, otherwise, PID control like Fig 12. (b) resulted in a difference of less than 0.2[%].

PI dual control also had an overshoot of about 1.2 times the reference voltage. Phase delay is shown in Fig. 12 (a) and is a weak point of synchronous rotating frame. Given gain conditions, the PI dual controller was controled hardly to tune as the limitation of 5-variables control condition, and bandwidth of each voltage and current couldn't be approved over maximum 400, 1200 degree. Besides the 5-variable control, the detection between positive seq. and negative seq. and the control after d,q transformation became complicated during simulation processing. When programmed for the experiment, the code length and processing time from transformation and 5-variable control will be increased.

6. Experiment Results

The algorithm being used in main processor is shown in Fig. 14. The program tool used code-composer and TI XD510. The configuration of the system is composed of control parts, inverters, LC filter, and series transformer.

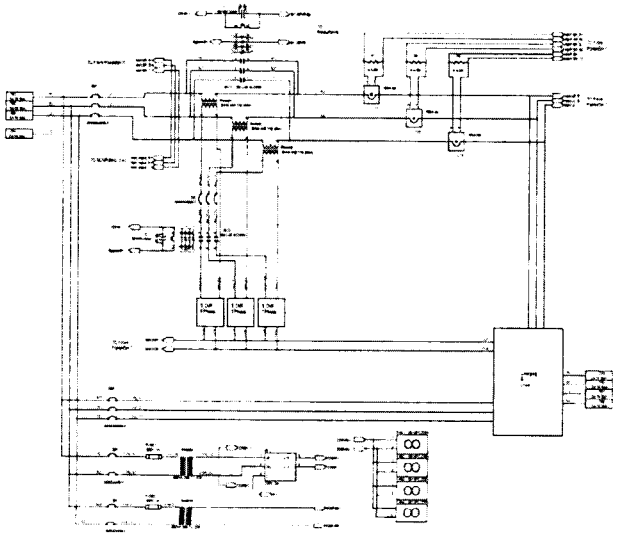


Fig 13 A circuit diagram for the system

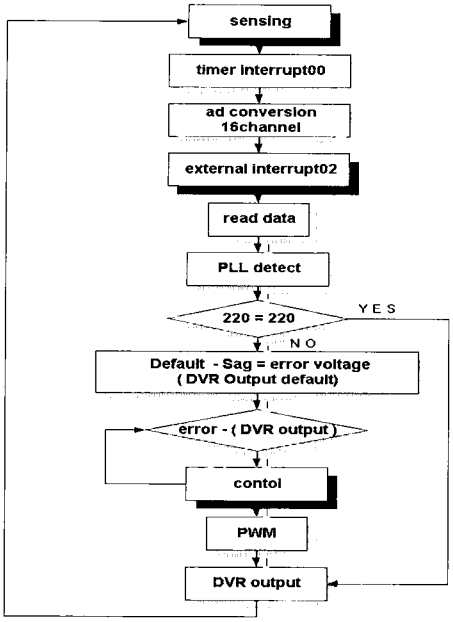


Fig. 14 The overall configuration algorithm

The control parts are composed of TMS320C31 DSP used as the main processor, an address decoder, Altera's max7000 for PWM, and sensing board using FLEX10K for detecting voltage sag.

Table 3 Experimental parameter

parameter			value
Capacity			15[KVA]
Reference voltage			380[V]
Fundamental frequency			60[Hz]
Switching frequency			6[kHz]
DC Link voltage			540[V]
Series transformer ratio			2:1
Linear load			24Ω
L(filter)	0.6[mH]	C(filter)	40[μF]

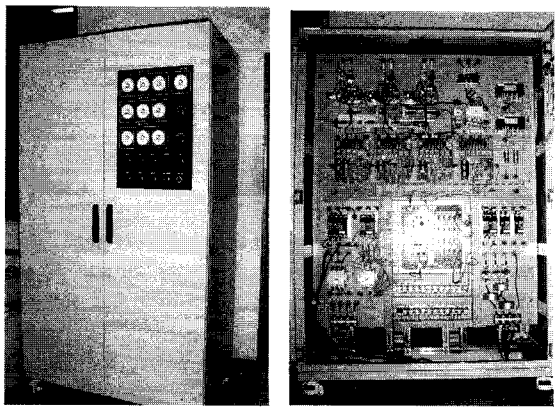


Fig. 15 producted compensation system

Table. 3 shows parameters used for the experiment.

The inverter parts are composed of 3 IGBT inverters using a single-phase bipolar switching method. The LC filter has a 1[kHz] cutoff frequency and the series transformer has 3 taps for testing the influence of the winding ratio. DC link is made 540[V] using 3 phase diode rectifier. For braking the compensation system when the fault occurs, a bypass switch was constructed. The experiment conditions are a source (voltage sag) of 120[V] and compensation voltage of 100[V] for phase voltage compensation of 220[V].

The waves are measured by DA converter channels of the main board.

6.1 PID Control Gain Improvement

To confirm the PID controller's efficiency, an experiment is performed with the same conditions as the simulation. Fig. 16 shows comparison between reference and controled voltage. A controled voltage is the detected waveform at a capacitor. gain parameters weren't yet tuned, but a 1[%] steady-states error was better than that of the PI dual controller on the simulation. It had a problem that phase differences were about 21[°] like at the simulation. Being gain tuned, command voltage, differences between source voltage and voltage sag, and sensing capacitor voltage which is compensated voltage detected through DA converter are shown Fig. 17. The waveform was distorted by the noise made from inverter switching, but the controlled voltage had a good dynamic response.

6.2 Phase Synchronization

A waveform to prove detected PLL is shown in Fig. 18. This is the result of the phase angle, theta, detected using the PLL algorithm, coinciding with source voltage. Fig. 18 (a) shows a waveform source voltage comprised of be capacitor voltage(compensated voltage) made the theta detected. Source voltage couldn't be seen due to the switching noise on capacitor voltage, but the proved phase synchronization. The comparison Between voltage sag and optional voltage using the theta detected are shown in Fig. 18 (b). Capacitor voltage had a phase delay as the switching noise and DA converter offset, but optional voltage at (b) was well done phase synchronization.

6.3 Compensation Limit

When source voltage is reduced within 1[min], figures the result is shown in the following to prove the efficiency of compensation system. The system can compensate the voltage sag from 10[%] to 50[%] of source voltage. Fig. 19 shows voltage sag reduced 20[%] and compensated load voltage. When voltage sag is 180[V], load voltage was compensated for almost up to 220(rms)[V] without steady-stats error and synchronous load voltage coincided with source voltage. When voltage sag was 120[V] and command voltage was 100[V], load voltage was 215(rms)[V] with steady-states error under about 0.05[%]. As series transformer's ratio was 2:1, a capacitor voltage must be 200[V]. Fig. 20 shows that waveforms. Phase delay between source voltage and load voltage is shown (a), but the system was able to compensate for up to 50[%] of voltage sag.

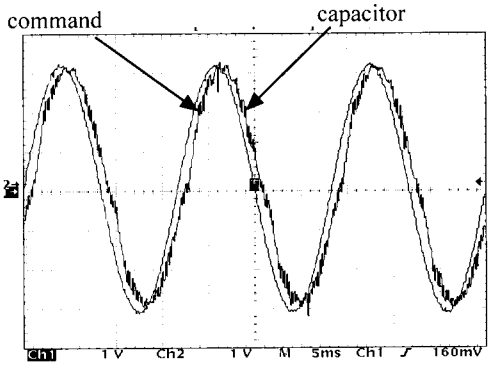
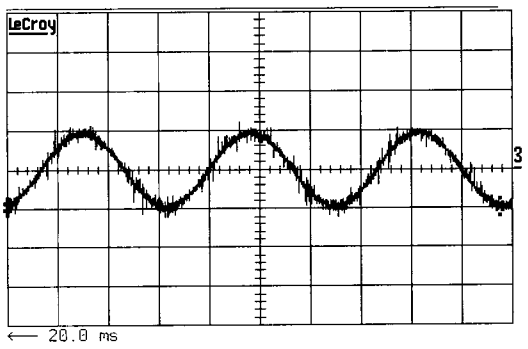
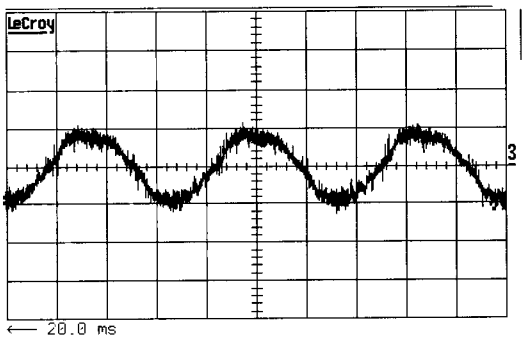


Fig 16 capacitor voltage using PID controller(80[V/div], voltage 250[V], 5[ms/div]) (Kd: 2.6e-5, Kp:0.066, Ki=1100)

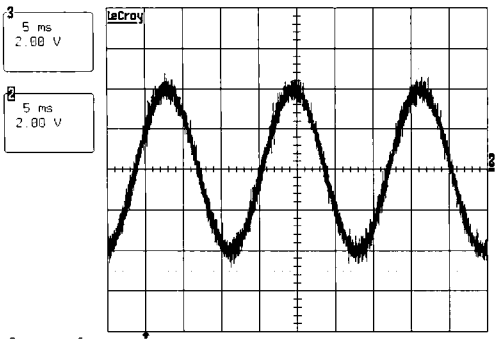


(a) reference voltage (command voltage)(80[V/div], voltage 160(RMS)[V], 5[ms/div])

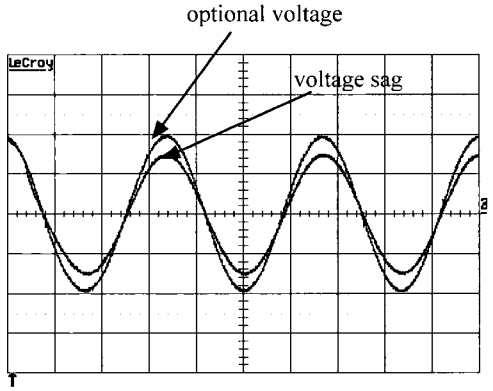


(b) capacitor voltage (compensated voltage)(80[V/div], voltage 160(RMS)[V], 5[ms/div])

Fig 17 Comparison both voltage (Kd: 6e-5, Kp=0.18, Ki=1800)



(a) source and capacitor voltage synchronization



(b) synchronization with voltage sag (160[V/div], voltage 311V, 5[ms/div])

Fig. 18 PLL detection

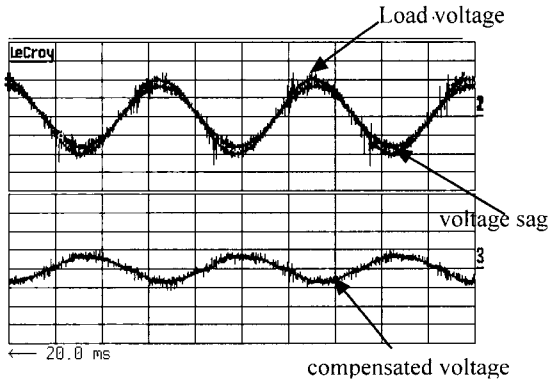
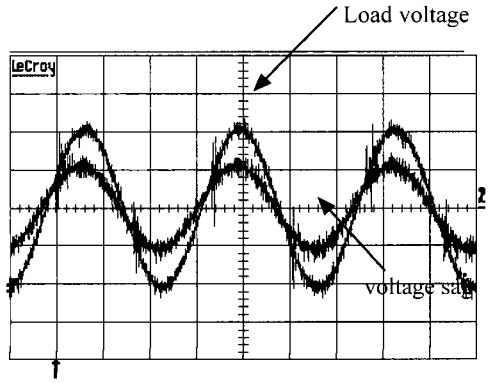
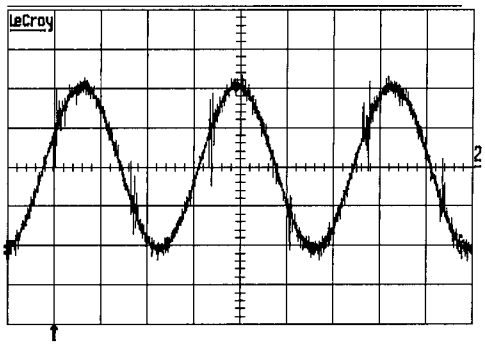


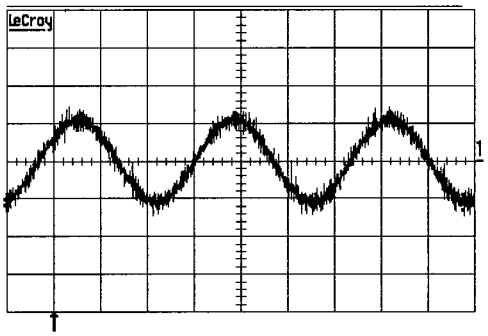
Fig. 19 compensation up to 20[%] (80[V/div], 5[ms/div])



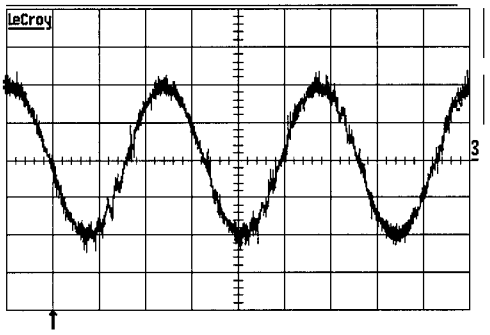
(a) voltage sag and load voltage



(b) Load voltage (220[V](RMS))



(c) voltage sag (120[V])



(d) compensated voltage (200[V])

Fig. 20 compensation up to 50[%] (80[V/div], 5[ms/div]) (Kd: 6e-5, Kp=0.18, Ki=1800)

7. Conclusion

PI control using generally method of performance of the compensation system, SAGCOM, for voltage sag has a dual control scheme as he compensation both current and voltage, also synchronous coordinate frame in unbalanced sources complicated to control separate positive and negative seq. voltage without simpleness, an advantage point, stationary coordinate frame must compensate zero-voltage too.

So d.q trans has not a great significance about 2 variable control of dq frame.

But the result using PID control at 3 phase gave much more the efficiency that steady-states error has about 0.05[%] and the system is able to compensate up to 50[%] than PI control.

And realization of PID controller rather than PI dual controller at synchronous frame was simple.

Now it must be compensated voltage sag within 20ms and be proved about transient condition. Also it will be considered switching noise.

Acknowledgement

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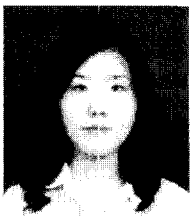

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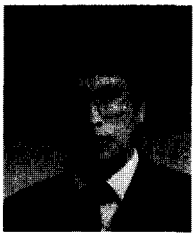

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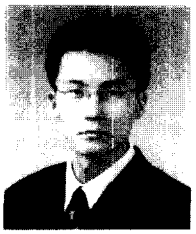

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