Reproducible Chemical Mechanical Polishing Characteristics of Shallow Trench Isolation Structure using High Selectivity Slurry

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Chemical mechanical polishing (CMP) has become the preferred planarization method for multilevel interconnect technology due to its ability to achieve a high degree of feature level planarity. Especially, to achieve the higher density and greater performance, shallow trench isolation (STI)-CMP process has been attracted attention for multilevel interconnection as an essential isolation technology. Also, it was possible to apply the direct STI-CMP process without reverse moat etch step using high selectivity slurry (HSS). In this work, we determined the process margin with optimized process conditions to apply HSS STI-CMP process. Then, we evaluated the reliability and reproducibility of STI-CMP process through the optimal process conditions. The wafer-to-wafer thickness variation and day-by-day reproducibility of STI-CMP process after repeatable tests were investigated. Our experimental results show, quite acceptable and reproducible CMP results with a wafer-to-wafer thickness variation within 400 Å.

Keywords : chemical-mechanical polishing (CMP), shallow trench isolation (STI), reliability high selectivity slurry (HSS), reproducibility

1. INTRODUCTION

Chemical mechanical polishing (CMP) has become the method choice for reducing the surface topographies of device wafers due to its ability to planarize both interlevel dielectrics and metals. Especially, shallow trench isolation (STI) process has been attracted attention for high density of semiconductor device as an essential isolation technology. STI facilitates the planar devices and higher IC packing densities[1], making it an attractive process for device isolation compared with conventional and modified local-oxidation-of-silicon (LOCOS) schemes. After defining shallow trenches to isolate active device regions physically, a blanket oxide deposition fills the trenches and covers the silicon nitride trench-etch mask regions. Then CMP polishes the trench-fill oxide to expose silicon nitride across all active device regions.

The introduction of CMP in STI process that could be dramatically simplified the planarization process without the complicated reverse moats etch process, have obtained the good planarization characteristics. However, the various defect problems was still generated[2,3], such as dishing effects[4], damages of active silicon region, and nitride residues[5], because the removal rates of each region were different and the correct end-point detection (EPD) was difficult in the direct STI-CMP process [6]. An excessive CMP process gives damage in silicon active area, while an insufficient CMP process remain a nitride residue on the active region.

In this paper, through the analysis of above planarization characteristics, we will determine the process control limit (upper and lower limit) that can minimize the dishing effects in the large field area. As a result, we can perfectly remove the silicon oxide film on the silicon nitride film in the moat region. Also, we will

estimate the reliability through the repeat tests with the optimized process conditions in order to identify the reproducibility of HSS STI-CMP process[7,8].

2. EXPERIMENTAL

Figure 1 schematically shows the fabrication procedure of STI pattern wafer. STI patterned wafers were used in this experiment were p-type boron doped (100) oriented silicon wafers of 8-inch size. A 150Å thermal oxide was deposited in electric furnace, as well as 2000Å nitride film using low-pressure chemical vapor deposition (LPCVD) in NH_3 and dichloro silane (DCS) at 750 °C for 120 min. Afterwards, trench depth of 3500Å was formed by moat pattern and dry etch. Then, linear oxidation was deposited by 270Å in electric furnace in O_2 at 900 °C for 60 min, and then was annealed in N_2 at 100 °C for 15 min. Continually, STI-fill oxide of 8000Å was deposited by atmosphere chemical vapor deposition (APCVD), finally STI-CMP polishing was performed using high selectivity slurry (HSS).

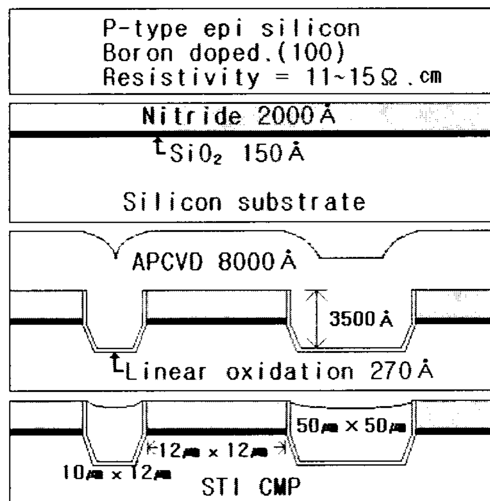


Fig. 1. Fabrication sequence of STI pattern wafer.

Table 1. Size of each region for thickness measurements.

Region	Size	Remarks
Large field	50 ㎛× 50 ㎛	Large field oxide area
Dense field	10 ㎛× 12 ㎛	Dense field oxide area
Large moat	80 ㎛× 250 ㎛	Device formation area
Dense moat	12 ㎛× 50 ㎛	Area surrounded by STI region

Table 2. Optimized recipe of additive mixing.

	DIW	TMAF	KOH	H_2O_2
Mixing ratio	200	70	8	1
wt %	-	4.26	0.87~0.92	0.14

In order to solve the various process defects that occur in STI CMP process, Table 1 represents the size of each region for STI pattern wafer. CMP polishing was done on an IPEC Avanti 472 polisher. The optimized recipe of HSS additive mixture summarizes in Table 2.

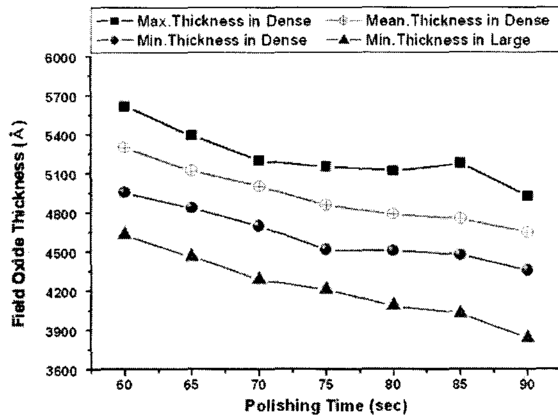
The post-CMP cleaning was rinsed by SC-1 chemicals and diluted HF (DHF). After the rinse step, the wafer surface was dried by spin rinse dry (SRD). Nano Metrics M8000X and Rudolph Ellipsometer FE VII systems were used to measure the thickness of oxide and nitride. Prior to experiment, the dummy wafers were polished in order to stabilized the CMP polisher. Next, we determined the optimized polishing time after polishing the sample wafer for 70 sec. Then, we polished the every test sample wafer with 5 seconds-interval. Also, in order to estimate the reliability between test wafers, we measured the thickness of position those wishes to evaluate in pattern wafer before CMP process. After that, we polished the pattern wafer with trench depth of 3500 Å for 63 seconds under stable process conditions. The repeatability of these polished wafers measured and polishing characteristics before and after CMP process was evaluated after cleaning process.

3. RESULTS AND DISCUSSION

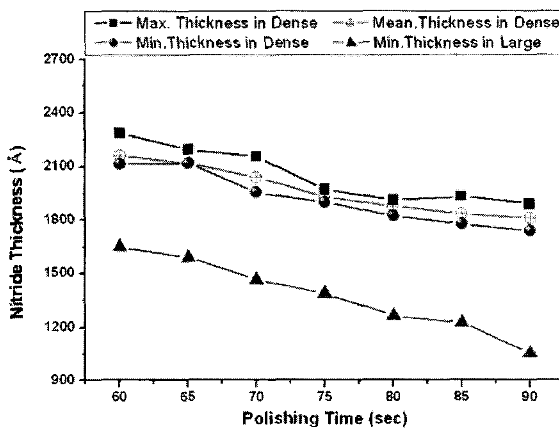
The determination of process margin in the STI-CMP process is very important parameter with regard to polished thickness control. That is to say, it is very effective to decide the upper limit and lower limit conditions, which can entirely remove silicon oxide on silicon nitride film of the dense moat region as reducing silicon damages of moat area, and minimizing a dishing effect in the large field region. Therefore, the lower limit of polishing thickness was defined to the range that do not generate the moat damages, and the upper limit was determined to the range that nitride residues after CMP polishing are not remaining.

Figure 2 (a) and (b) show the post-CMP thickness of field oxide and silicon nitride films in the large and dense moat area as a function of polishing times, respectively. CMP polishing was performed with 5 second-intervals, the results of sample wafer polishing, oxide film on moat area entirely removed. Thickness linearly decreases as the polishing time increases, and the oxide removal rate of the large area appeared more

highly than that of dense area. The dishing and moat damages did not occur, but we found that the nitride residue occurs at the pattern wafer polished during 60 and 65 seconds. The post-CMP thickness range where can remain nitride residues was an average value of 5120 Å and maximum value of 5392 Å . From the polishing result of Fig. 2, therefore, we could estimate that the upper limit of process margin for stable process without nitride residues was by average of 5000 Å and maximum value of 5300 Å. Next, it is important to decide the lower limit for minimizing the dishing effect.



(a)



(b)

Fig. 2. (a) Field oxide and (b) nitride film thickness as a function of polishing time.

Figure 3 shows the variation of field oxide thickness in the large and dense field region as a function of polishing time. The upper limit was same as previous result (Fig. 2), but the lower limit has to determine from Figure 3 because the nitride residues were occurred in the pattern wafer, which were polished during 75 and 80 seconds. And the moat damages were generated in the second polishing lot when the polishing time is 90 seconds. When the moat damages occurred, the average thickness of dense field region was 3991 Å, and minimum thickness in the large field area was 3498 Å, respectively. Therefore, we could conclude that the lower limit of process margin was the average of 4000 Å, and oxide thickness in the large field area must become over the minimum value of 3500 Å, because the trench depth is 3500 Å.

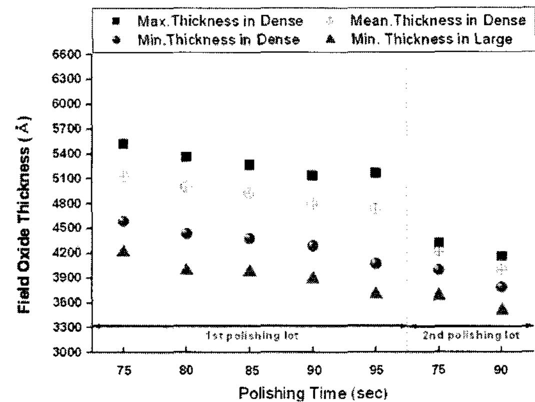
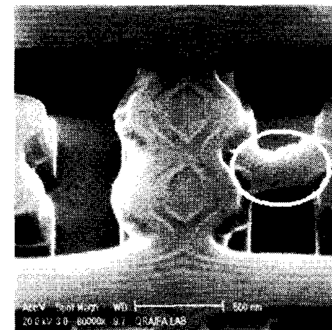
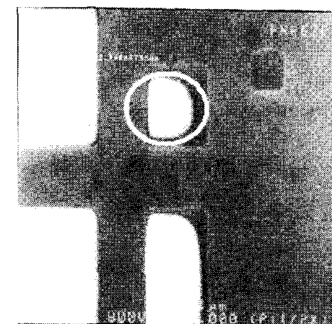


Fig. 3. Field oxide thickness as a function of polishing time.

Figure 4 (a) shows nitride residues that were generated on wafer, which polished during 75 and 80 seconds, and Figure 4 (b) is moat damage in result of over polishing in 90 seconds, respectively.



(a)



(b)

Fig. 4. (a) Nitride residue (b) Moat damage.

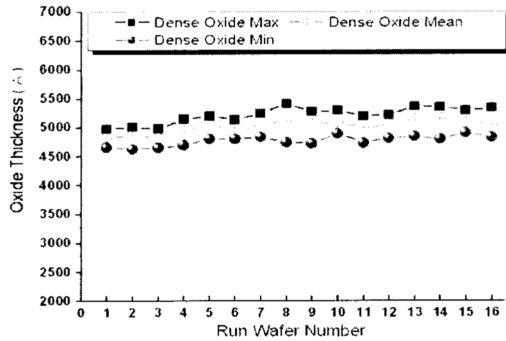


Fig. 5. Oxide thickness as a function of run wafer number in the dense moat area.

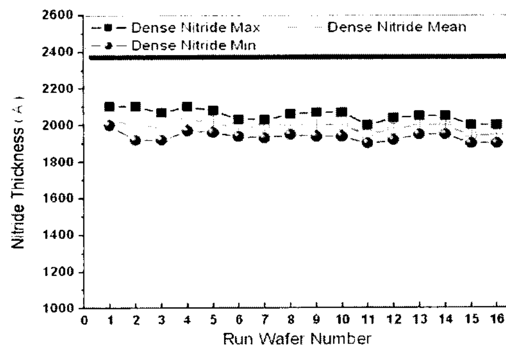
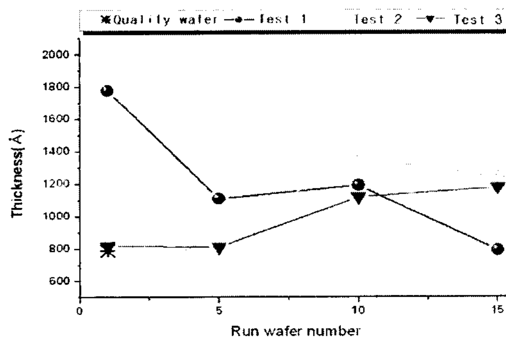
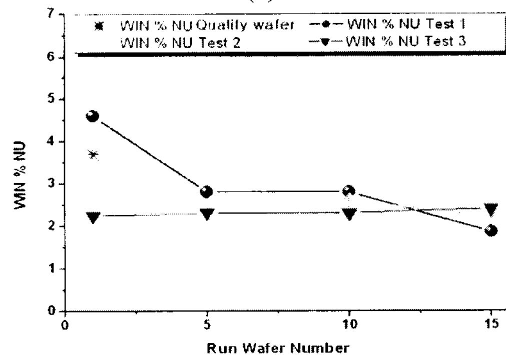


Fig. 6. Nitride thickness as a function of run wafer number in the dense moat area.

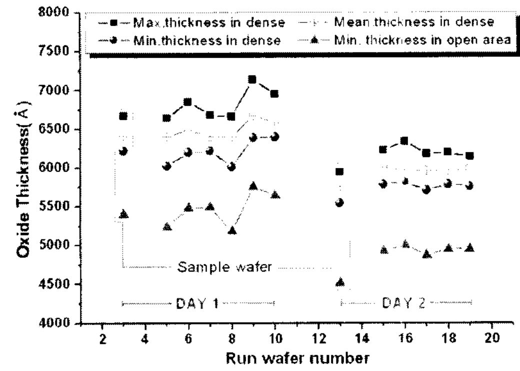


(a)

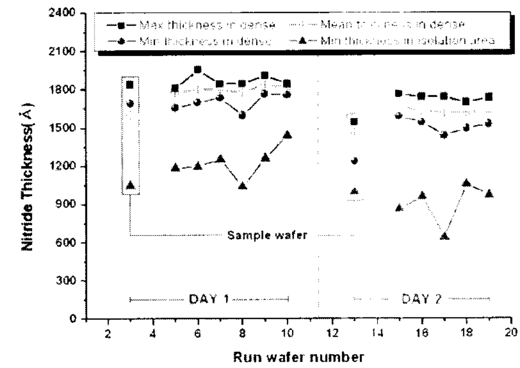


(b)

Fig. 7. (a) Oxide thickness and (b) non-uniformity as a function of run wafer number.



(a)



(b)

Fig. 8. (a) Oxide thickness and (b) nitride thickness as a function of run wafer number.

Figure 5 and Figure 6 show the oxide and nitride thickness in the dense moat region as a function of polished wafer count, respectively. The post-CMP thickness of oxide and nitride film on dense moat area showed a very good reproducibility that thickness variations were controlled within 400Å.

Figure 7 shows the oxide thickness variation and within wafer non-uniformity (WIN%NU) as a function of polished run number. In order to confirm the reproducibility of STI-CMP process using self-developed HSS, we had repeated the same experiment by three times. As the run wafer numbers are increasing, oxide thickness was more closed the qualify value, where, the value of qualify wafer means the target value of this HSS STI-CMP process. Especially, the within wafer non-uniformity showed a good result below 3 % NU. We think that some variations of oxide thickness due to the effect of consumables. This indicates that it is necessary to pre-polish the dummy wafer before CMP process.

Next, we had performed the same experiments for 2 days in order to estimate the process reliability of high selectivity slurry. Figure 8 (a) and (b) show the oxide and nitride thickness variation as a function of run wafer number. There was no apparent thickness difference

between day 1 and day 2. This means that our self-developed HSS is very superior. Similarly to Fig. 7, some variations of thickness were caused by the degradation of consumables.

4. CONCLUSION

Through the above experiments, we could notice the importance of the process control limit, which can entirely remove the silicon oxide film on silicon nitrides from high density of moat area as reducing the damage of moat area and minimizing dishing effect in large field area. The upper limit of post-CMP thickness, which can remain the nitride residues, was the ranges from average 5000 Å to 5300 Å. Also, the lower limit of post-CMP thickness without moat damages was average 4000 Å, and thickness limit in the large field oxide region must become more than minimum 3500 Å, which is trench depth. Finally, the target of post-CMP thickness is average 4500 Å, upper and lower limit are +/-500 Å, and maximum value of dense area must be maintained within 5300 Å. In addition, oxide thickness in the large field area must become more than 3500 Å, which is trench depth for minimizes dishing effect. In the case of same polishing process, the experimental results of thickness variation within wafer and the process reproducibility, the thickness difference of the maximum and minimum values of the within-wafer was controlled within 400 Å.

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REFERENCES

[1] S. Nag and A. Chatterjee, "Shallow trench isolation for sub-0.25 μm IC technologies", Solid State Tech., p. 129, 1997.

[2] S. W. Park, S. Y. Kim, and Y. J. Seo, "Improvement of pad lifetime using POU (point of use) slurry filter and high spray method of de-ionized water", J. of KIEEME(in Korean), Vol. 14, No. 9, p.707, 2001.

[3] C. B. Kim, S. Y. Kim, and Y. J. Seo, "Characteristics of slurry filter for reduction of CMP slurry-induced micro-scratch", J. of KIEEME(in Korean), Vol. 14, No. 7, p. 557, 2001.

[4] K. Smekalin, "CMP dishing effects in shallow trench isolation", Solid State Tech. p. 187, 1997.

[5] S. Y. Kim, C. I. Kim, E. G. Chang, Y. J. Seo, T. H. Kim, and W. S. Lee, "An optimized nitride residue phenomena of shallow trench isolation (STI) process by chemical mechanical polishing (CMP)", IUMRS-ICEM, p. 106, 1998.

[6] S. Y. Kim, C. J. Park, and Y. J. Seo, "Signal analysis of end point detection (EPD) method based on motor current (MC)", IUMRS-ICEM 2002, p. 509, 2002.

[7] C. B. Kim, S. Y. Kim, S. Y. Jeong, and Y. J. Seo, "Global planarization of direct STI-CMP process using high selectivity slurry", Proc. of VLSI Multilevel Interconnection Conference, p. 222, 2001.

[8] S. Y. Kim and H. S. Chung, "A study on characterization and modeling of shallow trench isolation in oxide chemical mechanical polishing", Trans. on EEM, Vol. 2, No. 3, p. 24, 2001.