Failure Analysis for High via Resistance by HDP CVD System for IMD Layer

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As the application of semiconductor chips into electronics increases, it requires more complete integration, which results in higher performance. And it needs minimization in device design for cost saving of manufacture. Therefore oxide gap fill has become one of the major issues in submicron devices. Currently HDP (High-Density Plasma) CVD system is widely used in IMD (Inter Metal Dielectric) to fill narrower space between metal lines. However, HDP-CVD system has some potential problems such as plasma charging damage, metal damage and etc. Therefore, we will introduce about one of via resistance failure by metal damage and a preventive method in this paper.

Keywords : HDP (High-Density Plasma), plasma charging damage, metal damage, Gap fill, IMD (Inter Metal Dielectric), Via Resistance

1. INTRODUCTION

HDP process simultaneously performs deposition and sputter etches. And the temperature of this process strongly depends on sputter etch which could rise its temperature because of bombardment of Ar ion to oxide by HF (High frequency) RF power[1,3]. With that reason HDP CVD system makes the process temperature cool down by flowing He gas that has high thermal conductivity to a wafer backside and uses ESC (Electrostatic Chuck) to chuck a wafer to maintain the status of floating it[2,4]. We had found wafers having high via resistance failure out of spec value (Fig. 1), which were processed for IMD on HDP-CVD system. The failures were often found in the other via resistance as well in DC test (e.g. via 2 or via 3). Form the result of SEM analysis for the failed point of via resistance, the phenomenon of empty, thickening or thinning of Al on metal layers (Ti/TiN/Al/Ti) was found (Fig. 2 & Fig. 3) [5-7]. We have frequently experienced locally melted metal, when the He leak error on backside of a wafer occurred.

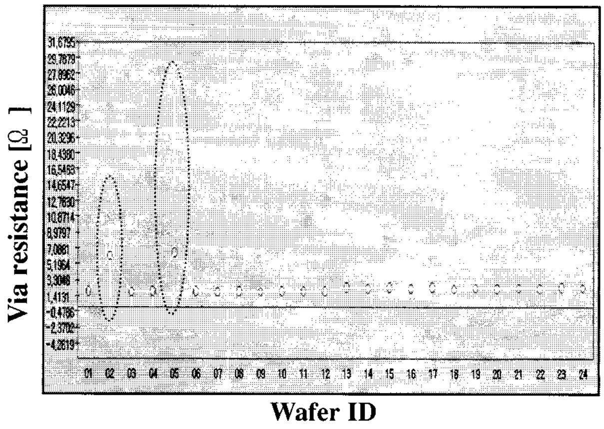


Fig. 1. High resistance of via chain.

In most of those cases the vacant or migrated points of Al were not over whole of a wafer but near the edge. So we experimented the following test to find what process parameters could make Al migrated, thick or thin and how to prevent from it.

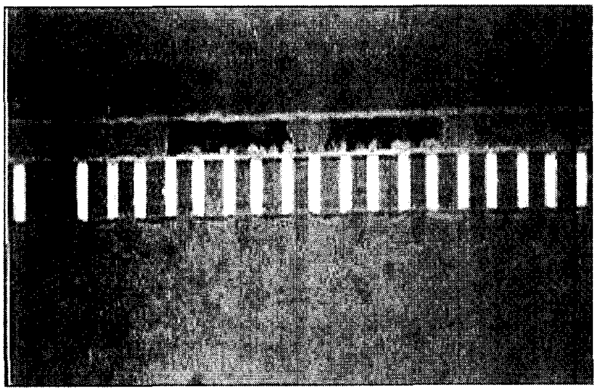
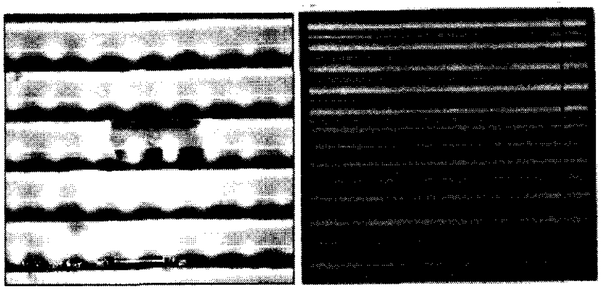


Fig. 2. Vacancy of Al on metal layer [SEM].



(a) (b)

Fig. 3. Vacancy(a) and normal state(b) of Al[Top view].

2. EXPERIMENTAL

The experiment was tested on Novellus SPEED chamber for HDP-CVD, which has two different type of RF power. One is LF (Low Frequency)-RF that implements dissociation of gas in a chamber and the other is HF-RF that enables Ar ion to carry out sputter etch.

On this system there are three main process parameters of LF-RF, HF-RF and backside He gas that could have an effect on process temperature. The set values of the baseline process were 3500W of LF-RF, 3000W of HF-RF and 8 Torr of backside He pressure.

And Figure 4 and Table 1 illustrate how the process temperature of the baseline to help understood how HDP-CVD system works. We respectively tested for those and examined how much those items effected on the process temperature.

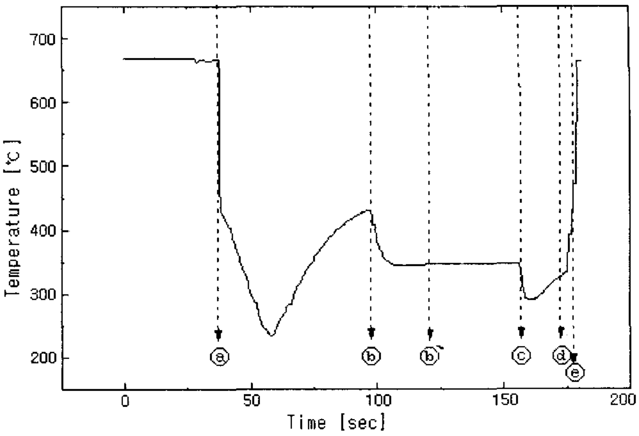


Fig. 4. Process temperature profile of the baseline.

Table 1. Description for Fig. 4.

Section	Description
ⓐ	wafer-in and process starts
ⓐ ~ ⓑ	preheating
ⓑ ~ ⓒ	chucking, cooling and main process is on (HF-RF on)
ⓑ' ~ ⓒ	stabilized process temperature
ⓒ	turning off backside He and HF-RF
ⓓ	discharging chuck
ⓔ	opening slit valve and wafer-out

3. RESULTS AND DISCUSSION

The test 1 was done for 3100 / 3300 / 3500 / 3700 / 3900 W of LF RF under the condition of UBUC (UnBiased UnClamped) in which only LF-RF is turned on and no chucking and Figure 5 and Table 2 show the results of process temperature of the section from ⓑ` to ⓒ which are the stabilized temperature.

There was no much change in temperature by LF-RF power (Fig. 6).

The test 2 was done for 2600 / 2800 / 3000 / 3200 / 3400 W of HF-RF under the condition of BC (Biased Clamped) in which both of LF-RF and HF-RF is turned on and Figure 7 and Table 3 show the results of process temperature of the section from ⓑ` to ⓒ.

As Figure 8 shows there was more variation in temperature by about 20℃/200 W. The maximum change

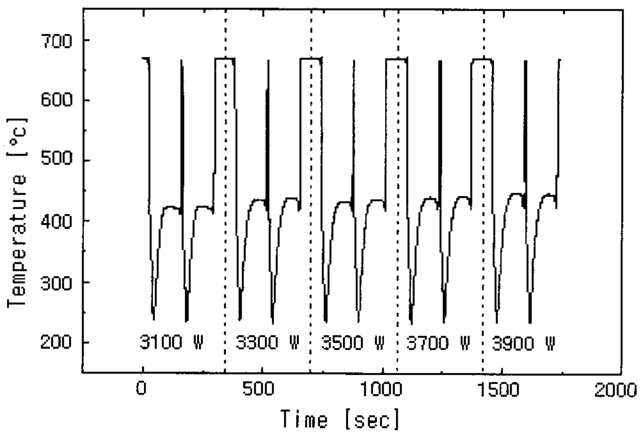


Fig. 5. Temperature profile by LF-RF.

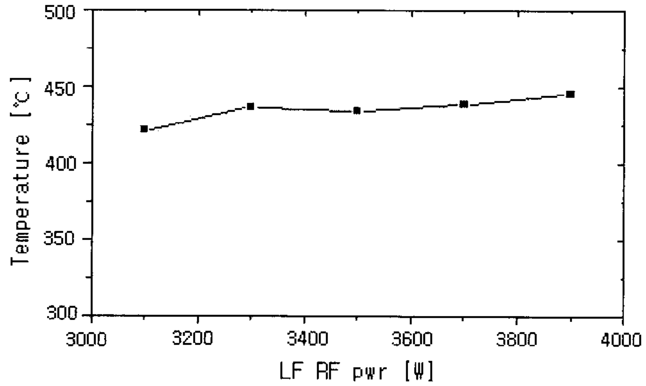


Fig. 6. Stabilized temperature by LF RF.

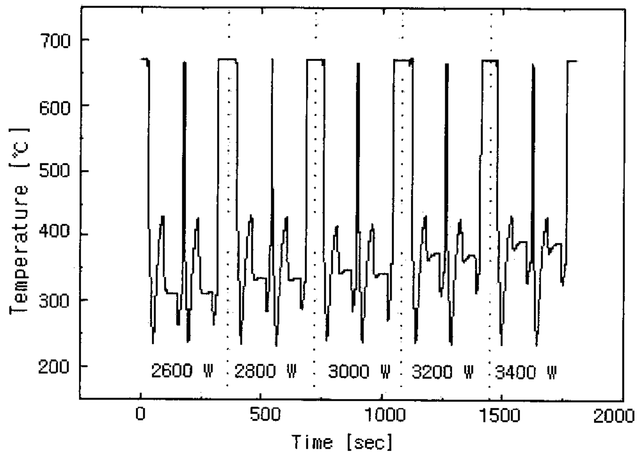


Fig. 7. Temperature profile by HF-RF.

Table 2. Temperature variation by LF-RF.

LF-RF [W]	Temperature [℃]	Difference [L_n-L_{n-1}]
L_1 3100	421.1	
L_2 3300	436.6	15.5
L_3 3500	434.1	-2.5
L_4 3700	438.5	4.4
L_5 3900	445.4	6.9

Table 3. Temperature variation by HF-RF.

HF-RF [W]	Temperature [℃]	Difference [H_n-H_{n-1}]
H_1 2600	310.1	
H_2 2800	332.4	22.3
H_3 3000	345.9	13.5
H_4 3200	364.4	18.5
H_5 3400	390.7	26.3

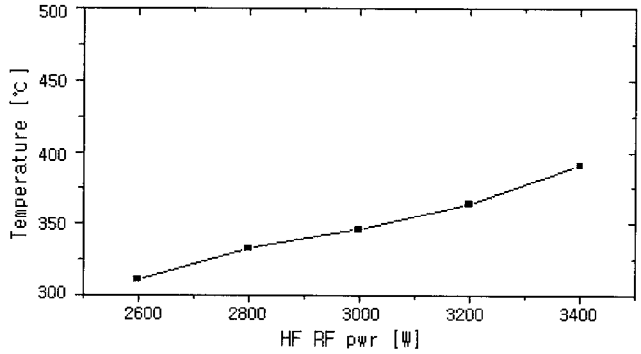


Fig. 8. Stabilized temperature by HF RF.

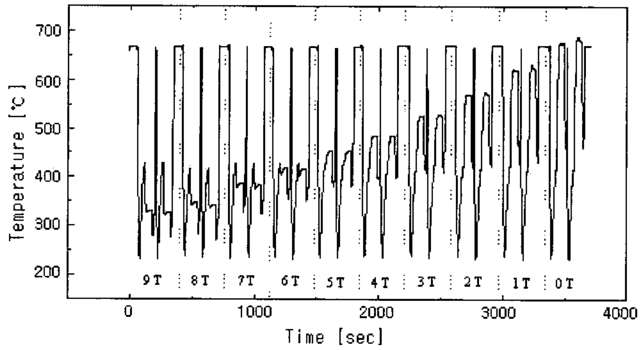


Fig. 9. Temperature profile by backside of He pressure.

was 80.7 ℃ in change from 2600 w to 3400W.

The test 3 was done for pressure of He gas flowing to the backside of a wafer that were from 9 Torr to 0 Torr decreasing 1 Torr under the condition of BC and Figure 9 and Table 4 show the results of process temperature of the section from ⓑ\` to ⓒ.

Figure 10 illustrates the flow rate of He gas by its pressure. According to the test the most effective factor to the process temperature was He pressure flowing to backside of a wafer was shown (Fig. 11).

Table 4. Temperature variation table by He pressure.

He press. [T]	F/R [sccm]	Temp. [℃]	Diff. [Hen-Hen-1]
He_1 9	100.64	330.2	
He_2 8	88.04	340.4	10.2
He_3 7	75.59	386.5	46.1
He_4 6	62.85	418.6	32.1
He_5 5	50.39	453.2	34.6
He_6 4	38.40	484.0	30.8
He_7 3	26.66	523.4	39.4
He_8 2	15.82	568.8	45.4
He_9 1	6.74	620.3	51.5
He_{10} 0	0.73	681.1	60.8

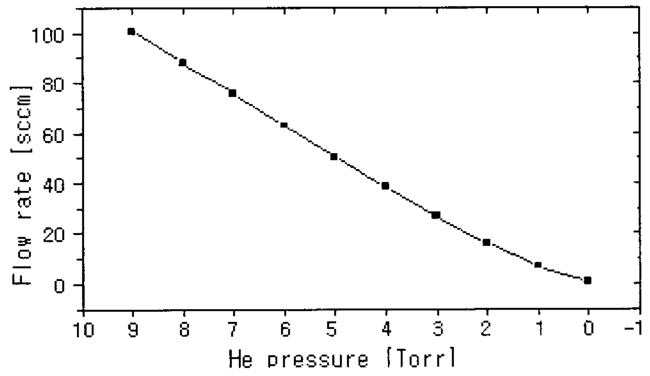


Fig. 10. Flow rate vs. pressure of He.

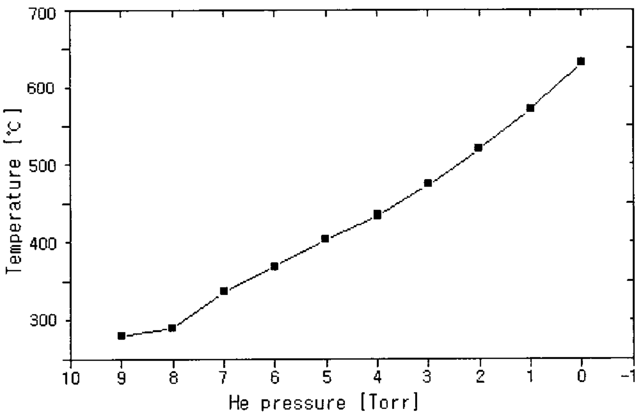


Fig. 11. Stabilized temperature by He pressure.

4. CONCLUSION

Melting points of the materials on metal layer are about 660℃ for Al and over 1660℃ for Ti, and TiN. And when Al is given thermal stress over half of its melting point during a constant time, its deformation can be slowly generated. We found He gas flowing for cooling a wafer is heavily dominant in controlling process temperature on HDP-CVD system. So the results of this test indicates that the failure of via resistance caused by melted Al could be happened when the cooling effect of He gas flowing to the backside of a wafer is considerably decreased (below 4Torr in this case). Therefore it is very important to prevent from He leak error on HDP-CVD system and right hand-off calibration, removal of particles between ESC and a wafer, and its non-sliding is needed to remove it. Addition to those the way to get rid of the migration of Al by He leak error is that HF-RF power, which increases the temperature by generation of sputter etch with Ar, is made turn off in the occurrence of the error.

ACKNOWLEDGEMENTS

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